# BeagleBoard-xM Rev C2
# System Reference Manual

**Revision 0.0**
**October 11, 2012**

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—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by this manual for compliance could void the user's authority to operate the equipment.

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## THIS DOCUMENT



For any questions, concerns, or issues submit them to gerald@BeagleBoard.org

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Please refer to sections 12 and 13 of this document for the board checkout procedures and troubleshooting guides.

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**NOTES**

# 1.0 Introduction

This document is the System Reference Manual for the BeagleBoard-xM, a low cost ARM Cortex A8 board supported through BeagleBoard.org. This document provides detailed information on the overall design and usage of the BeagleBoard from the system level perspective. It is not intended to provide detailed documentation of the processor or any other component used on the board. It is expected that the user will refer to the appropriate documents for these devices to access detailed information.

The processor used on the BeagleBoard-xM is compatible with several Cortex A8 processors manufactured by Texas Instruments. Currently, the processor is a DM3730 processor manufactured and sold by Texas Instruments and information on this can be found at the TI website. Additional information for the ARM only version, AM3715, can also be found on the TI website. The key difference between the AM3715 and the DM3730, is that the DSP is not included on the AM3715.

For the remainder of this document the DM3730 will be referred to as the processor.

The key sections in this document are:

**Section 2.0– Change History**
Provides tracking for the changes made to the System Reference Manual.

**Section 3.0– Definitions and References**
This section provides definitions for commonly used terms and acronyms.

**Section 4.0– Overview**
This is a high level overview of the BeagleBoard.

**Section 5.0– Specification**
Provided here are the features and electrical specifications of the BeagleBoard.

**Section 6.0-Product Contents**
Describes what the BeagleBoard package looks like and what is included in the box.

**Section 7.0– Connections**
Covered here is how to connect the various cables to the BeagleBoard.

**Section 8.0– System Architecture and Design**
This section provides information on the overall architecture and design of the BeagleBoard. This is a very detailed section that goes into the design of each circuit on the board.

**Section 9.0– Connector Pinouts and Cables**
The section describes each connector and cable used in the system. This will allow the user to create cables, purchase cables, or to perform debugging as needed.

**Section 10.0– BeagleBoard Accessories**

Covered in this section are a few of the accessories that may be used with BeagleBoard. This is not an exhaustive list, but does provide an idea of the types of cables and accessories that can be supported and how to find them. It also provides a definition of what they need to be. It does not guarantee that these devices will work on all OS implementations.

**Section 11.0 – Mechanical**

Information is provided here on the dimensions of the BeagleBoard.

**Section 12.0 – Troubleshooting**

Here is where you can find tips on troubleshooting the setup of the BeagleBoard.

**Section 13.0- Known Issues**

This section describes the known issues with the current revision of the BeagleBoard and any workarounds that may be possible.

**Section 14.0- BeagleBoard Components**

This section provides information on the top and bottom side silkscreen of the BeagleBoard showing the location of the components.

**Section 15.0- BeagleBoard Schematics**

These are the schematics for the BeagleBoard and information on where to get the PDF and OrCAD files..

**Section 16.0- Bill Of Material**

This section describes where to get the latest Bill of Material for the BeagleBoard.

**Section 17.0- BeagleBoard PCB Information**

This section describes where to get the PCB file information for the BeagleBoard.

# 2.0 Change History

## 2.1 Change History

**Table 1** tracks the changes made for each revision of this document.

**Table 1. Change History**

| Rev | Changes | Date | By |
|---|---|---|---|
| A | Initial release. | 6/4/2010 | GC |
| A1 | Updated to new power OVP scheme | 6/21/2020 | GC |
| A2 | Updated with camera and Memory information | 7/23/2010 | GC |
| A3 | Moved to Rev B PCB. | 10/18/2010 | GC |
| B | Moved to ES1.1 silicon revision. | 10/26/2010 | GC |
| C | Design changes and moved to revision ES1.2 silicon | 4/4/2010 | GC |
| C1.1 | Changed Table 5 to reflect GPIO4 instead of GPIO7for the user button.<br>Change section 7.20.1.1 to reflect I2C1 instead of I2C2. | 1/17/201 | GC |
| C2 | Changed POP memory part number due to obsolescence of the current device. | 10/11/2012 | GC |

## 2.2 BeagleBoard vs. BeagleBoard-xM

There are several differences between the **BeagleBoard** and the **BeagleBoard-xM** . The **BeagleBoard** refers to the original board and the **BeagleBoard-xM** is the newer version.

### 2.2.1 Hardware Changes

| AREA | BeagleBoard-xM | BeagleBoard | Comments |
|---|---|---|---|
| Processor | DM3730 | OMAP3530 | |
| ARM Frequency | 1GHZ | 720MHz | |
| DSP Frequency | 800Mhz | 520MHz | |
| SGX Frequency | 200Mhz | 110MHz | |
| DDR | 512MB | 256MB | |
| DDR Speed | 166MHz | 166MHz | |
| NAND | 0 | 256MB | |
| SD Connector | uSD | MMC/SD | |
| USB Host Ports | 4 | 1 | |
| Host Port Speed | FS/LS/HS | HS | |
| Serial Connector | DB9 | Header | Direct connect to USB to Serial Cable |
| Camera Header | Yes | No | Leopard Imaging Camera module |
| Ships with 4G SD | Yes | No | Contains bootable desktop |
| Overvoltage Protection | Yes | No | |
| Power LED turnoff | Yes | No | |
| Serial Port Power Turnoff | Yes | No | |

| | | | |
|---|---|---|---|
| MMC3 Expansion Header | Yes | No | |
| McBSP2 Expansion Header | Yes | No | |

### 2.2.2 Software Changes

Following are the changes to the SW.

- Use of a universal Beagle XLoader and UBoot. These will work on any Beagle made. They include support for the 512MB DDR and the removal of the NAND from the –xM board.
- A demo version of the Angstrom desktop distribution.

## 2.3 –xM Revision A2 vs. –xM Revision A3

There were no major hardware feature changes between the Rev A2 and Rev A3 revisions. Below are the differences between the Rev A2 and Rev A3 revisions.

- Slightly modified PCB layout (Rev B) to correct the following
  - Changed silkscreen on L12 to R159 to reflect the usage of a resistor instead of an inductor. Resistor was used on Rev A2. **No electrical difference**.
  - Changed routing on R66 and R68 to make them separate paths instead of parallel. **No electrical difference**.
  - Added 33 ohm resistor R157 in series with MMC clock line. Not used on board, only for expansion. **No electrical difference.**
  - Added R158 to allow isolation of drain pin on TPS2141. Loaded with a zero ohm resistor. **No electrical difference.**
  - Moved DVI_PUP pin to the TPS65950 GPIO2. No SW impact and Angstrom kernel, however, updated SW can be used to turn off the DVI interface by taking the pin LO. There may be issues with other distributions until such time as their code is updated. **Electrical change from A2**.
  - Added R160 and R155 as a possible future option. Not populated on Rev A3. **No electrical difference.**
  - Changed R120 to 0603 package to align with arts purchased. **No electrical difference.**
  - Added R156 to remove the required lifting of U18 pin 4. Resistor is not loaded on Revision A3. **No electrical difference.**

## 2.4 –xM Revision A3 vs. –xM Revision B

The only change from Rev –A3 to the Rev B was the replacement of the processor form ES1.0 to ES1.1. For a detailed description of the issues present in the ES1.1 revision,

please refer to http://focus.ti.com/lit/er/sprz319a/sprz319a.pdf . There are no issues resolved by ES1.1 that are anticipated to have any impact on the operation of the BeagleBoard-xM.

### 2.5 –xM Revision B vs. –xM Revision C

There were seven changes made to the BeagleBoard-xM Rev C version over the Rev B design.

- Resistor loading was changed to allow for the reading of the Rev C revision by the SW. GPIO171=0, GPIO_172=1, and GPIO_173=0.
- Replacement of the processor from ES1.1 to ES1.2. For a detailed description of the issues present in the ES1.2 revision, please refer to http://focus.ti.com/lit/er/sprz319a/sprz319a.pdf . There are no issues resolved by ES1.2 that are anticipated to have any impact on the operation of the BeagleBoard-xM. ES1.2 is the latest revision.
- Fixed capacitor footprint in the PCB layout.
- Replaced the microSD connector with a new part. The current part was targeted for EOL and a new one was required. This required a PCB footprint change.
- Redesigned the overvoltage protection circuit. We were seeing issues with a small number of boards being damaged on the TPS2054 USB power FET, so a new design was implemented. Overall operation is the same as the original version with te exception that it is now possible to power the entire board over the USB OTG port. This includes the HUB. Care should be taken not to add high current devices on the USB ports as that will cause the host to shut down the USB port,
- Changed the default power state of the USB HUB to OFF as an added layer of protection to make sure the USB power rails are off on initial power up. This will minimize the initial current drain on the board. SW can turn on the HUB power as needed by setting the TPS65950 LEDA/VIBRA.P pin LO to turn it on.
- Added the ability for the SW to detect when the board is powered from the DC supply or the OTG supply. Status is read from GPIO.6 pin on the TPS65950. If LO, then the board is powered from the DC jack. The HUB will only work in the DC powered mode so this change allows the board to know not to try and initialize the USB Host when under OTG power.

## 2.6 –xM Revision C vs. –xM Revision C1

There was only one change made on the Revision C1 board. The pads on the expansion headers wee beefed up to address some issues we were seeing where there was a disconnect between the etch and the pads inside the PCBs.

## 2.7 –xM Revision C1 vs. –xM Revision C2

There was only one change made on the Revision C2 board. The LPDDR POP memory is being made obsolete by Micron. The new part is being used on the manufacture of the revision C1 board. There are no functional differences as a result of this change. And no SW changes are required. The new part number is MT46H128M32L2KQ-5 WT:B.

## 2.8 Definitions

**SD**- Secure Digital
**microSD**- Small version of the standard SD card
**MDDR**- Mobile Dual Data Rate
**SDRAM-** Synchronous Dynamic Random Access Memory
**BeagleBoard**- The original version of the board based on the DM3530
**BeagleBoard-xM**- The newer version of the board based on the DM3730.

# 3.0 BeagleBoard Overview

The BeagleBoard is designed specifically to address the Open Source Community. It has been equipped with a minimum set of features to allow the user to experience the power of the processor and is not intended as a full development platform as many of the features and interfaces supplied by the processor are not accessible from the BeagleBoard. By utilizing standard interfaces, the BeagleBoard is highly extensible to add many features and interfaces. It is not intended for use in end products. All of the design information is freely available and can be used as the basis for a product. BeagleBoards will not be sold for use in any product as this hampers the ability to get the boards to as many community members as possible and to grow the community.

## 3.1 BeagleBoard Versions

There are two different versions of the beagle in production, the BeagleBoard and the BeagleBoard–xM. **Figure 1** is a picture of each of these versions. This manual covers the revision A and B of the –xM version only. Please refer to the BeagleBoard System Reference Manual for information on that version. It can be found at http://beagleboard.org/hardware/design .

The **Figure 1** shows pictures of the two different versions. The **BeagleBoard** is on the left and the **BeagleBoard–xM** is on the right.

**Figure 1. BeagleBoard and BeagleBoard-xM**

# 4.0 BeagleBoard Specification

This section covers the specifications of the BeagleBoard and provides a high level description of the major components and interfaces that make up the BeagleBoard.

## 4.1 BeagleBoard Features

**Table 2** provides a list of the BeagleBoard's features.

**Table 2. BeagleBoard-xM Features**

| | Feature | |
|---|---|---|
| **Processor** | Texas Instruments Cortex A8 1GHz processor | |
| **POP Memory** | Micron 4Gb MDDR SDRAM (512MB) 200MHz | |
| **PMIC TPS65950** | Power Regulators | |
| | Audio CODEC | |
| | Reset | |
| | USB OTG PHY | |
| **Debug Support** | 14-pin JTAG | GPIO Pins |
| | UART | 3 LEDs |
| **PCB** | 3.1" x 3.0" (78.74 x 76.2mm) | 6 layers |
| **Indicators** | Power, Power Error | 2-User Controllable |
| | PMU | USB Power |
| **HS USB 2.0 OTG Port** | Mini AB USB connector | |
| | TPS65950 I/F | |
| **USB Host Ports** | SMSC LAN9514 Ethernet HUB | |
| | 4 FS/LS/HS | Up to 500ma per Port if adequate power is supplied |
| **Ethernet** | 10/100 | From USB HUB |
| **Audio Connectors** | 3.5mm | 3.5mm |
| | L+R out | L+R Stereo In |
| **SD/MMC Connector** | MicroSD | |
| **User Interface** | 1-User defined button | Reset Button |
| **Video** | DVI-D | S-Video |
| **Camera** | Connector | Supports Leopard Imaging Module |
| **Power Connector** | USB Power | DC Power |
| **Overvoltage Protection** | Shutdown @ Over voltage | |
| **Main Expansion Connector** | Power (5V & 1.8V) | UART |
| | McBSP | McSPI |
| | I2C | GPIO |
| | MMC2 | PWM |
| **2 LCD Connectors** | Access to all of the LCD control signals plus I2C | 3.3V, 5V, 1.8V |
| **Auxiliary Audio** | 4 pin connector | McBSP2 |
| **Auxiliary Expansion** | MMC3 | GPIO,ADC,HDQ |

The following sections provide more detail on each feature and sections of the BeagleBoard.

## 4.2 Processor

The BeagleBoard-xM processor is the DM3730CBP 1GHz version and comes in a .4mm pitch POP package. POP (Package on Package) is a technique where the memory is mounted on top of the processor. For this reason, when looking at the BeagleBoard, you will not find an actual part labeled DM3730CBP, but instead see the part number for the memory.

## 4.3 Memory

There are two possible memory devices used on the –xM. The -00 assembly uses the Micron POP memory and the -01 uses the Numonyx POP memory. The key function of the POP memory is to provide:

- 4Gb MDDR SDRAM x32 (512MB @ 166MHz)

Unlike with earlier versions of the board, no other memory devices are on the BeagleBoard. It is possible however, that additional non volatile memory storage can be added to BeagleBoard by:

- Accessing the memory on the uSD card
- Use the USB OTG port and a powered USB hub to drive a USB Thumb drive or hard drive.
- Install a thumbdrive into one of the USB ports
- Add a USB to Hard Disk adapter to one of the USB ports

Support for these devices is dependent upon driver support in the OS.

## 4.4 Power Management

The TPS65950 is used on the BeagleBoard to provide power with the exception of a 3.3V regulator which is used to provide power to the DVI-D encoder and RS232 driver and an additional 3.3V regulator to power the USB Hub. In addition to the power the TPS65950 also provides:

- Stereo Audio Out
- Stereo Audio in
- Power on reset
- USB OTG PHY
- Status LED

### 4.5 HS USB 2.0 OTG Port

The USB OTG port can be used as the primary power source and communication link for the BeagleBoard and derives power from the PC over the USB cable. The client port is limited in most cases to 500mA by the PC. There are instances where the PC or laptop does not supply sufficient current to power the board as it does not provide the full 500mA. Under this mode the USB HUB will now be powered based on the design changes made to the over volt circuitry. Care should be taken not to overload the USB ports as the total power supplied to the ports will not enable full power to all of the USB ports as you can have with the DC power.

It is possible to take the current supplied by the USB ports to 1A by using a Y cable. **Figure 2** shows and example of the Y-Cable for the USB.

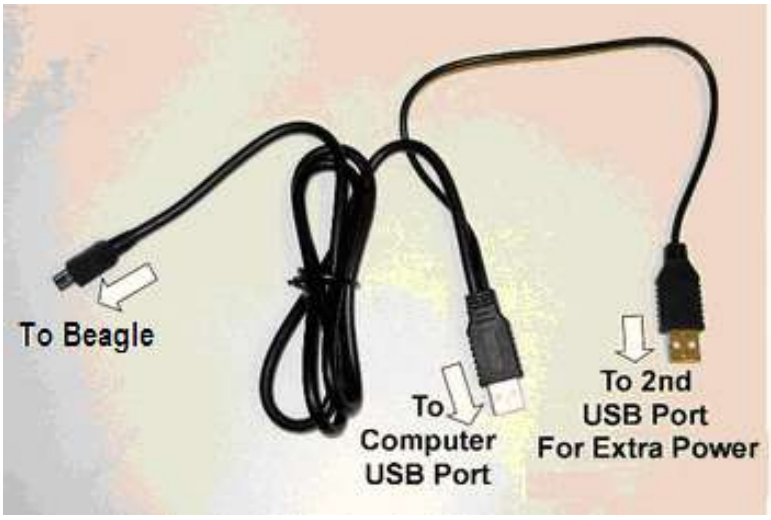



**Figure 2. USB Y-Cable**

The BeagleBoard requires a Y-Cable minAB to USB A cable or as mentioned a single cable can be used if the USB Hub is powered down or not loaded on all of the ports.

### 4.6 HS USB 2.0 Host Ports

On the board are four USB Type A connectors with full LS/FS/HS support. Each port can provide power on/off control and up to 500mA of current at 5V as long as the input DC is at least 3A. The ports will not function unless the board is powered by the DC jack. They cannot be powered via the OTG port.

### 4.7 Stereo Audio Output Connector

A 3.5mm standard stereo output audio jack is provided to access the stereo output of the onboard audio CODEC. The audio CODEC is provided inside the TPS65950.

### 4.8 Stereo Audio In Connector

A 3.5mm standard stereo audio input jack is provided to access the stereo output of the onboard audio CODEC.

### 4.9 S-Video Connector

A 4 pin DIN connector is provided to access the S-Video output of the BeagleBoard. This is a separate output from the processor and can contain different video output data from what is found on the DVI-D output if the software is configured to do it.

It will support NTSC or PAL format output to a standard TV. The default is NTSC, but can be changed via the Software.

### 4.10 DVI-D Connector

The BeagleBoard can drive a LCD panel equipped with a DVI-D digital input. This is the standard LCD panel interface of the processor and will support 24b color output. DDC2B (Display Data Channel) or EDID (Enhanced Display ID) support over I2C is provided in order to allow for the identification of the LCD monitor type and the required settings.

The BeagleBoard is equipped with a DVI-D interface that uses an HDMI connector that was selected for its small size. It does not support the full HDMI interface and is used to provide the DVI-D interface portion only. The user must use a HDMI to DVI-D cable or adapter to connect to a LCD monitor. This cable or adapter is not provided with the BeagleBoard. A standard HDMI cable can be used when connecting to a monitor with an HDMI connector.

**DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.**

### 4.11 LCD Header

A pair of 1.27mm pitch 2x10 headers are provided to gain access to the LCD signals. This allows for the creation of LCD boards that will allow adapters to be made to provide the level translation to support different LCD panels.

### 4.12 microSD Connector

A single microSD connector is provided as a means for the main non-volatile memory storage on the board. This replaces the 6 in 2 SD/MMC connector found on the BeagleBoard.

### 4.13 Reset Button

When pressed and released, causes a power on reset of the BeagleBoard.

### 4.14 User Button

A button is provided on the BeagleBoard to be used as an application button that can be used by SW as needed. As there is no NAND boot option on the board, this button is no longer needed to force an SD card boot. It is can be used by the UBoot SW to switch between user scripts to allow different boot configurations to be selected as long as that feature is included in the UBoot used. If you press this button on power up, the board will not boot properly.

### 4.15 Indicators

There are five green LEDs on the BeagleBoard that can be controlled by the user.

- One on the TPS65950 that is programmed via the I2C interface
- Two on the processor controlled via GPIO pins
- One Power LED that indicates that power is applied and can be turned off via SW.
- One to indicate that power is applied to the onboard USB HUB and can be controlled via the SW.

There is also one red LED on the BeagleBoard that provides an indication that the power connected to the board exceeds the voltage range of the board. If this LED ever turns on, please remove the power connector and look for the correct power supply in order to prevent damage to the board.

### 4.16 Power Connector

Power can be supplied via the USB OTG connector for some application that does not require the USB Host ports. A wall supply 5V can be plugged into the DC power jack fro full access to all functions of the board. When the wall supply is plugged in, it will remove the power path from the USB connector and will be the power source for the whole board. The power supply is not provided with the BeagleBoard.

When using the USB OTG port in the host mode, the DC supply must be connected as the USB port will be used to provide limited power to the hub at a maximum of 100mA, so the hub must be powered. The 100mA is not impacted by having a higher amperage supply plugged into the DC power jack. The 100mA is a function of the OTG port itself. Make sure the DC supply is regulated and a clean supply. If the power is over the voltage specification, a RED LED will turn on. This will prevent the power from actually making it to the circuitry on the board and will stay on as long as the power exceeds the voltage specification.

### 4.17 JTAG Connector

A 14 pin JTAG header is provided on the BeagleBoard to facilitate the SW development and debugging of the board by using various JTAG emulators. The interface is at 1.8V on all signals. Only 1.8V Levels are supported. **DO NOT expose the JTAG header to 3.3V.**

### 4.18 RS232 DB9 Connector

Support for RS232 via UART3 is provided by DB9 connector on the BeagleBoard for access to an onboard RS232 transceiver. A USB to Serial cable can be plugged directly into the Beagle. Unlike on the original version of the Beagle, a straight through non null modem cable is required. The cable you used on the BeagleBoard will NOT work on the –xM version. A standard male to female straight DB9 cable may be used or you can use a USB to serial adapter that will plug directly into the board without the need for any other cables.

### 4.19 Main Expansion Header

A single 28 pin header is provided on the board to allow for the connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin. This header is populated on each board.

### 4.20 Camera Connector

A single connector has been added to the BeagleBoard–xM board for the purpose of supporting a camera module. The camera module does not come with the board but can be obtained from Leopard Imaging. The supported resolutions include VGA, 2MP, 3MP, and 5MP camera modules. For proper operation of the cameras, the correct SW drivers are required. This connector is populated on the board and is ready for the camera module to be installed.

### 4.21 MMC3 Expansion Header

New to the BeagleBoard-xM is a 20 pin connector provided to allow access to additional signals including GPIO and the MMC3 port. This connector is populated on the board.

### 4.22 McBSP Expansion Header

A 4 pin connector is provided to allow access to the McBSP2 signals for audio applications. In order to use these signals, the audio interface on the TPS65950 must be disabled by the SW. This connector is populated on the board..

### 4.23 BeagleBoard Mechanical Specifications

| | |
|---|---|
| Size: | 3.35” x 3.45” |
| Max height: | TBM |
| Layers: | 6 |
| PCB thickness: | .062” |
| RoHS Compliant: | Yes |
| Weight: | TBW |

## 4.24 Electrical Specifications

**Table 3** is the electrical specification of the external interfaces to the BeagleBoard-xM Rev C.

**Table 3. BeagleBoard Electrical Specification -xM Rev C**

| Specification | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Power** | | | | |
| Input Voltage USB | | 5 | 5.2 | V |
| Current USB | | 350 | | mA |
| Input Voltage DC | 4.8 | 5 | 5.2 | V |
| Current DC | | 750 | | mA |
| Max Voltage without damage | | | 12 | V |
| Expansion Voltage (5V) | 4.8 | 5 | 5.2 | V |
| Curent (Dépends on source curent available) | | 750 | | A |
| Expansion Voltage (1.8V) | 1.75 | 1.8 | 1.85 | V |
| Current | | | 30 | mA |
| USB Host (Same as the DC supplied by the power plug or USB 5V) | 4.8 | 5 | 5.2 | V |
| Current (Depends on what the DC source can supply over what the board requires) | | Varies | | |
| Maximum current supplied by all four USB Host ports Total | | 1500 | | mA |
| **USB OTG** | | | | |
| High Speed Mode | | | 480 | Mb/S |
| Full Speed Mode | | | 12.5 | Mb/S |
| Low Speed Mode | | | 1.5 | Mb/S |
| **USB Host** | | | | |
| High Speed Mode | | | 480 | Mb/S |
| Full Speed Mode | | | 12.5 | Mb/S |
| Low Speed Mode | | | 1.5 | Mb/S |
| **RS232** | | | | |
| Transmit | | | | |
| High Level Output Voltage | | 5 | 5.4 | V |
| Low Level output voltage | | -5 | -5.5 | V |
| Output impedance | | +/-35 | +/-60 | mA |
| Maximum data rate | 250 | | | Kbit/S |
| Receive | | | | |
| High level Input Voltage | -2.7 | -3.2 | | V |
| Lo Level Input Voltage | | | .4 | |
| Input resistance | 3 | 5 | 7 | Kohms |
| **JTAG** | | | | |
| Realview ICE Tool | | | 30 | MHz |
| XDS560 | | | 30 | MHz |
| XDS510 | | | 30 | MHz |
| Lauterbach(tm) | | | 30 | MHz |
| **microSD** | | | | |
| Voltage Mode 1.8V | 1.71 | 1.8 | 1.89 | V |
| Voltage Mode 3.0V | 2.7 | 3.0 | | V |
| Current | | | 220 | mA |
| Clock | | | 48 | MHz |
| **DVI-D** | | | | |
| Pixel Clock Frequency | 25 | | 65 | MHz |

| | | | | |
|---|---|---|---|---|
| High level output voltage | | 3.3 | | V |
| Swing output voltage | 400 | | 600 | mVp-p |
| Maximum resolution | | | 1024 x 768 | |
| **S-Video** | | | | |
| Full scale output voltage (75ohm load) | .7 | .88 | 1 | V |
| Offset voltage | | 50 | | mV |
| Output Impedance | 67.5 | 75 | 82.5 | Ohms |
| **Audio In** | | | | |
| Peak-to-peak single-ended input voltage (0 dBFs) | | | 1.5 | Vpp |
| Total harmonic distortion (sine wave @ 1.02 kHz @ -1 dBFs) | | -80 | -75 | dB |
| Total harmonic distortion (sine wave @ 1.02 kHz) 2 0 Hz to 20 kHz, A-weighted audio, Gain = 0 dB | | -85 | -78 | dB |
| **Audio Out** | | | | |
| Load Impedance @100 pF | 14 | 16 | | ohms |
| Maximum Output Power (At 0.53 Vrms differential output voltage and load impedance = 16 Ohms) | | 17.56 | | mW |
| Peak-to-Peak output voltage | | | 1.5 | Vpp |
| Total Harmonic Distortion @ 0 dBFs | | -80 | -75 | dB |
| Idle channel noise (20Hz to 20KHz) | | -90 | -85 | dB |
| **Environmental** | | | | |
| Temperature range | 0 | | +85 | C |

# 5.0 Product Contents

Under this section is a description of what comes in the box when the BeagleBoard is purchased.

## 5.1 BeagleBoard In the Box

The final packaged -xM Rev C product will contain the following items:

- 1 Box with the following items inside:
  - 1 BeagleBoard in an ESD Bag
  - 1 uSD card
  - 1 uSD Card to MMC Adapter

**NO CABLES ARE PROVIDED WITH THE BEAGLEBOARD.**


**Figure 3. The -xM Rev C Box**


**Figure 4. -xM Rev C Box Contents**

### 5.2 Software on the BeagleBoard

There is no NAND flash memory on the board so no SW is preinstalled on the board as it is on the BeagleBoard. The BeagleBoard–xM does come with a 4GB microSD card that the board boots from. It contains all of the code required for the board to boot to an Angstrom validation image. You will see a login prompt but no GUI will be visible. It can also be used to boot to UBoot by hitting a key during the booting process before it reads the UImage.

### 5.3 Repairs

If you feel the board is in need of repair, follow the RMA Request process found at http://beagleboard.org/support/rma

**Do not send the board in for repair until a RMA authorization has been provided.**

Do not return the board to the distributor unless you want to get a refund. You must get authorization from the distributor before returning the board. Beagleboard.org does not handle refunds.

# 6.0 BeagleBoard Connections

This section provides an overview of all of the connectors on the BeagleBoard-xM.

Only the use of FCC Part 15 approved devices in the BeagleBoard-xM installation is allowed. Care should be taken to insure that all add-on boards, power supplies, monitors, PC equipment, and any other add-on component or device meets the FCC Part 15 requirements. The user is responsible for compliance with this statement. Any changes or modifications to this board that causes the board to no longer comply with the FCC Part 15 requirements voids the user's rights to use this system.

## 6.1 Connecting USB OTG

The USB OTG port connects to the PC host and uses a miniAB cable through which power can be provided to the BeagleBoard. **Figure 5** shows where the cable is connected to the BeagleBoard.

If the OTG Port is to be used as a Host, the ID pin must be grounded. This means that you must have a 5 pin cable connected to the OTG port on the BeagleBoard and you must use a powered USB HUB. There is also an option to ground the ID on the board and is discussed later in this document. You can power the board from this port, but there may not be enough power supplied by the PC to power all features, such as the USB Host ports and the Ethernet Port. If you use the double ended USB cable, you should be able to power the board with minimal issues as long as you do not load down the USB Host ports with heavy current devices. This will depend on the current available from the HOST PC.

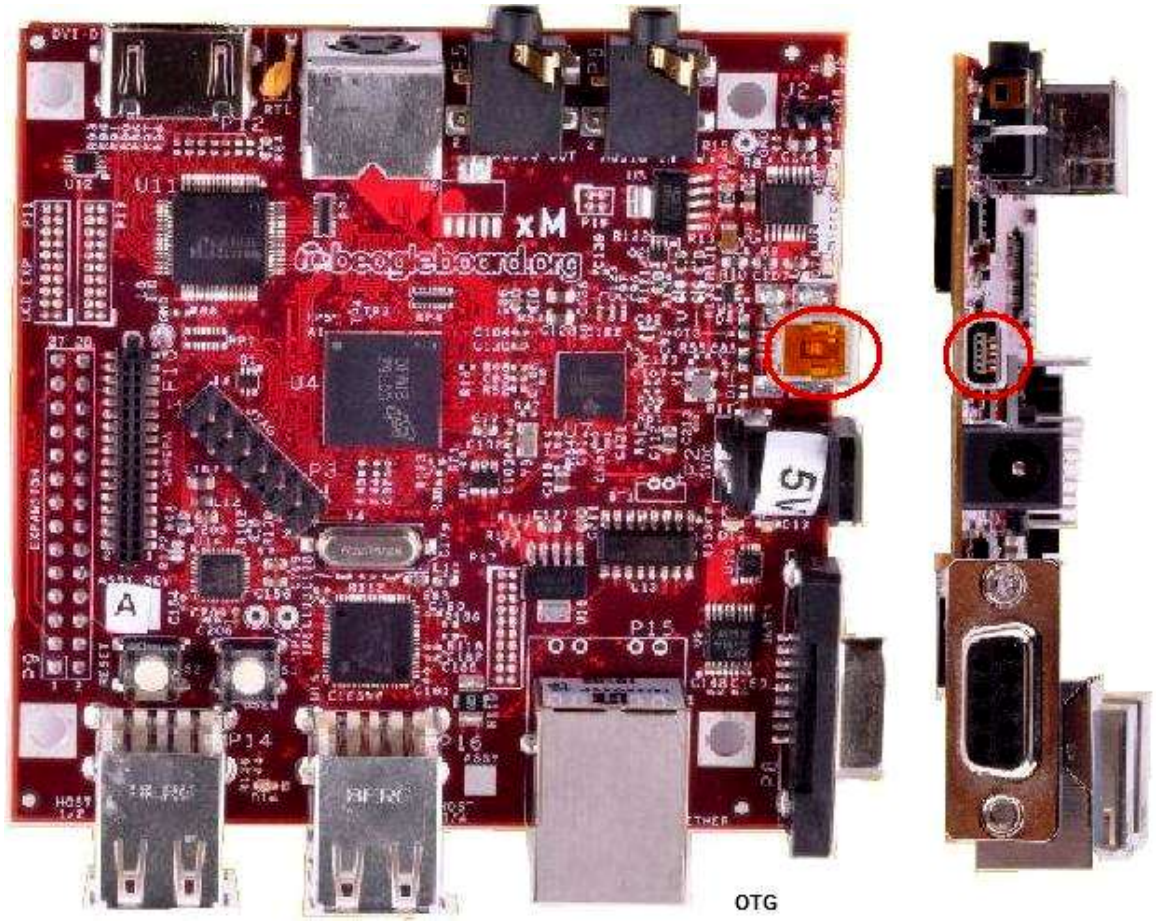



**Figure 5. USB OTG Connection**

## 6.2 Connecting USB Host

The Beagle is equipped with 4 USB Host connectors. **Figure 6** shows the location of the USB Host connectors.

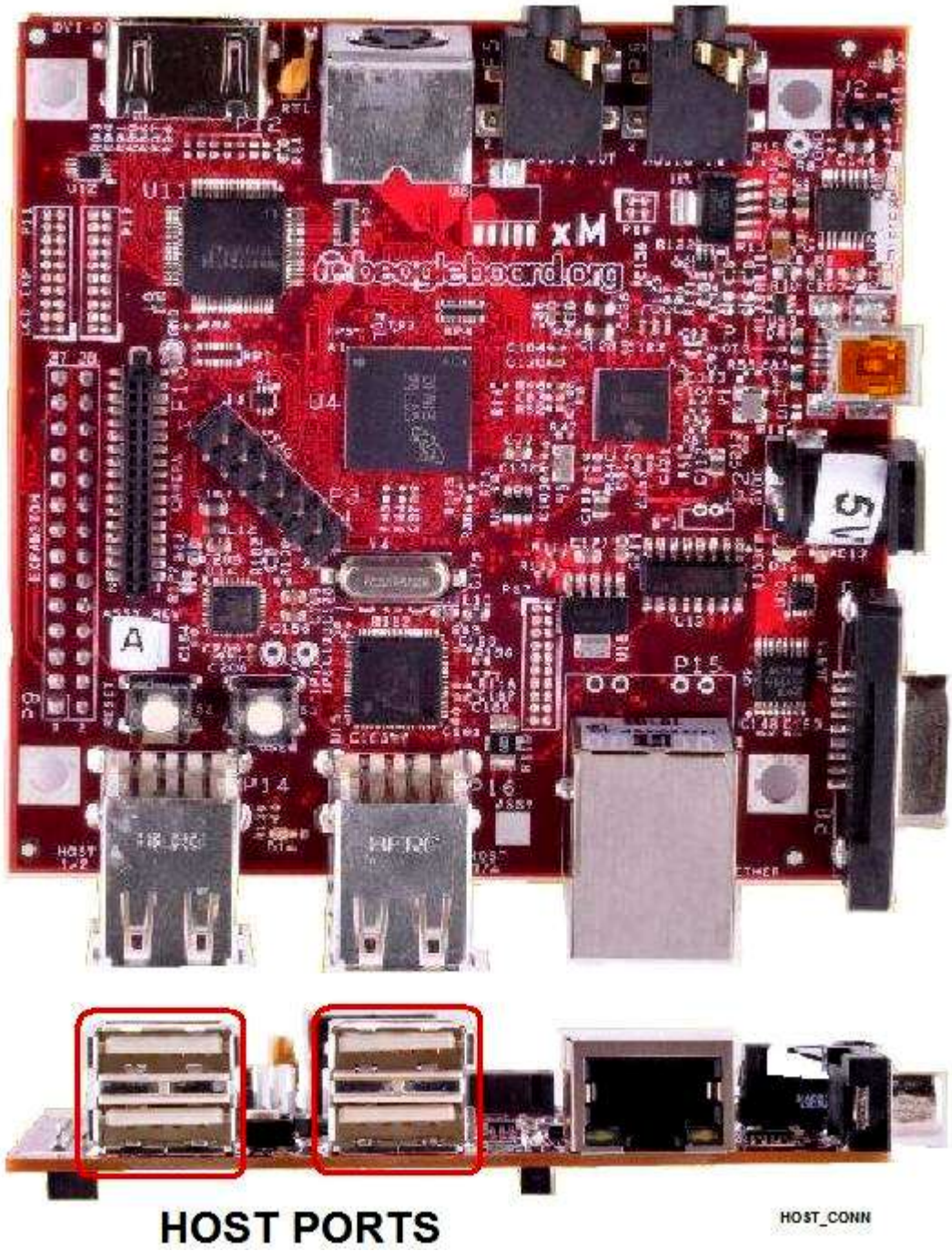



**Figure 6. USB Host Connection**

## 6.3 Connecting DC Power

A DC supply can be used to power the BeagleBoard by plugging it into the power jack. The power supply is not provided with the BeagleBoard, but can be obtained from various sources. You need to make sure the supply is a regulated 5V supply. **Figure 7** shows where to insert the power supply into the power jack.

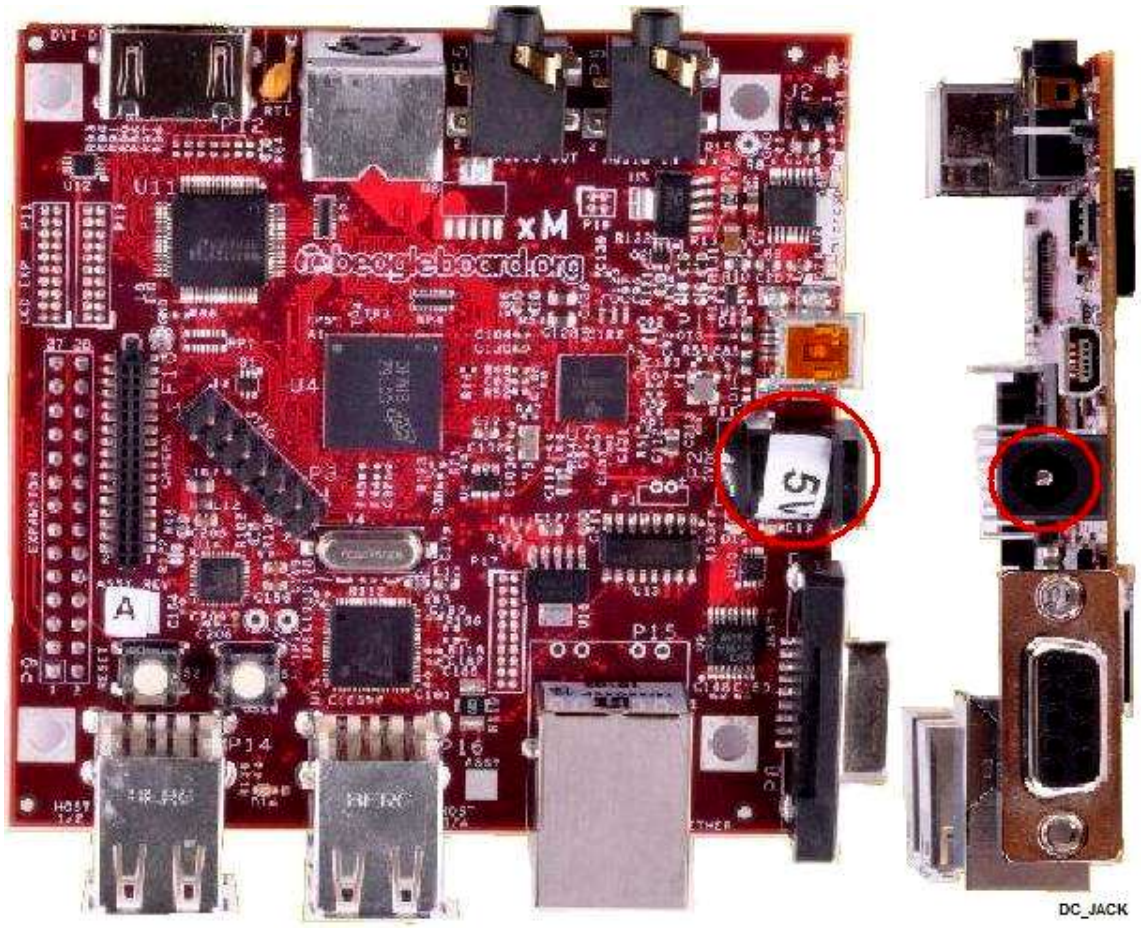



**Figure 7. DC Power Connection**

The power supply must have a 2.1mm I.D x 5.5mm O.D. x 9.5mm and can be either straight or right angle. Connecting anything other than 5V will activate the over voltage circuitry, turning on a red LED. The board will not function until the correct power supply is used. If you are using the USB OTG port in the OTG or host mode, you must have an external DC supply powering the BeagleBoard.

It is required that on the BeagleBoard-xM board that an external power supply used if the USB Host is to be used.

## 6.4 Connecting JTAG

A JTAG emulator can be used for advanced debugging by connecting it to the JTAG header on the BeagleBoard. Only the 14pin version of the JTAG is supported and if a 20pin version is needed, you will be required to contact your emulator supplier for the appropriate adapter to be supplied by that manufacturer. **Figure 8** shows the connection of the **JTAG** cable to the BeagleBoard.

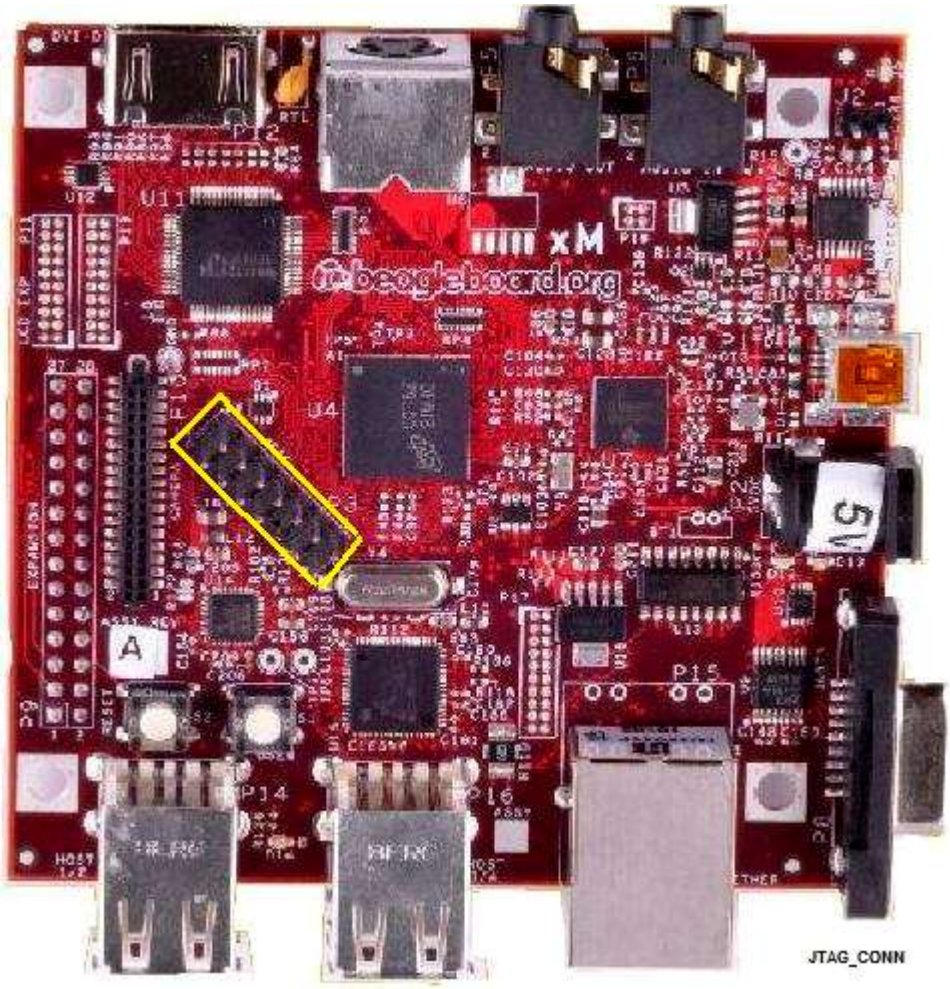



**Figure 8. BeagleBoard JTAG Connection**

DO NOT expose the JTAG header to 3.3V. It supports 1.8V only. There is no overvoltage protection on these pins and the pins connect direct to the processor. If you do this, the board will be damaged beyond repair and the board will NOT be replaced under any circumstances

## 6.5 Connecting Serial Cable

In order to access the serial port of the BeagleBoard a serial cable is required. New to the BeagleBoard-xM version is the removal of the 10 pin header and the addition of a female DB9 connector. The configuration of the DB9 is such that a USB to serial adapter can be plugged direct into the Beagle connector. No null modem cable is required. **Figure 9** shows where the serial cable is to be installed.

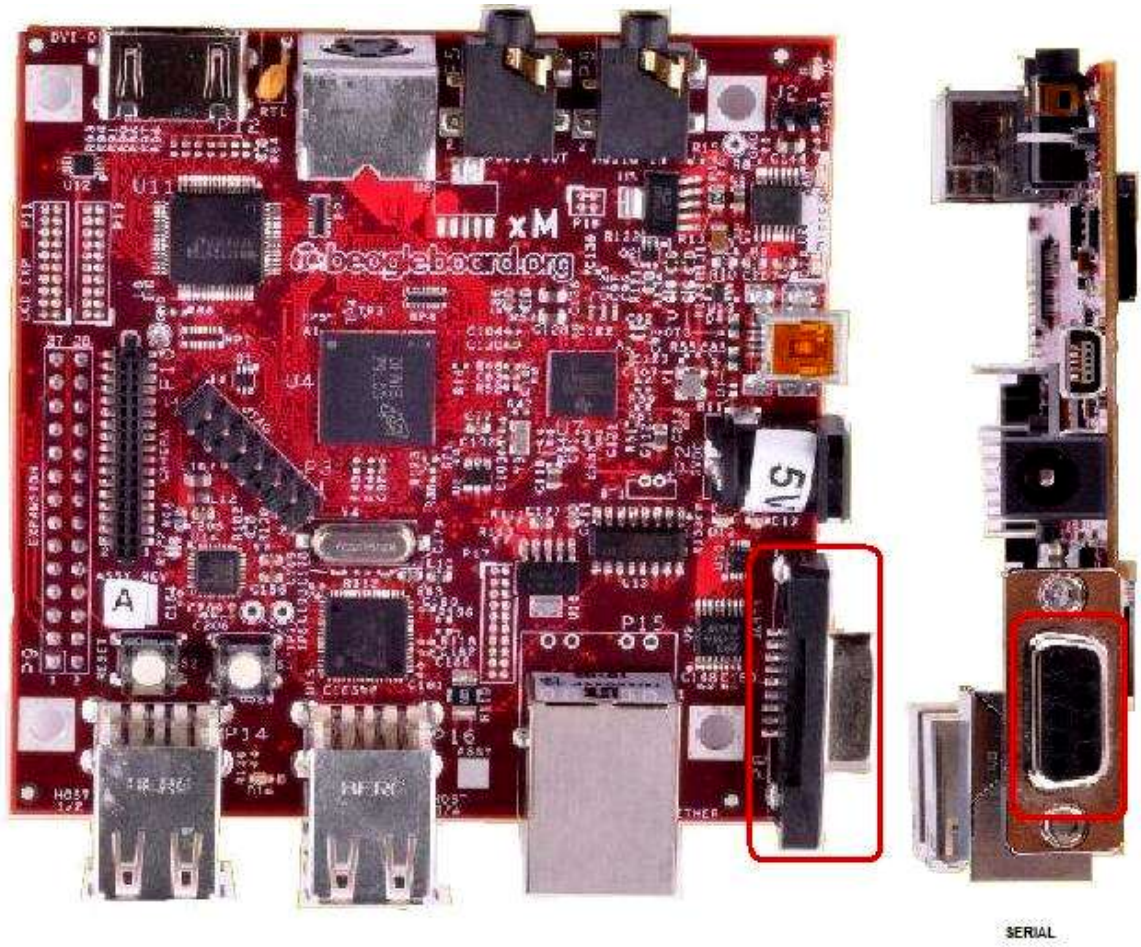



**Figure 9. BeagleBoard Serial Cable Connection**

If you are using a standard serial port on the PC, a straight through male to female cable is required. The cable used on the BeagleBoard will not work on the BeagleBoard–xM board.

## 6.6 Connecting S-Video

An S-Video cable can be connected to the BeagleBoard and from there it can be connected to a TV or monitor that supports an S-Video input. This cable is not supplied with the BeagleBoard. **Figure 10** shows the connector for the S-Video cable.

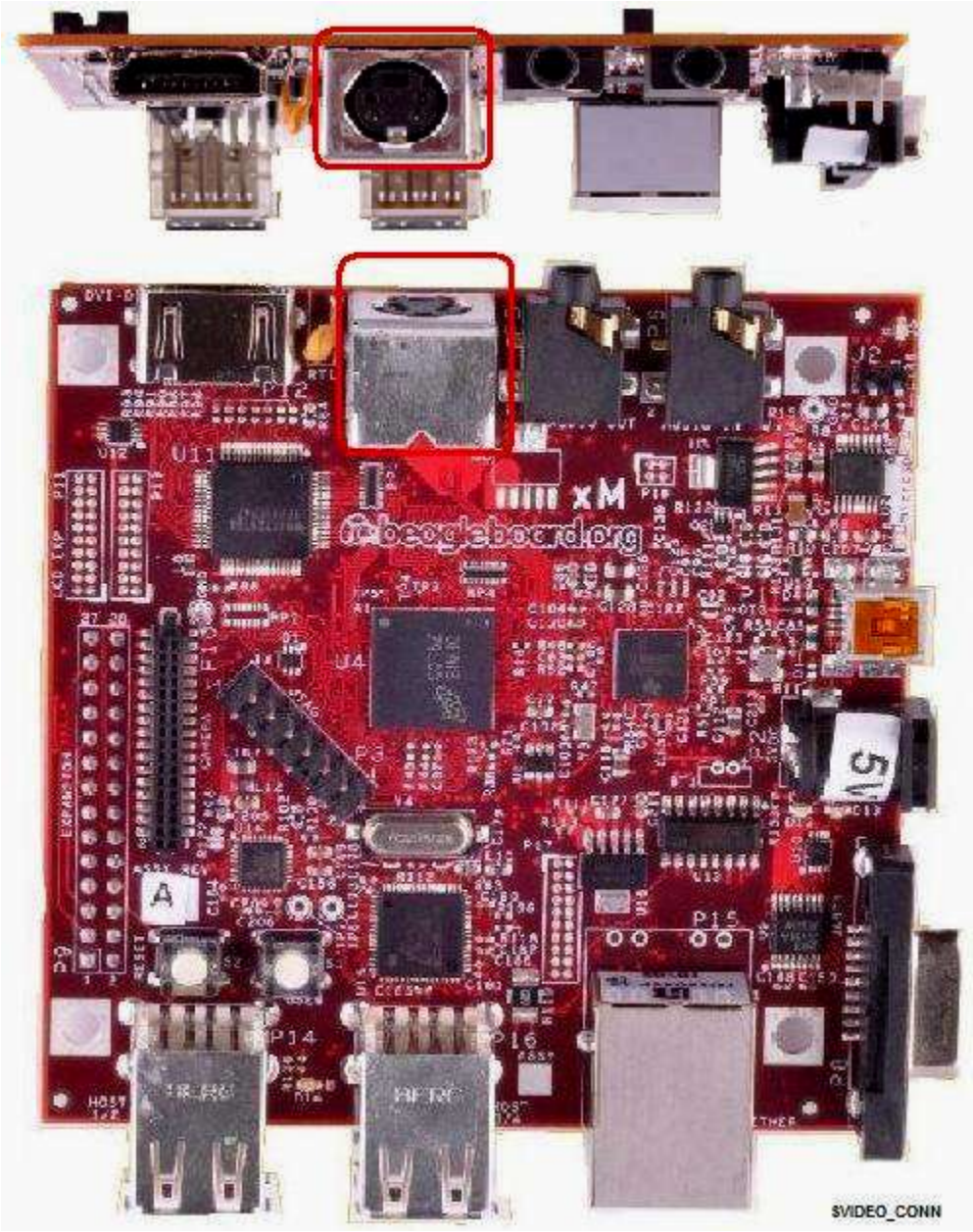



**Figure 10. BeagleBoard S-Video Connection**

## 6.7 Connecting DVI-D Cable

In order to connect the DVI-D output to a monitor, a HDMI to DVI-D cable is required. This cable is not supplied with BeagleBoard but can be obtained through numerous sources. **Figure 11** shows the proper connection point for the cable.

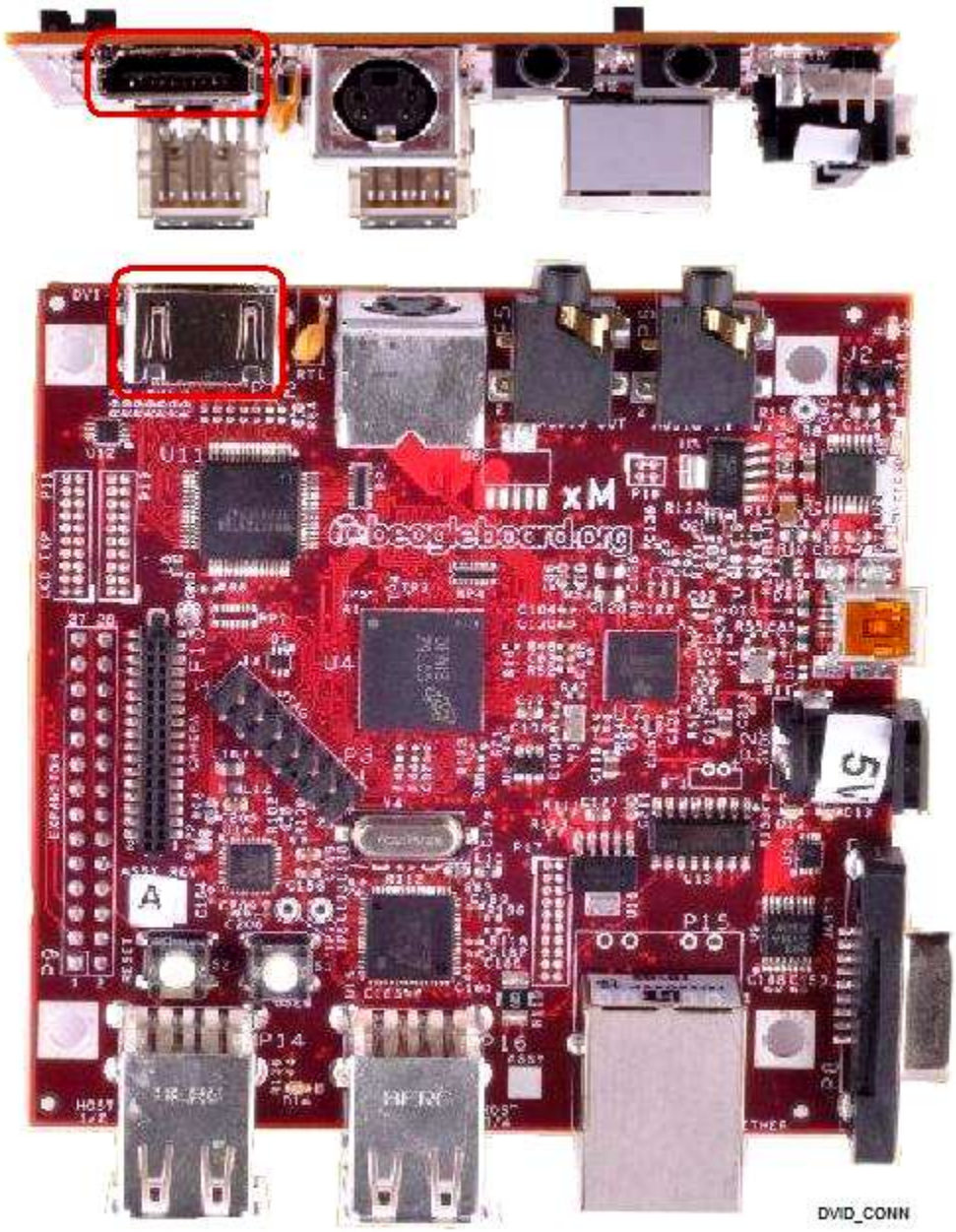



**Figure 11. BeagleBoard DVI-D Connection**

**DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.**

## 6.8 Connecting Stereo Out Cable

An external Audio output device, such as external stereo powered speakers, can be connected to the BeagleBoard via a 3.5mm jack. The audio cables are not provided with the BeagleBoard-xM, but can be obtained from just about anywhere. **Figure 12** shows where the cable connected to the stereo out jack.

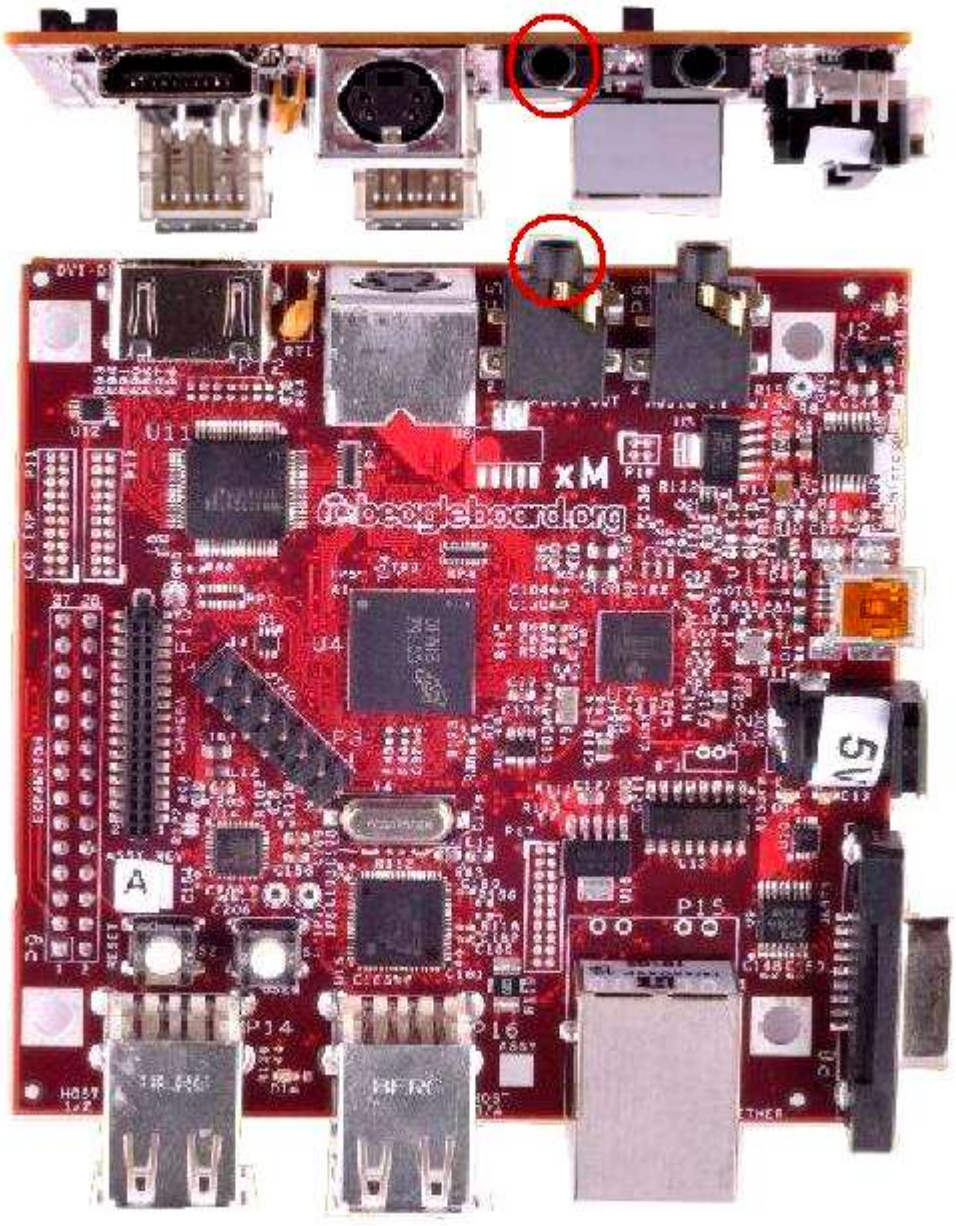



**Figure 12. BeagleBoard Audio Out Cable Connection**

## 6.9 Connecting Stereo In Cable

External Audio input devices, such as a powered microphone or the audio output of a PC or MP3 player, can be connected to the BeagleBoard-xM via a 3.5mm jack. The audio cables are not provided with the board, but can be obtained from several sources. **Figure 13** shows where the cable is connected to the stereo input jack.

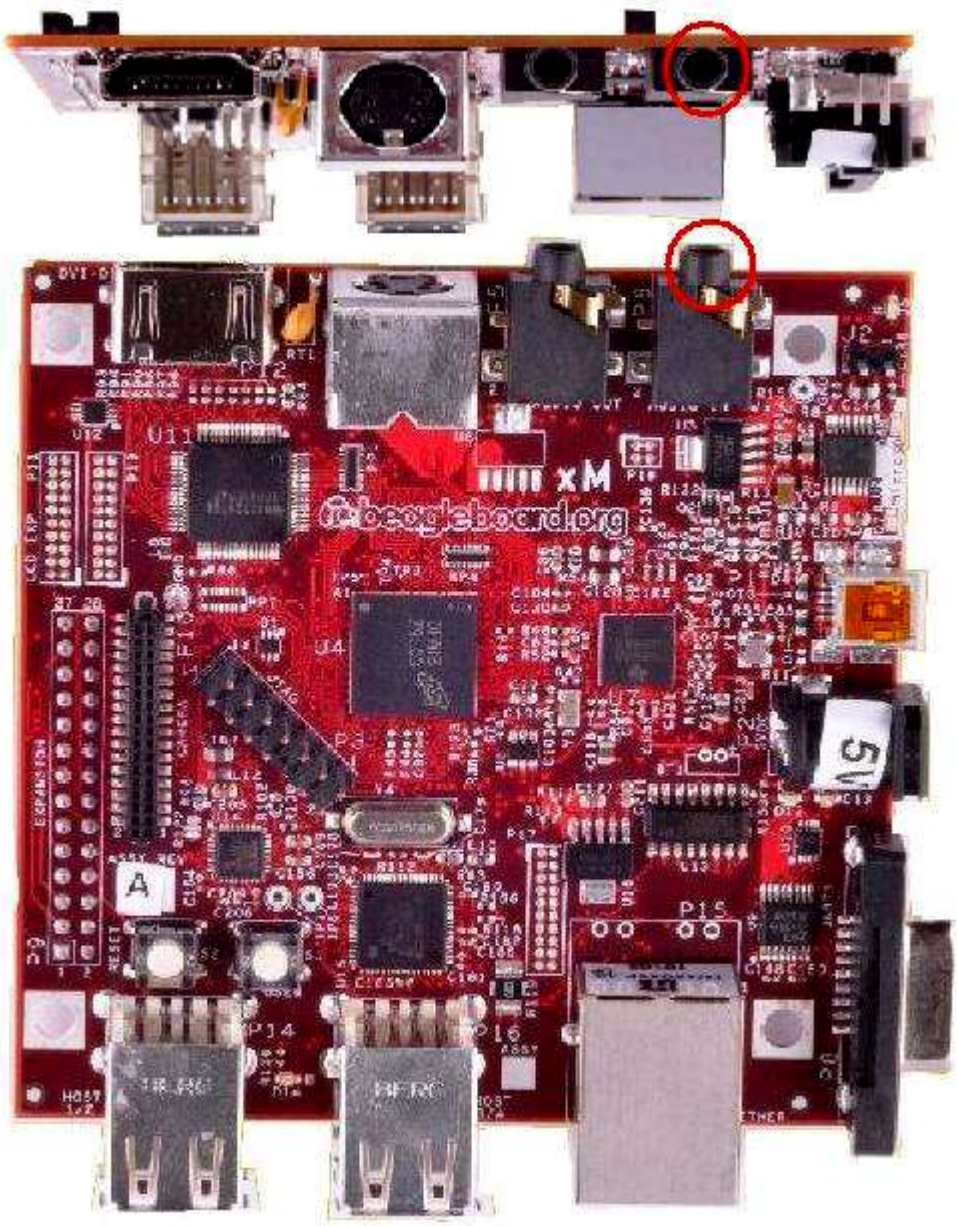



**Figure 13. BeagleBoard Audio In Cable Connection**

## 6.10 Indicator Locations

There are five green and one red indicator on the BeagleBoard. **Figure 14** shows the location of each indicator. Each indicator will be described in more detail later in this document.

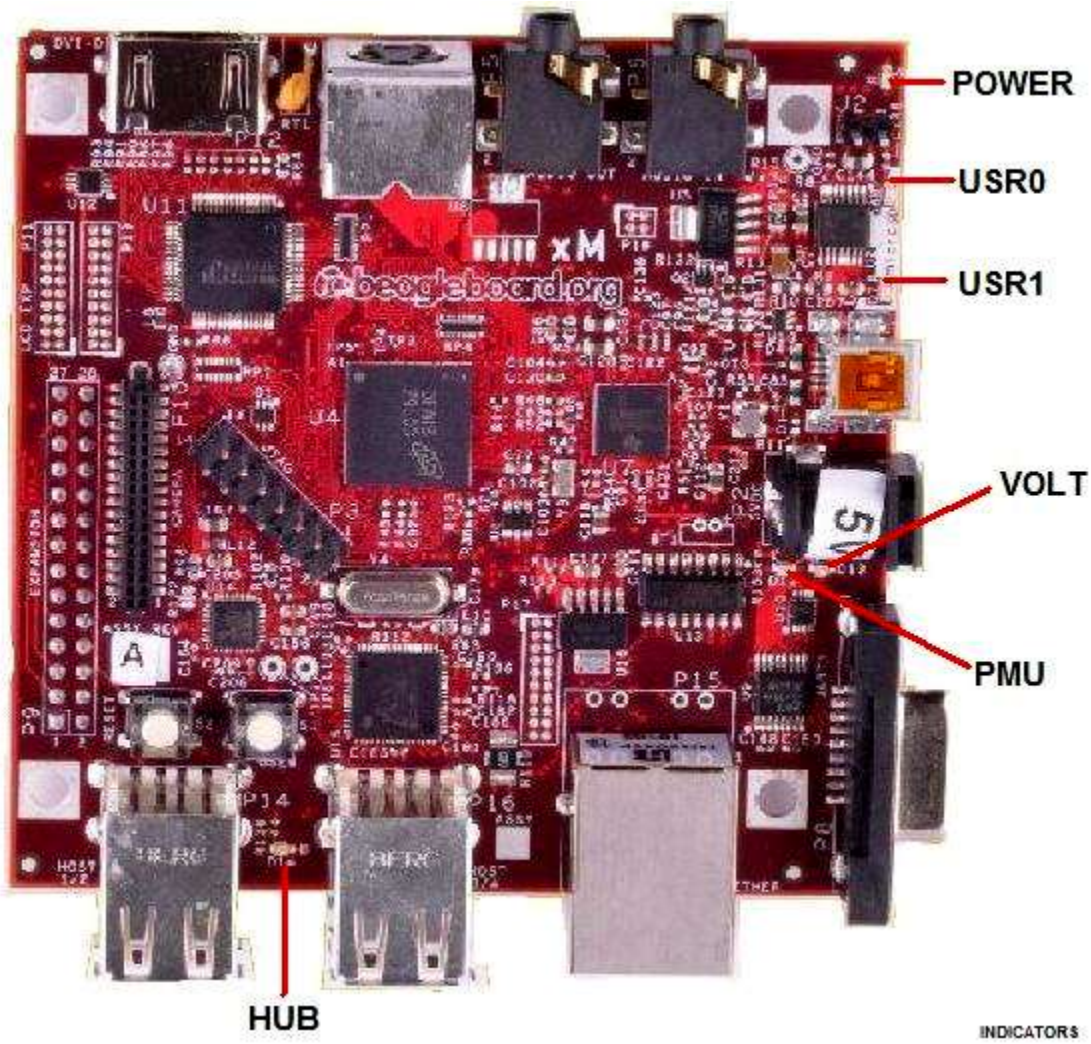



**Figure 14. BeagleBoard Indicator Locations**

**POWER** indicates that power is applied to the board.
**USR0/1** can be used by the SW as needed
**PMU** is controlled from the power management chip and can be connected to a PWM.
**VOLT** will turn on when the DC voltage exceeds specification
**HUB** turns on when power is applied to the USB HUB.

### 6.11 Button Locations

There are two buttons on the BeagleBoard-xM; the **RESET** button when pressed will force a board reset and the **USER** button which can be used by the SW for user interaction. **Figure 15** shows the location of the buttons.

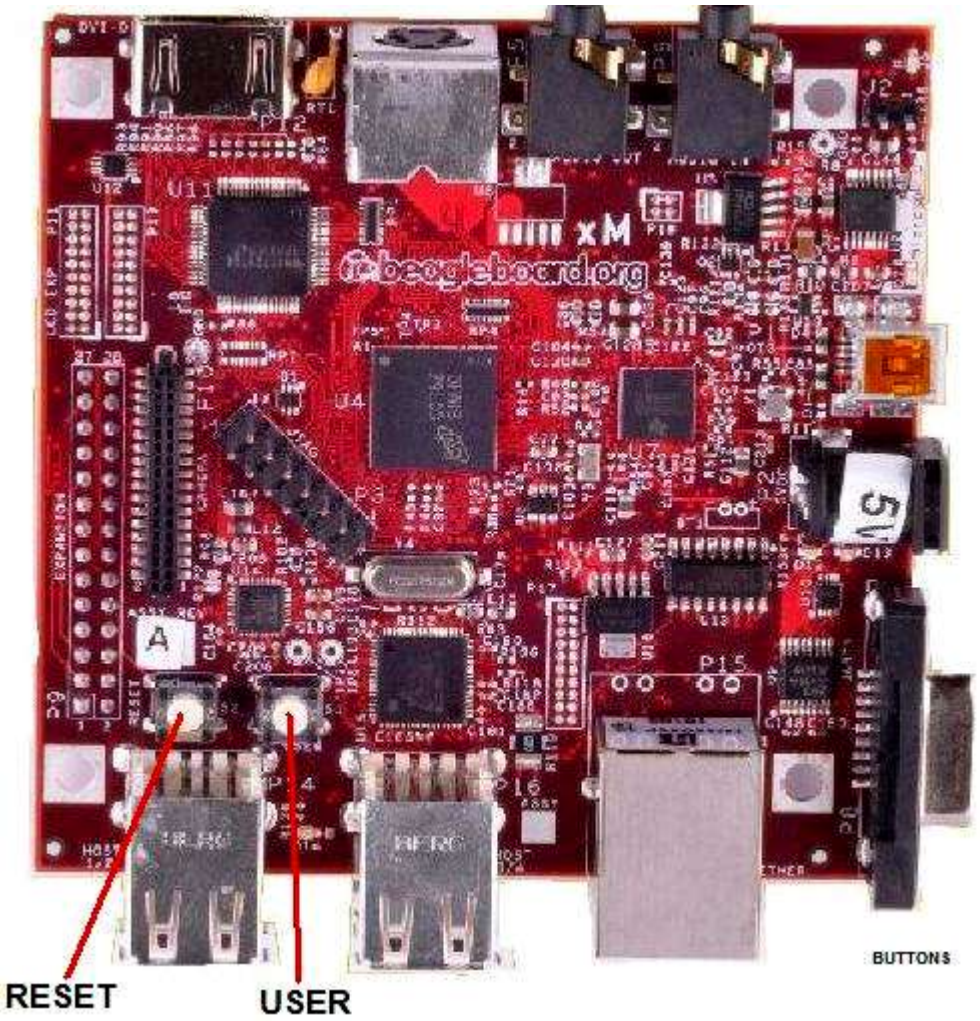



**Figure 15. BeagleBoard Button Location**

The User button does no affect the boot source of the board as is the case on the BeagleBoard version. If you do press the User Button on power up, the board will not boot.

### 6.12 microSD Connection

The microSD is the boot source for the board. It uses a push-push connector for the insertion and removal of the microSD card. The connector is mounted on the bottom side of the board. **Figure 16** shows the location of the microSD connector.

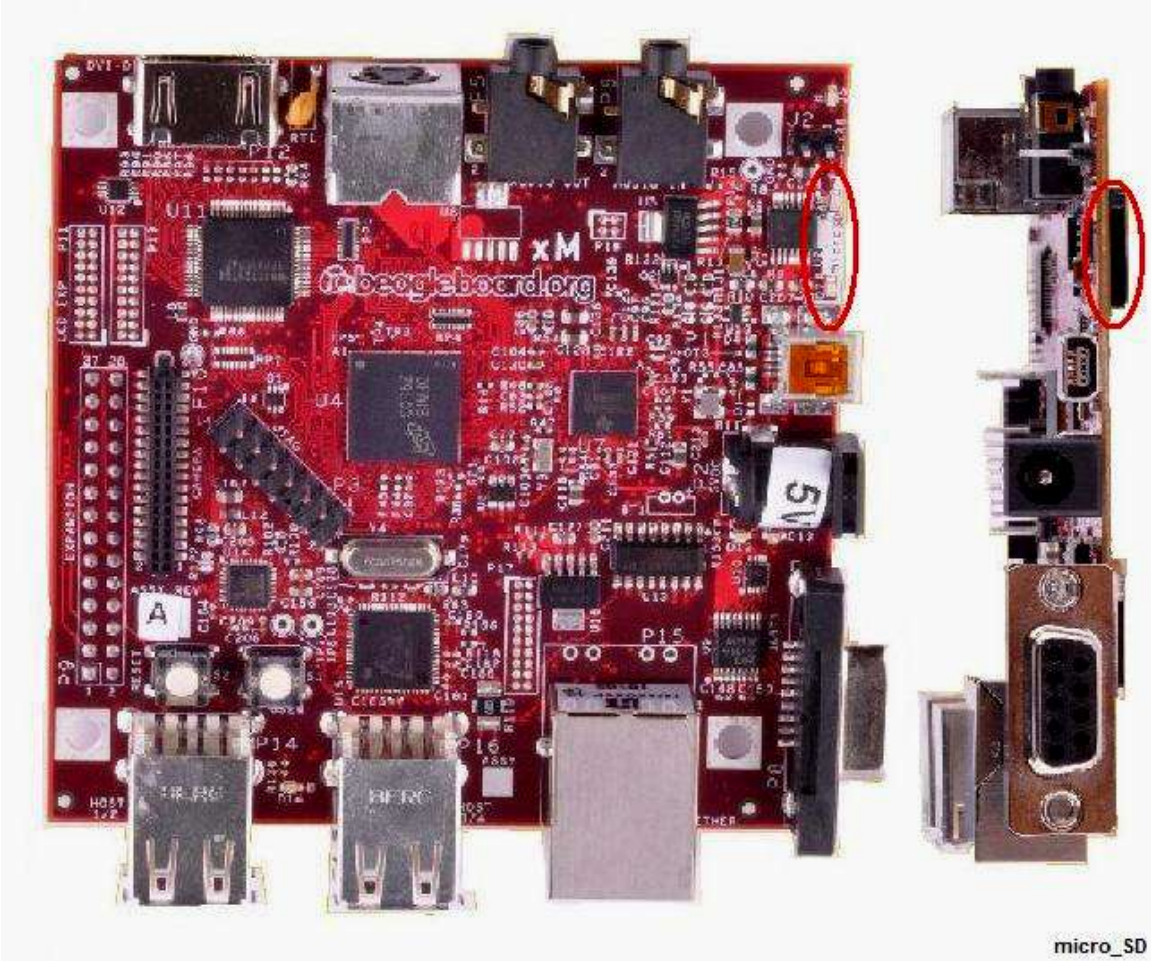



**Figure 16. BeagleBoard microSD Card Location**

The microSD card should be inserted with the writing on the card facing up. The white silkscreen area on top of the board works as a guide to align the card for insertion.

### 6.13 LCD Connection

There are two headers provided to access the LCD signals on the BeagleBoard-xM. These headers are 2x10 headers with a spacing of .05 (1.27mm) pitch. How these connectors are used is determined by the design of the adapter board that is connected to them. **Figure 17** shows the location of the LCD headers on the board.

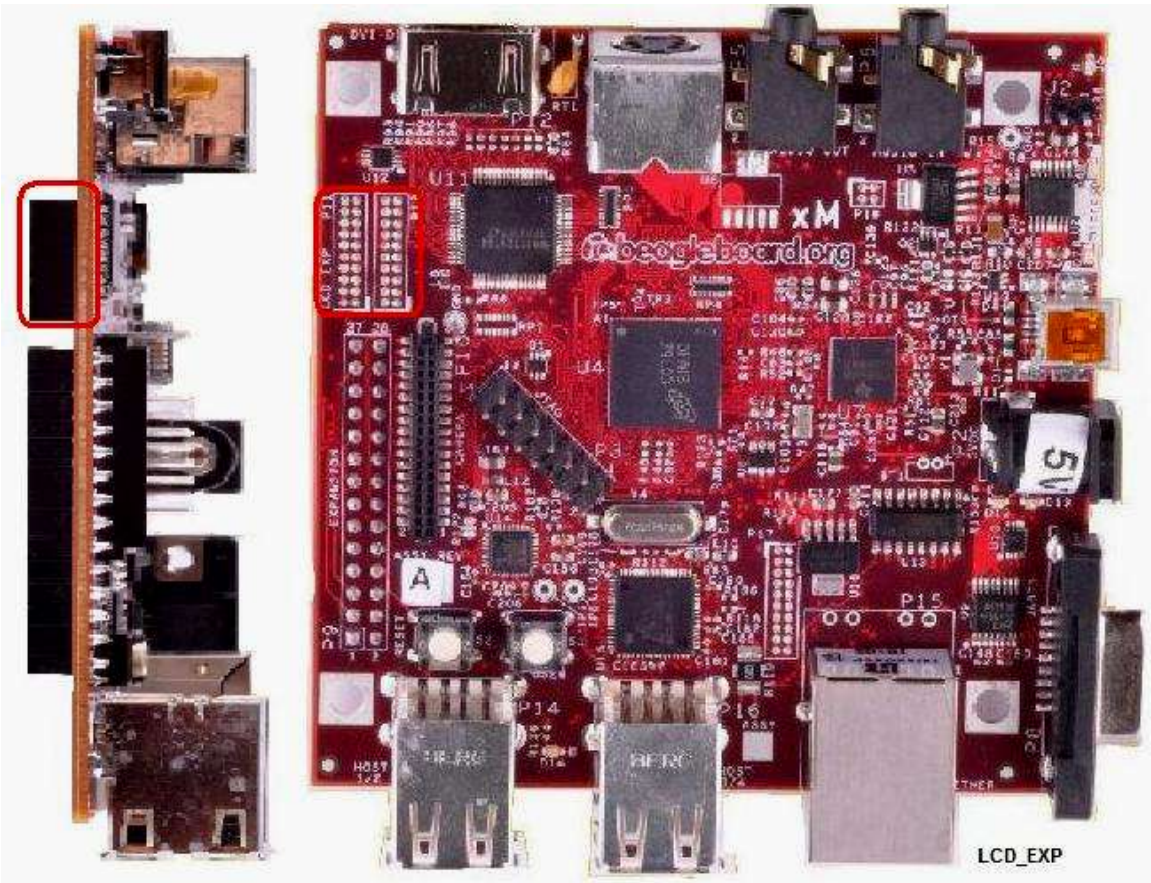



**Figure 17. BeagleBoard LCD Header Location**

Adapter boards are becoming available for such things as LCD panels and VGA adapters. As different LCD panels have different requirements, it is difficult to design an interface that will work with all LCD panels. That is the reason only the raw signals are brought out on these headers.

# 7.0 BeagleBoard-xM System Architecture and Design

This section provides a high level description of the design of the BeagleBoard-xM and its overall architecture.

## 7.1 System Block Diagram

**Figure 18** is the high level block diagram of the BeagleBoard-xM.

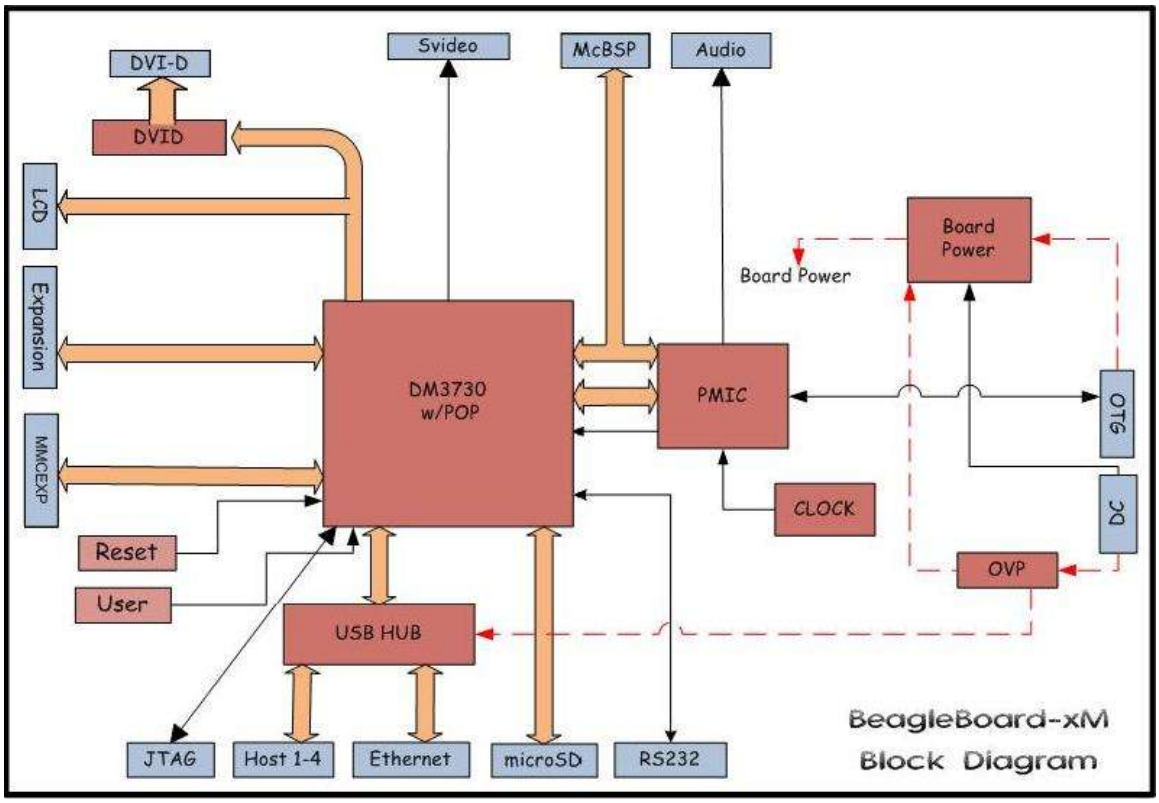



**Figure 18. BeagleBoard-xM High Level Block Diagram**

**Figure 19** shows the location of the key components on the board.

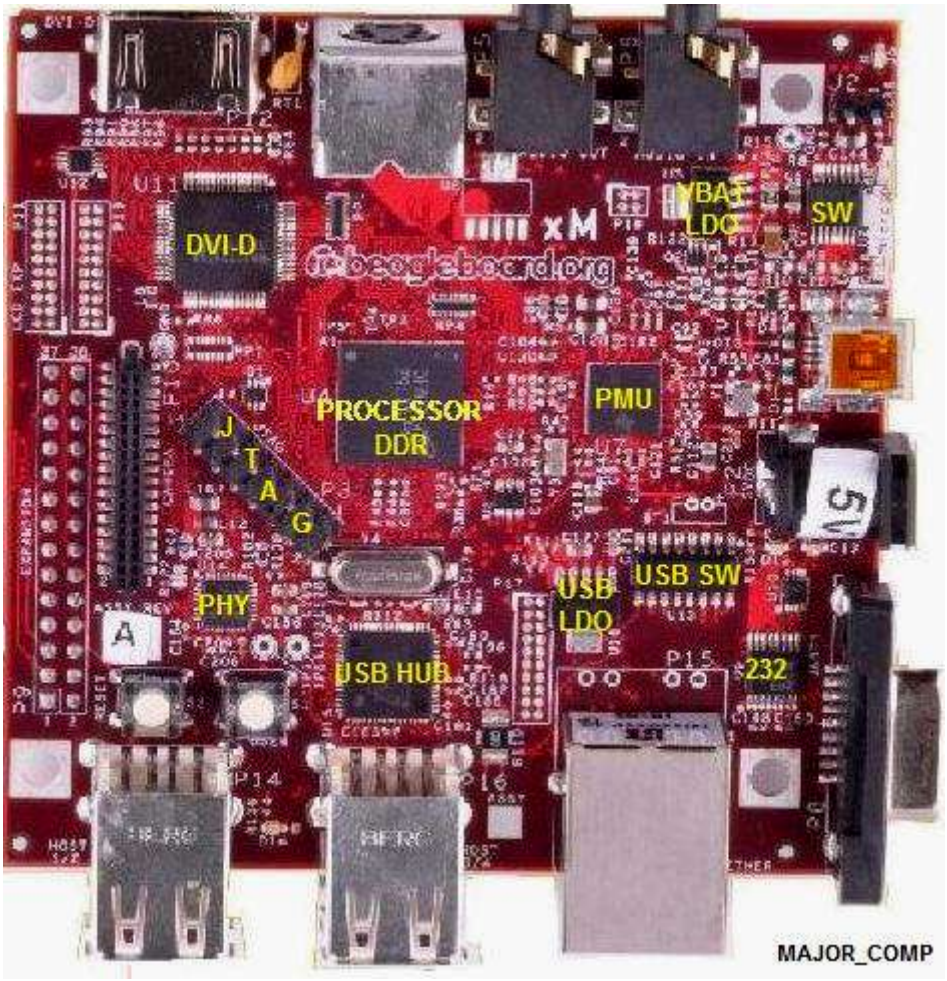



**Figure 19. BeagleBoard Major Components**

The information found in the remainder of this section describes in detail the architecture and design of the BeagleBoard-xM.

You will notice certain things in this section.

- The schematic has been created for each section showing only the pertinent components and their connections.
- The pin names differ from the actual schematic. For ease of reading, the names have been truncated to only show the specific functions of that pin as used in the design.

## 7.2 Over Voltage Protection

A new feature found on the BeagleBoard–xM board is the overvoltage protection circuit. The design of this circuit has been changed on the Rev C version of the board and is much simpler and more affective. The primary function of this circuit it to prevent voltage levels in excess of the specification from reaching other circuitry on the board and causing damage to the board. **Figure 20** is the diagram of the circuitry design.

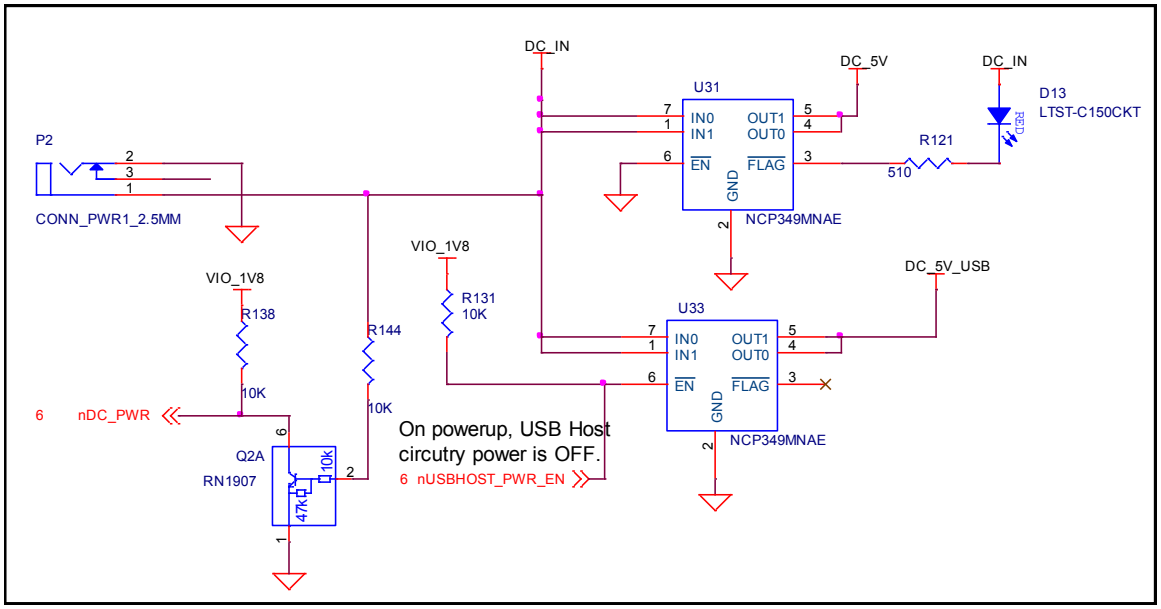



**Figure 20. Overvoltage Protection**

These functions are controlled by the **NCP349** device. The **NCP349** provides overvoltage protection for positive voltage, up to 28V. A low NMOSFET protects the systems connected on the OUT0/1 pins against positive overvoltage. At power up, with *EN* pin = low, the output is delayed before it is turned on to insure that the voltage is not in excess of 5.8V. The **NCP349** provides a *FLAG* output, which alerts the system that a fault has occurred by turning on **D13**, a red LED. The board will not power up if the voltage is in excess of the 5.8V max level.

Also new in the REV C is the fact that the USB 5V defaults to off, making sure that the voltage is not connected to the USB power FET. We were seeing a small number of boards that still had this device sustaining damage. This was the reason for the circuit design change. Having this default to off provides an additional level of protection.

New to the Rev C as well, is the ability to detect when the board is DC powered by reading the **nDC_PWR** signal. This is useful to allow the SW to determine that if in the OTG power mode, that the USB Host ports are not available.

Also new for the Rev C is the ability to power the HUB for the USB OTG port. As **U31** is always on, connecting power via the OTG port provided 5V to the **DC_5V** rail which

in turn will supply power to the DC in rail which can then be used to power the HUB as long as **U33** is enabled.

### 7.3 Power Conditioning

There are two possible sources of the 5V required by the BeagleBoard. It can come from the USB OTG port connected to a PC or a 5V DC supply. The USB supply is sufficient to power the BeagleBoard in most as long as you understand that the USB Host ports will not function. It is recommended that a DC supply be used.

It should also be noted that if an OTG configuration is used, for example tying two BeagleBoards together via a UBS OTG cable, both of the BeagleBoards must be powered by the DC supply. If the OTG port is used as a Host port, then the DC supply must also be used. **Figure 21** is the design of the main power input section.

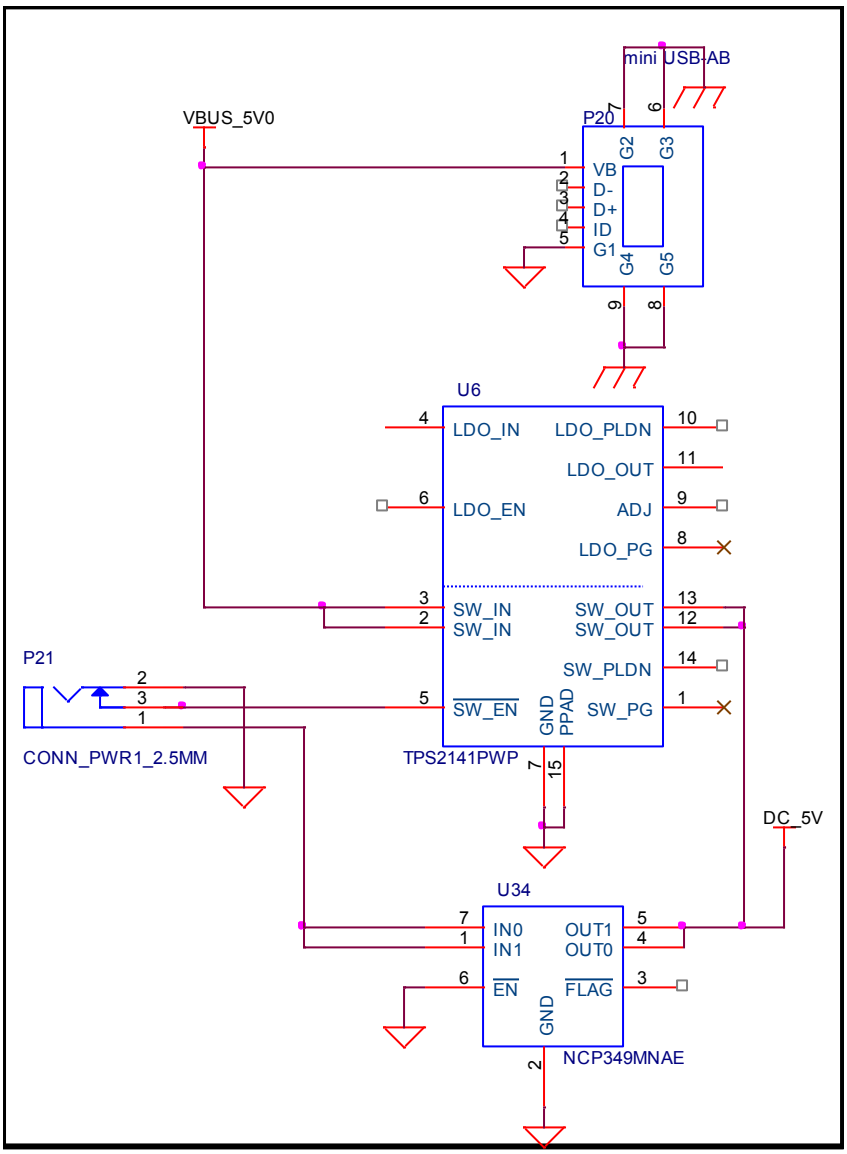



**Figure 21. Input Power Section**

### 7.3.1 USB DC Source

The USB specification requires that the current consumed prior to enumeration be limited to 100mA @ 5V (500mW). The 5V DC from the USB is routed through the **TPS2141** switch to insure that this requirement is met as uncharged capacitors on the BeagleBoard can exhibit a large current drain during start up that could exceed this requirement. The **TPS2141** is a USB 2.0 Specification-compatible IC containing a dual-current limiting power switch and an adjustable low dropout regulator (LDO). Both the switch and LDO limit inrush current by controlling the turn on slew rate. The dual-current-limiting feature of the switch allows USB peripherals to utilize high-value capacitance at the output of the switch, while keeping the inrush current low.

During turn on, the switch limits the current delivered to the capacitive load to less than 100 mA. When the output voltage from the switch reaches about 93% of the input voltage, the switch current limit increases to 800mA (minimum), at which point higher current loads can be turned on. The higher current limit provides short circuit protection while allowing the peripheral to draw maximum current from the USB bus.

When in the USB powered mode and no DC supply is connected, the **TPS2141** is enabled, allowing the power to be supplied to the board from the OTG port through the integrated switch inside the **TPS2141**.

### 7.3.2 Wall Supply Source

A wall supply can be used to provide power to the board. A regulated 5V DC supply of at least 2A is required and a rating of 3A is preferred, assuming that the USB ports and expansion headers are likely to be used. It needs to have a 2.1mm plug with a center hot configuration. If you are using the USB HUB or Ethernet interface, additional current is required. In the event that a higher DC load is required due to the addition of a Daughtercard or if all the USB host ports need to supply the full 500mA per port, a higher current supply can be used. The maximum current should not exceed 3A.

### 7.3.3 DC Source Control

Unlike when powering from the USB OTG port, in the case of the DC voltage, the current limiting is not required. As long as the DC supply is not connected, the switch for the USB is enabled. When the DC supply is plugged in, the switch is disabled because the ground is removed from **pin 5** of the **TPS2141**. This insures that the 5V from the USB is not connected by disabling the internal FET. In the case where there is no USB plugged in, there is no 5V available to be routed so the removal of the pullup in **pin 5** has no affect.

When in the DC mode of operation, the USB OTG can be used in the Host or Client modes. The **TPS65950** will be responsible for handling the supply of the **VBUS_5V0** rail in the OTG or Host modes. As this is limited to 100mA, a powered hub must be used to support peripherals on the OTG port.

It is possible to provide 5V via the expansion connectors as would be the case from a daughter card to prevent you from having to have two DC supplies. You should be careful in doing this. If you plan to use the USB OTG port, you will need to place an unconnected connector into the DC power jack to insure that the DC from the OTG port is not shorted to the 5V supplied via the expansion connector. There is a signal called **nUSB_PWR** which if a logic level "1" (5V) indicates that there is 5V supplied by the USB OTG port, it is plugged in, and the DC dummy jack is installed. This condition could be used on the daughtercard to know that it is OK to supply power onto the expansion bus to power the board. If this signal is low, then that indicates that there is no

DC power connected and there is no USB OTG port connected. For this reason, is recommended however, that a large pullup be provided on the daughtercard to make the signal a logic level "1" (5V) to detect the true state of the DC jack. It is always possible that at any point a USBOTG cable could be installed. This means that in order to power the board from the expansion headers, the DC dummy jack must be installed and there is a method to verify that condition.

### 7.3.4 AUX 3.3V Supply

The **TPS2141** has an integrated 3.3V LDO which is being used to supply the **3.3V** as required on the BeagleBoard for the **DVI-D** interface and the **UART**. The input to the LDO is supplied by the main **DC_5V**. This insures that the power to the LDO can be supplied by either the USB or the DC wall supply and that the current measurement includes the 3.3V supply. The 3.3V supply can be turned off by activating GPIO1 on the T**PS65950** to a 1. By default the voltage is on. You will also see that the 3.3V supply powers the power LED, **D5.** If during a low power mode, the user chooses to turn of the power LED, this GPIO pin can be used to turn off the power LED. It should also be noted, that the 3.3V rail controls the serial port power, so this will be powered down as well. **Figure 22** is the AUX 3.3V Supply design.

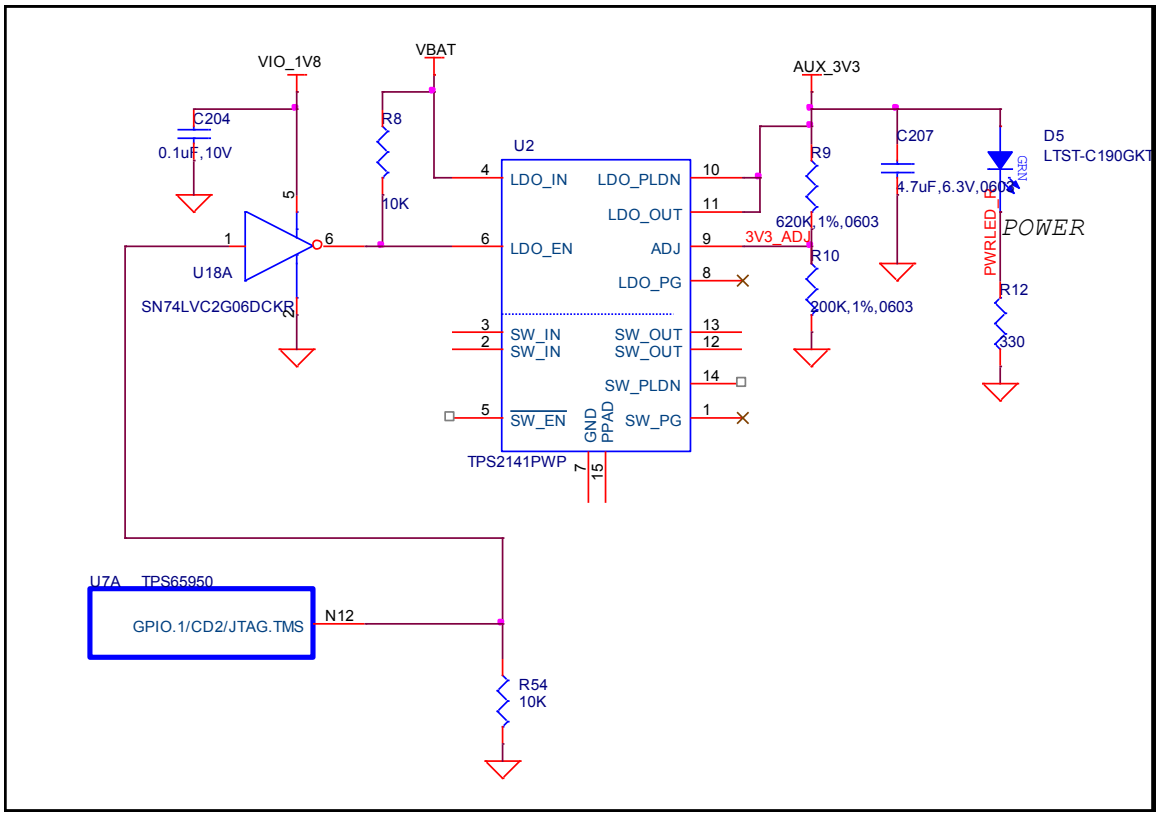



**Figure 22. AUX 3.3 Power Section**

## 7.4 Meter Current Measurement

Jumper **J2** is a header that allows for the voltage drop across the resistor to be measured using a meter, providing a way to measure the current consumption of the BeagleBoard from the main voltage rails, either USB or DC. The resistor, **R13**, is a .1 ohm resistor across which the voltage is measured. The reading you get is .1mV per mA of current. You will need to make sure you have a sensitive meter to make your measurements. Please keep in mind, that this current reading does not include any current consumed by the USB HUB, USB ports, or the Expansion headers.

## 7.5 Processor Current Measurement

The resistor across **J2** can also be used to measure the current of the board by reading the voltage drop across **R13** from software. There are two pairs of resistors provided on the **TPS65950** that measure the voltage on either side of **R13**. This is done via the I2C control bus to the **TPS65950** from the processor. These values along with resistance of **R**13 are used to calculate the current consumption of the board. **Figure 24** is the schematic of the measurement circuitry. The maximum value that can be input to the ADC inputs is based on the setting of the **VINTANA2.OUT** voltage rail which defaults to 2.5V. In order to prevent the voltage levels from exceeding this value a pair of resistors of **12K** and **10K** is used to scale the voltage down.

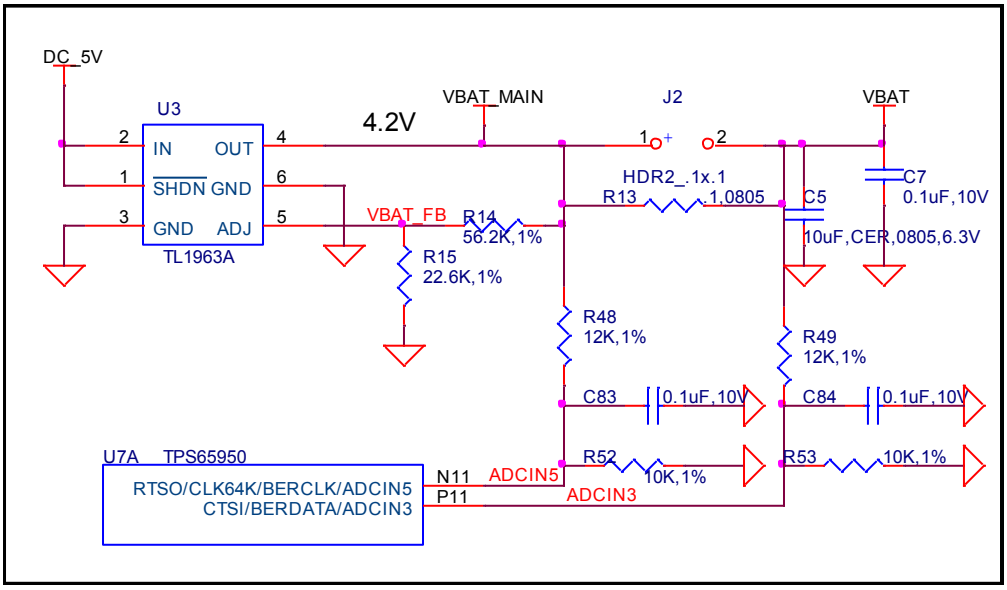



**Figure 23. Processor Current Measurement**

This results in a value that is 46% of the actual value. So, for a maximum value of 5.25V, the voltage read would be 2.415V which keeps it below the 2.5V point. The voltage drop across **R13** will be small as the value of the resistor is 0.1 ohms. For every 100 mA of

current a voltage of .01V will be detected. In order to determine the actual power, the input voltage and the voltage drop must be measured.

## 7.6 VBAT Power Conditioning

This circuitry regulates the DC input to a nominal 4.2VDC level. This is required in order to meet the maximum DC voltage level as specified by the **TPS65950** Power Management device which is 4.7V. Using 4.2V gives us some margin and meets the nominal 4.2V rating of the **TPS65950**.

**Figure 25** is the power conditioning section of the BeagleBoard.

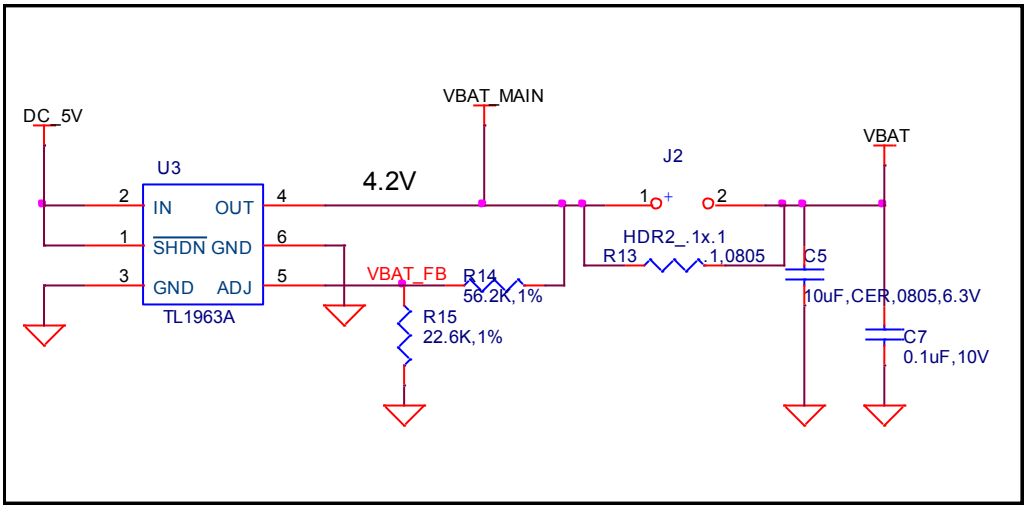



**Figure 24. VBAT Power Conditioning**

The **TPS65950** provides the main power rails to the board and has a maximum limit of 4.7V on its VBAT input and a nominal of 4.2V. **U3**, the **TL1963A**, is used to convert the DC_5V, which can come from a DC wall supply or the USB, to 4.2V to meet this requirement. The **TL1963A** is a linear low-dropout (LDO) voltage regulator and is thermal shutdown and current limit protected. It has the ability to deliver 1A of current, although this is far and above the requirements of the board. By adjusting the values of **R14** and **R15**, the actual voltage can be adjusted if needed.

## 7.7 TPS65950 Reset and Power Management

The **TPS65950** supplies several key functions on the BeagleBoard. This section covers a portion of those functions centered on the power and reset functions. Included in this section are:

- Main Core Voltages
- Peripheral Voltages
- Power Sequencing
- Reset

- Current measurement via SW

The other functions are covered in other sections in this document and are grouped by their overall board functions. The explanation of the various regulators found on the **TPS65950** is based upon how they are used in the board design and are not intended to reflect the overall capability of the **TPS6595**0 device. Please refer to the **TPS65950** documents for a full explanation of the device operation.

### 7.7.1 Main Core Voltages

The **TPS65950** supplies the three main voltage rails for the processor and the board:

- VDD1 (1.2V, adjustable)
- VDD2 (1.3V)
- VIO_1V8 (1.8V)

The **VOCORE_1V3** defaults to **1.2V** at power up, but can be adjusted by software to the **1.3V** level. **Figure 26** is the interfacing of the **TPS65950** to the system as it provides the three main rails.

### 7.7.2 Main DC Input

The main supply to the **TPS65950** for the main rails is the **VBAT** rail which is a nominal 4.2V. Each rail has a filter cap of **10uF** connected to each of the three inputs. A **.1uF** cap is also provided for high frequency noise filtering.

### 7.7.3 Processor I2C Control

The various components in the **TPS65950** are controlled from the processor via the I2C interface. I2C_0 is used to control the **TPS65950** device.

### 7.7.4 VIO_1V8

The **VIO_1V8** rail is generated by the **TPS65950 VIO** regulator. The **VIO** output is a stepdown converter with a choice of two output voltage settings: 1.8 V or 1.85 V. The voltage is set by configuring the VSEL bit (VIO_VSEL[0]). When the VSEL bit is set to 0, the output voltage is 1.8 V, and when it is set to 1, the output voltage is 1.85 V.

When the **TPS65950** resets, the default value of this LDO is 1.80 V; the processor must write 1 to the VSEL field to change the output to 1.85 V. The default for the BeagleBoard is 1.8V. This regulator output is used to supply power to the system memories and I/O ports. It is one of the first power supplies to be switched on in the power-up sequence. VIO does not support the SmartReflex voltage control schemes. VIO can be put into sleep or off mode by configuring the SLEEP_STATE and OFF_STATE fields of the VIO_REMAP register.

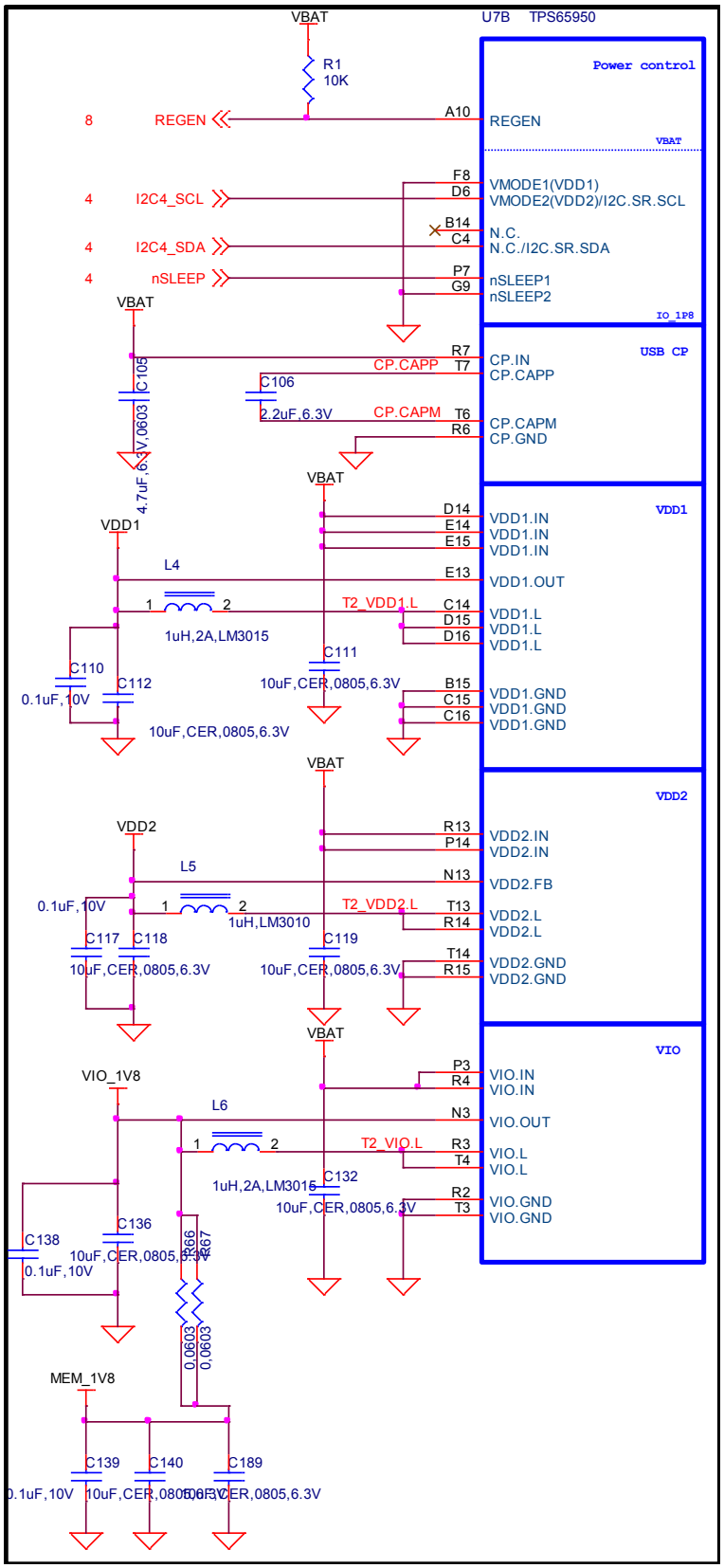



**Figure 25. Main Power Rails**

### 7.7.5 Main Core Voltages Smart Reflex

**VDD1** and **VDD2** regulators on the **TPS65950** provide SmartReflex-compliant voltage management. The SmartReflex controller in the processor interfaces with the **TPS65950** counterpart through the use of a dedicated **I2C** bus. The processor computes the required voltage and informs the **TPS65950** using the SmartReflex I2C interface.

SmartReflex control of the **VDD1** and **VDD**2 regulators can be enabled by setting the SMARTREFLEX_ENABLE bit (DCDC_GLOBAL_CFG[3]) to 1. To perform **VDD1** voltage control through the SmartReflex interface, the TPS65950 provides the VDD1_SR_CONTROL register. The MODE field of the VDD1_SR_CONTROL register can be set to 0 to put VDD1 in an ACTIVE state; setting the field to 1 moves **VDD1** to a SLEEP state. **VDD1** output voltage can be programmed by setting the VSEL field of the VDD1_SR_ CONTROL register. The **VDD1** output voltage is given by VSEL*12.5 mV + 600 mV.

### 7.7.6 VDD1

The **VDD1** rail is supplied by the **VDD1** regulator of the **TPS65950**. The **VDD1** regulator is a 1.1A stepdown power converter with configurable output voltage between 0.6 V and 1.45 V in steps of 12.5 mV. This regulator is used to power the processor core.

The processor can request the **TPS65950** to scale the **VDD1** output voltage to reduce power consumption. The default output voltage at power-up depends on the boot mode settings, which in the case of the BeagleBoard is 1.2V. The output voltage of the **VDD1** regulator can be scaled by software or hardware by setting the ENABLE_VMODE bit (VDD1_VMODE_CFG[0]). In each of these modes, the output voltage ramp can be single-step or multiple-step, depending on the value of the STEP_REG field of the VDD1_STEP[4:0] register. The VOCORE_1V3 rail should be set to 1.3V after boot up.

Apart from these modes, the **VDD1** output voltage can also be controlled by the processor through the SmartReflex I2C interface between the DM3730 and the **TPS65950**. The default voltage scaling method selected at reset is a software-controlled mode. Regardless of the mode used, **VDD1** can be configured to the same output voltage in sleep mode as in active mode by programming the DCDC_SLP bit of the VDD1_VMODE_CFG[2] register to 0. When the DCDC_SLP bit is 1, the sleep mode output voltage of **VDD1** equals the floor voltage that corresponds to the VFLOOR field (VDD1_VFLOOR[6:0]).

### 7.7.7 VDD2

The **VDD2** voltage rail is generated by the **TPS65950** using the **VDD2** regulator. The **VDD2** regulator is a stepdown converter with a configurable output voltage of between

0.6 V and 1.45 V and is used to power the processor core. **VDD2** differs from **VDD1** in its current load capabilities with an output current rating of 600 mA in active mode.

The **VDD2** provides different voltage regulation schemes. When **VDD2** is controlled by the VMODE2 signal or with the SmartReflex interface, the range of output voltage is 0.6 V to 1.45 V. The use of the VMODE2 signal and the VDD2_VMODE_CFG, VDD2_STEP, VDD2_FLOOR, and VDD2_ROOF registers is similar to the use of the corresponding signals and registers for **VDD1**. **VDD2** shares the same SmartReflex I2C bus to provide voltage regulation. The VDD2_SR_CONTROL register is provided for controlling the **VDD2** output voltage in SmartReflex mode.

When the **VDD2** is used in software-control mode, the VSEL (VDD2_ DEDICATED[4:0]) field can be programmed to provide output voltages of between 0.6 V and 1.45 V. The output voltage for a given value of the VSEL field is given by VSEL*12.5 mV + 600 mV. If the VSEL field is programmed so that the output voltage computes to more than 1.45 V, the TPS65950 sets the **VDD2** output voltage to 1.5 V.

## 7.8 Peripheral Voltages

There are 10 additional voltages used by the system that are generated by the **TPS65950**. These are:

- VDD_PLL2
- VDD_PLL1
- VDAC_1V8
- VDD_SIM
- VMMC2
- VDD_VMMC1
- CAM_2V8
- CAM_1V8
- USB_1V8
- EXP_VDD

**Figure 27** shows the peripheral voltages supplied by the **TPS65950**.

### 7.8.1 VDD_PLL2

This programmable LDO is used to power the processor PLL circuitry. The **VPLL2** LDO can be configured through the I2C interface to provide output voltage levels of 1.0 V, 1.2 V, 1.3 V, or 1.8 V, based on the value of the VSEL field (VPLLI_DEDICATED[3:0]). On the board this rail is used to power DVI output for pins DSS_DATA(0:5), DSS_DATA(10:15) and DSS_DATA(22:23). The VPLL2 must be set to 1.8V for proper operation of the **DVI-D** interface.

### 7.8.2 VDD_PLL1

The VPLL1 programmable LDO regulator is low-noise, linear regulator used for the processor PLL supply. The VDD_PLL1 rail is initialized to 1.8V.

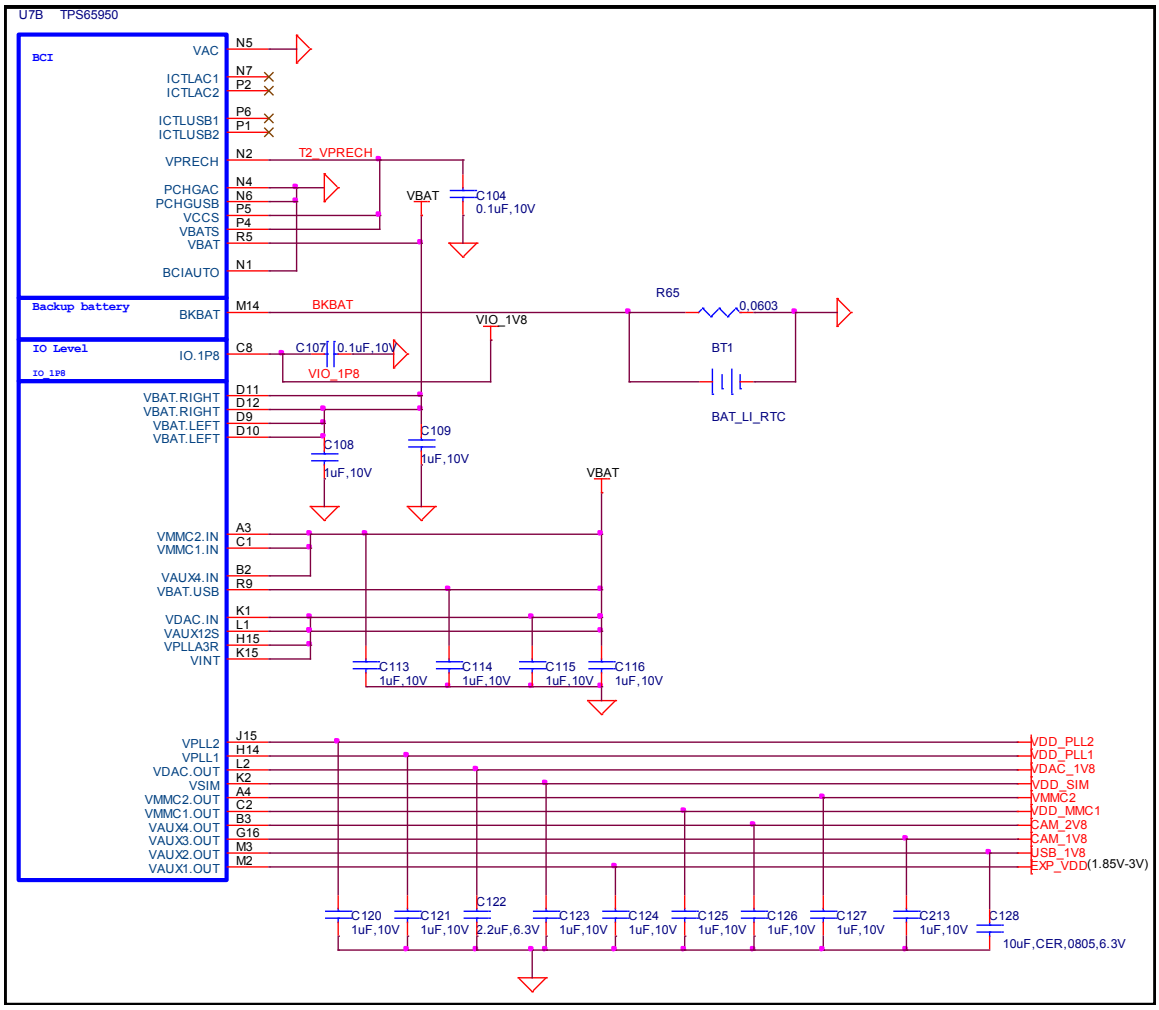



**Figure 26. Peripheral Voltages**

### 7.8.3 VDAC_1V8

The **VDAC** programmable LDO regulator is a high-PSRR, low-noise, linear regulator that powers the PROCESSOR dual-video DAC. It is controllable with registers via I2C and can be powered down if needed. The **VDAC** LDO can be configured to provide 1.2V, 1.3 V, or 1.8 V in on power mode, based on the value of the VSEL field (VDAC_DEDICATED[3:0]). The **VDAC_1V8** rail should be set to 1.8V for the BeagleBoard.

### 7.8.4 VDD_SIM

This voltage regulator is a programmable, low dropout, linear voltage regulator supplying the bottom 4 bits of the 8 bit **SD/MMC** card slot. The VSEL field (VSIM_DEDICATED[3:0]) can be programmed to provide output voltage of 1.0 V, 1.2 V, 1.3 V, 1.8 V, 2.8 V, or 3.0 V and can deliver up to 50mA. The default output voltage of this LDO as directed by the **TPS65950** boot pins is 1.8V.

### 7.8.5 VMMC2

The VMMC2 rail uses the **VMMC2.OUT** rail from the TP65950. VMMC2 is adjustable from 1.85 to 3.15V and can deliver up to 100mA of current. VMMC2 is provided as an auxiliary voltage rail on **P17**, the Auxiliary Access Header. The proper setting of this rail is determined by the application and the HW supplied that connects to P17.

### 7.8.6 VDD_VMMC1

The **VMMC1** LDO regulator is a programmable linear voltage converter that powers the MMC1 slot and includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected. The VMMC1 LDO is powered from the main **VBAT** rail. The **VMMC1** rail defaults to 3.0V as directed by the **TPS65950** boot pins and will deliver up to 220mA. It can be set to 3.0V in the event 3V cards are being used.

### 7.8.7 CAM_2V8

This rail powers the optional camera module and uses the **VAUX4.OUT** rail from the **TPS65950**. VAUX4 is adjustable from .7 to 2.8V and can deliver up to 200mA of power. This railed should be set to 1.8V for proper operation of the camera module. See the camera module section for more information.

### 7.8.8 CAM_1V8

This rail powers the optional camera module and uses the **VAUX3.OUT** rail from the **TPS65950**. VAUX4 is adjustable from 1.5 to 2.8V and can deliver up to 100mA of power. This railed should be set to 1.8V for proper operation of the camera module. See the camera module section for more information.

### 7.8.9 USB_1V8

The **VAUX2** LDO regulator is a programmable linear voltage converter that powers the 1.8V I/O rail of the USB PHY and includes a discharge resistor and overcurrent protection (short-circuit). The **VAUX2 LDO** is powered from the main **VBAT** rail. The **VAUX2** rail defaults to off as directed by the **TPS65950** boot pins and will deliver up to 100mA. The voltage rail is labeled **VDD_EHCI** on the schematic.

#### 7.8.10 EXP_VDD

The **EXP_VDD** rail uses the **VAUX1.OUT** rail from the **TP65950**. **EXP_VDD** is adjustable from 2.5 to 3.0V and can deliver up to 200mA of current. **EXP_VDD** is provided as an auxiliary voltage rail on **P13**, the LCD Expansion Header. The proper setting of this rail is determined by the application and the HW supplied that connects to P13.

### 7.9 Other Signals

This section describes other signals in the design that have not been categorized.

#### 7.9.1 Boot Configuration

The boot configuration pins on the **TPS65950** determine the power sequence of the device. In order to support the processor on the board with the correct power configuration, the boot pin configuration is fixed at:

- **BOOT0** tied to VBAT
- **BOOT1** tied to Ground.

#### 7.9.2 RTC Backup Battery

An optional battery to backup for the Real Time Clock that is in the **TPS65950** is provided for in the design. The board does not come equipped with the battery. The battery can be purchased from DigiKey or other component suppliers. When the battery is not installed, **R65** must be installed. You must make sure that prior to installing the battery that **R65** is removed.

Refer to section **9.11** for information on the battery selection and installation.

### 7.9.3 Power Sequencing

Based on the boot configuration pins, the **TPS65950** knows the type of OMAP processor that it needs to support, in this case the processor. The voltages are ramped in a sequence that is compatible with the processor. **Figure 27** is the sequence in which the power rails, clocks, and reset signal come up.

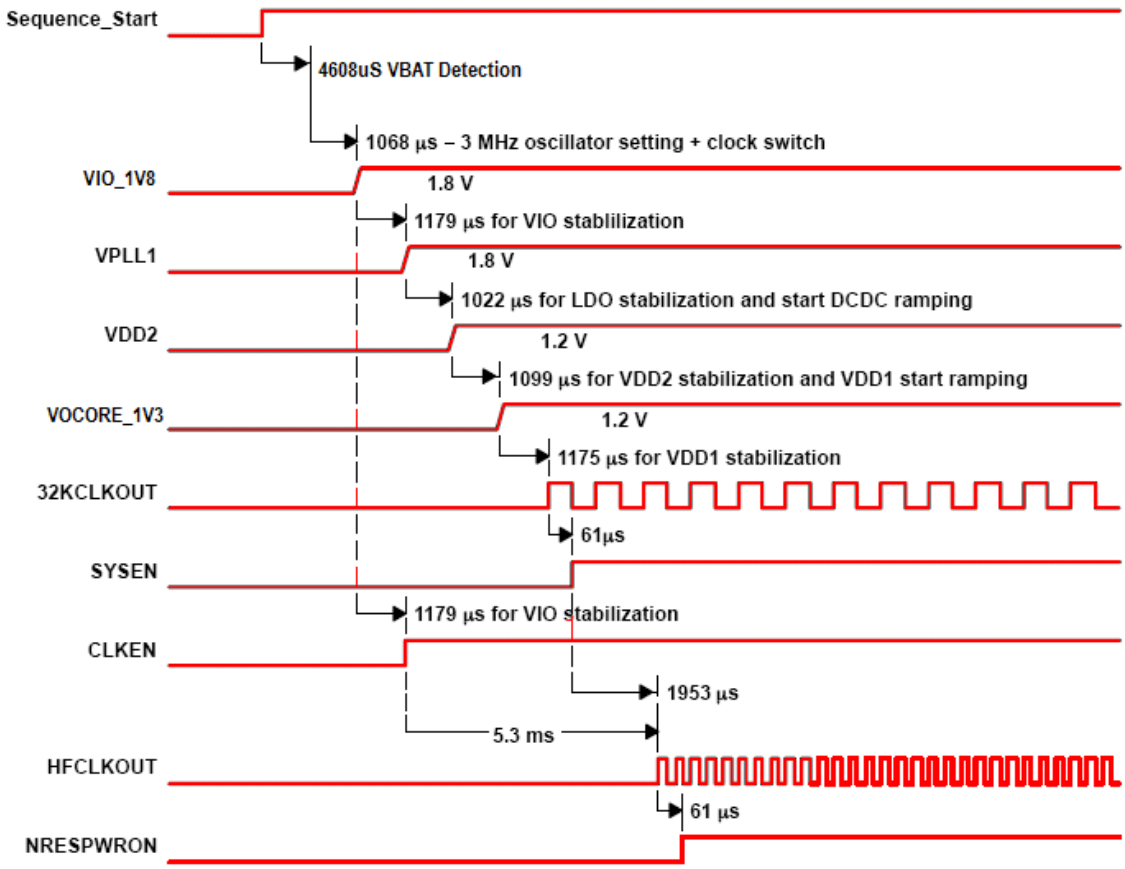



**Figure 27. Power Sequencing**

### 7.9.4 Reset Signals

The BeagleBoard uses three distinct reset circuits:

- Warm Reset
- Cold Reset
- User Reset

**Figure 28** shows the connections for the Reset interfaces.

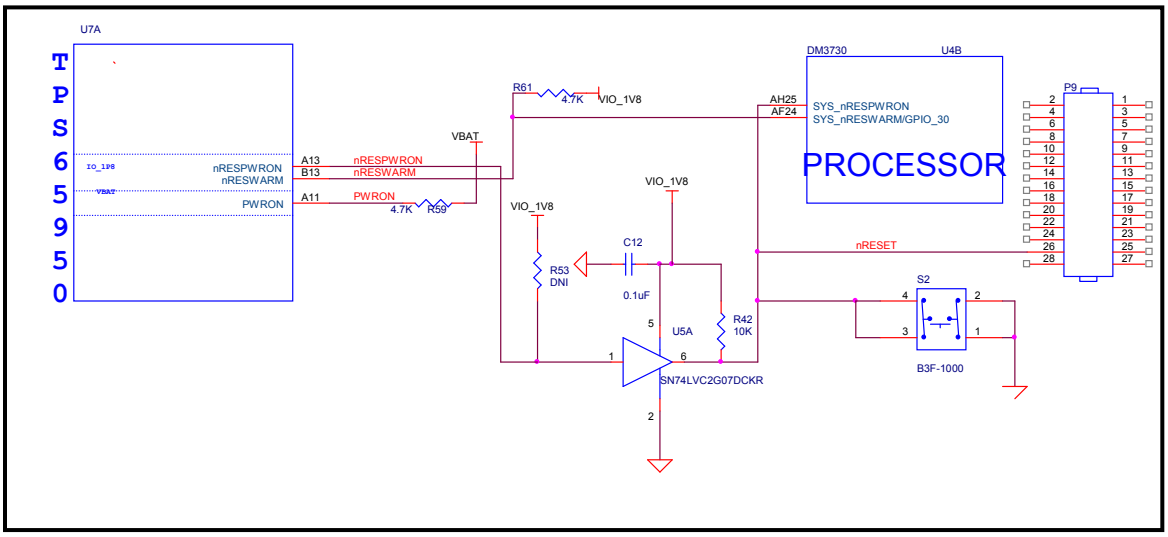



**Figure 28. Reset Circuitry**

#### *7.9.4.1 Warm Reset*

The warm reset is generated by the processor on power up. The **nRESWARM** signal is a bidirectional reset. When an internal reset occurs, **nRESWARM** goes low and resets all the peripherals and the **TPS65950**. The **TPS65950** can be configured to perform a warm reset of the device to bring it into a known defined state by detecting a request for a warm reset on the **NRESWARM** pin. The minimum duration of the pulse on the **nRESWARM** pin should be two 32-kHz clock cycles. The **nRESWARM** output is open-drain; consequently, an external pullup resistor is required. There is no way for the user to generate a warm reset on the BeagleBoard.

#### *7.9.4.2 Cold Reset*

On power up as shown in **Figure 27**, the **TPS65950** generates **nRESPWRON**, power on reset. The signal from the **TPS65950** is an output only and is not an open drain signal. By running the signal through a buffer, **SN74LVC2G07**, the signal becomes open drain, which requires a pullup on the signal. This will allow the **nRESPWRON** signal to be pulled low, by pressing the reset switch **S2**, to force a reset to the **PROCESSOR** processor and to any device on the expansion card that require a reset.
It also allows for the reset signal to be pulled low or held low for an extended time by circuitry on the expansion card if needed.

#### *7.9.4.3 User Reset*

The USER RESET button can be used to request a Warm Reset from the processor. After initialization, this pin becomes an input to the processor. By pushing the Reset button, an interrupt is generated into the processor. The software that is run as a result of this can then do whatever housekeeping is required and then send the processor into a reset mode.

#### *7.9.4.4 PWRON*

You will notice another signal on the **TPS65950** called **PWRON**. This signal is referenced in the **TPS65950** documentation. In the BeagleBoard design it is not used but it is pulled high to insure the desired operation is maintained.

### 7.9.5 mSecure Signal

This signal provides for protection of the **RTC registers** in the **TPS65950** be disabling that function via a control signal from the processor.

For more information on the operation on the signal, please refer to the processor **Technical Reference Manual**.

## 7.10 Processor

The heart of BeagleBoard-xM is the DM3730 processor. **Figure 29** is a high level block diagram of the processor.

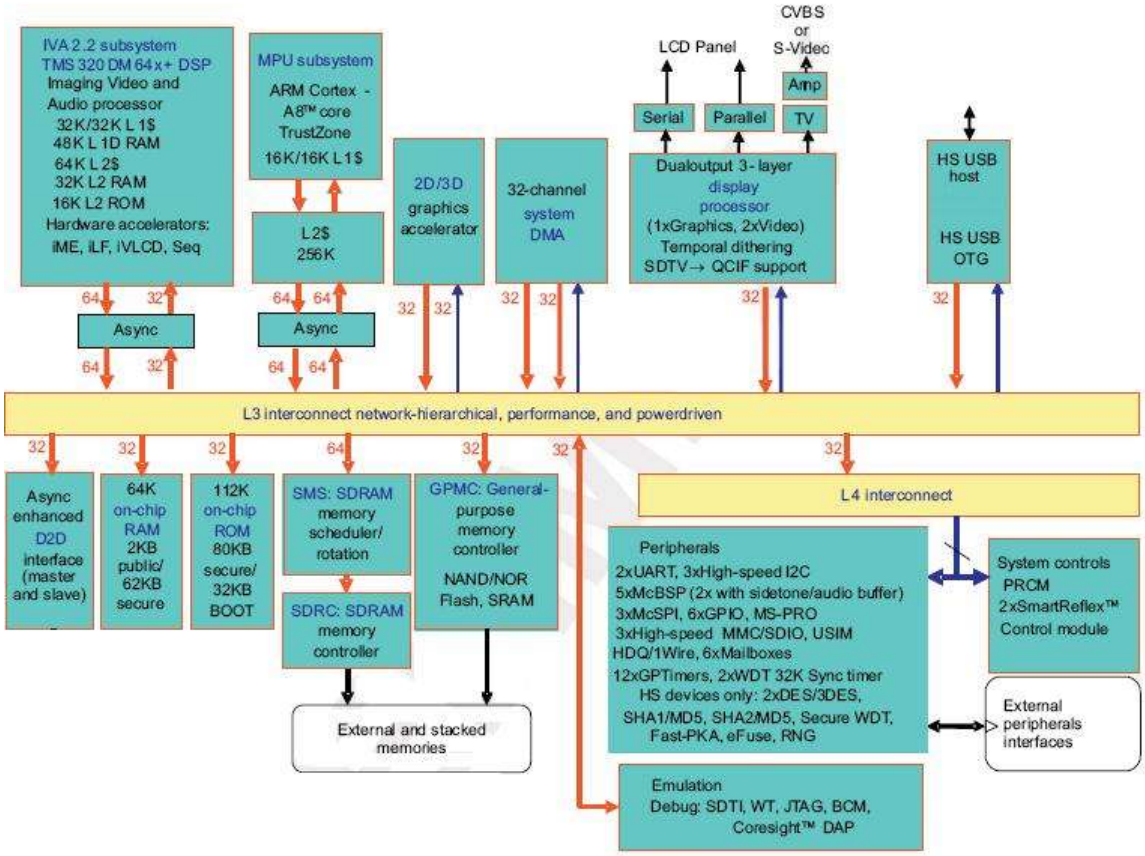



**Figure 29. DM37x Block Diagram**

### 7.10.1 Overview

The DM3730 is a high-performance, multimedia application device and is integrated onto TI's advanced 45-nm process technology. The processor architecture is configured with different sets of features in different tier devices. Some features are not available in the lower-tier devices. For more information, refer to the Technical Reference Manual (TRM).The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to various applications.

The processor supports high-level operating systems (OSs), such as:

- Windows CE
- Linux
- QNX
- Symbian
- Others

This processor device includes state-of-the-art power-management techniques required for high-performance low power products. The DM3730 supports the following functions and interfaces on the BeagleBoard:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8™ microprocessor
- POP Memory interface
  - 4Gb MDDR (512Mbytes)
- 24 Bit RGB Display interface (DSS)
- SD/MMC interface
- USB OTG interface
- NTSC/PAL/S-Video output
- Power management
- Serial interface
- $I^2C$ interface
- $I^2S$ Audio interface (McBSP2)
- Expansion McBSP1
- JTAG debugging interface

### 7.10.2 SDRAM Bus

The SDRAM bus is not accessible on the BeagleBoard. Its connectivity is limited to the POP memory access on the top of the processor and therefore is only accessible by the SDRAM memory. The base address for the DDR SDRAM in the POP device is **0x8000 0000**.

If you look at the –xM schematic, you will notice on page 3 there are a lot of signals labeled NA0…65. These pins are located on the bottom of the processor. In the Rev

BeagleBoard processor, these pins provided access to the SDRAM bus. However, in the case of the processor on the BeagleBoard–xM, these there are no signals on these pins.

### 7.10.3 GPMC Bus

The GPMC bus is not accessible on the BeagleBoard. Its connectivity is limited to the POP memory access on the top of the processor and therefore is only accessible by the NAND memory.

The memory on the GPMC bus is NAND and therefore will support the classical NAND interface. The address of the memory space is programmable.

### 7.10.4 DSS Bus

The display subsystem provides the logic to display a video frame from the memory frame buffer in SDRAM onto a liquid-crystal display (LCD) display via the DVI-D interface or to a standalone LCD panel via the LCD interface connectors. The logic levels of the LCD expansion connectors are 1.8V so it will require buffering of the signals to drive most LCD panels. The DSS is configured to a maximum of 24 bits, but can be used in lower bit modes if needed.

### 7.10.5 McBSP2

The multi-channel buffered serial port (McBSP) McBSP2 provides a full-duplex direct serial interface between the processor and the audio CODEC in the **TPS65950** using the I2S format. Only four signals are supported on the McBSP2 port. **Figure 30** is a depiction of McBSP2.

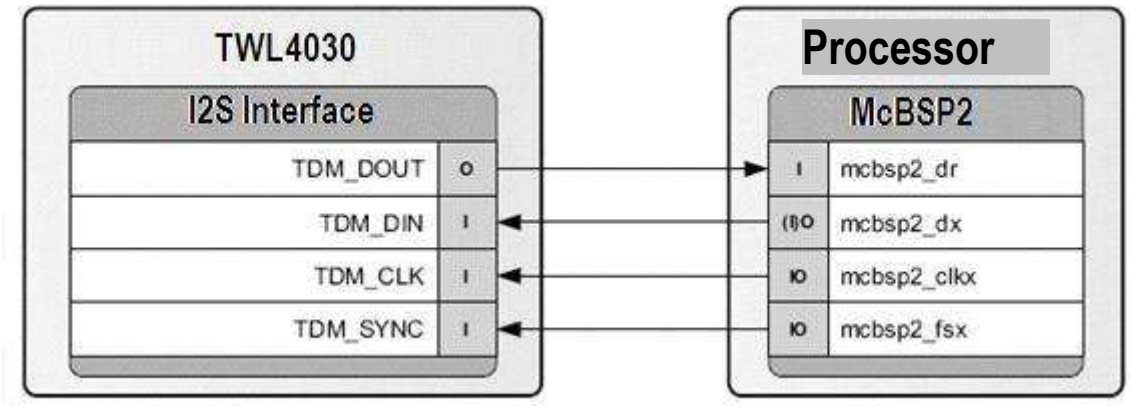



**Figure 30. McBSP2 Interface**

### 7.10.6 McBSP1

McBSP1 provides a full-duplex direct serial interface between the processor and the expansion interface. There are 6 signals supported on McBSP1, unlike the 4 signals on the other ports. **Figure 31** is a diagram of McBSP1.

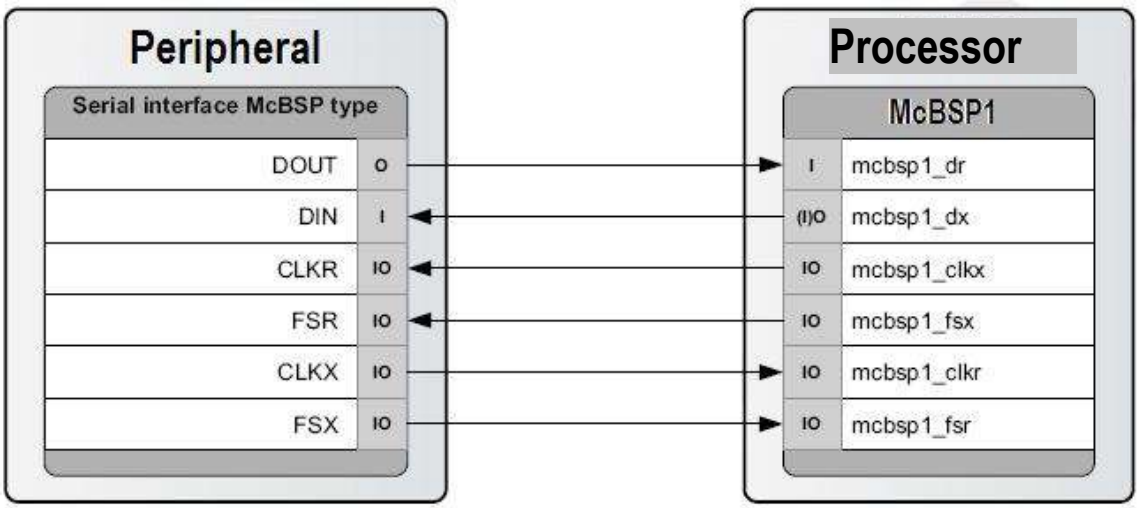



**Figure 31. McBSP1 Interface**

### 7.10.7 McBSP3

McBSP3 provides a full-duplex direct serial interface between the processor and the expansion interface. **Figure 32** is a diagram of McBSP3.

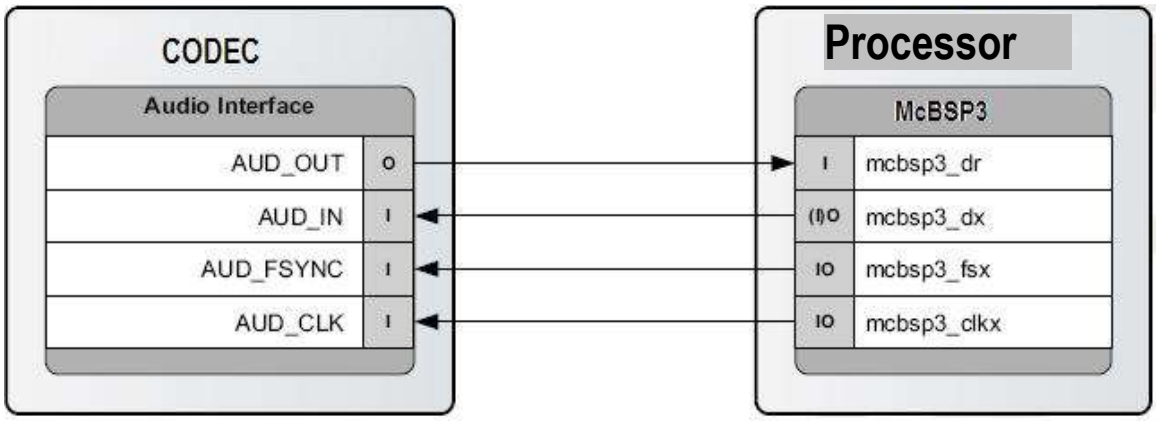



**Figure 32. McBSP3 Interface**

### 7.10.8 Pin Muxing

On the processor, the majority of pins have multiple configurations that the pin can be set to. In essence, the pin can become different signals depending on how they are set in the software. In order for the BeagleBoard to operate, the pins used must be set to the correct signal. In some cases, the default signal is the correct signal. Each pin can have a maximum of 8 options on the pin. This is called the pin mode and is indicated by a three bit value (0:3). In the case of the signals going to the expansion connector, the settings required for those pins depends on how they are to be used. For an explanation of the options, please refer to the Expansion Header section. Each pin can be set to a different mode independent of the other pins on the connector.

**Table 4** is a list of all of the signals used on the processor for the BeagleBoard and the required mode setting for each pin. Where the default setting is needed, it will be indicated. The USER notation under mode indicates that this is an expansion signal and can be set at the discretion of the user. A FIXED indicates that there is only one function for that signal and that it cannot be changed,

**Table 4. Processor Pin Muxing Settings**

| Signal | Mode |
|---|---|
| DSS | Default |
| MMC1 | Default |
| MMC2 | User |
| UART3 | Default |
| GPMC | Default |
| UART1 | Default |
| I2C1 | Default |
| I2C2 | Default |
| I2C3 | Default |
| I2C4 | Default |
| JTAG | FIXED |
| TV_OUT | Default |
| SYS_nRESPWRON | Default |
| SYS_nRESWARM | Default |
| SYS_nIRQ | Default |
| SYS_OFF | Default |
| SYS_CLKOUT | Default |
| SYS_CLKOUT2 | Default |
| SYS_CLKREQ | Default |
| SYS_XTALIN | FIXED |
| GPIO_149 | 4 |
| GPIO_150 | 4 |
| McBSP1 | Default |
| McBSP2 | User |
| McBSP3 | Default |
| GPIO_171 | 4 |
| GPIO_172 | 4 |

### 7.10.9 GPIO Mapping

There are a number of GPIO pins from the processor that are used on the BeagleBoard design. **Table 5** shows which of these GPIO pins are used in the design and whether they are inputs or outputs. While GPIO pins can be used as interrupts, the table only covers the GPIO pin mode. If it is an interrupt, then it is covered in the interrupt section.

**Table 5. Processor GPIO Pins**

| OMAP PIN | INT/GPIO | I/O | Signal | USAGE |
|---|---|---|---|---|
| AA9 | GPIO_150 | O | LED_GPIO150 | Controls User LED0 |
| W8 | GPIO_149 | O | LED_GPIO149 | Controls User LED1 |
| AG9 | GPIO_23 | I | MMC1_WP | SD/MMC card slot Write protect |
| J25 | GPIO_170 | O | DVI_PUP | Controls the DVI-D interface. A Hi = DVI-D enabled. |
| AE21 | GPIO_4 | I | SYSBOOT_5 | Used to put the device in the boot mode or as the **USER BUTTON** input. |

Other signals, such as those that connect to the expansion connector, may also be set as a GPIO pin. For information on those, refer to the Expansion Connector section.

### 7.10.10 Interrupt Mapping

There are a small number of pins on the processor that act as interrupts. Some of these interrupts are connected to the TPS65950 and their status is reflected through the main TPS65950 interrupt. **Table 6** lists the interrupts.

**Table 6. Processor Interrupt Pins**

| TPS65950 Pin | Processor PIN | INT/GPIO | USAGE |
|---|---|---|---|
| | AF26 | SYS_nIRQ | Interrupt from the TPS65950 |
| | AH8 | GPIO_29 | SD Write protect lead. Can be polled or set to an interrupt. |
| P12 | | GPIO0 | MMC1 card detect input. Goes to the processor over the SYS_nIRQ pin. |

## 7.11 POP Memory Device

The processor uses what is called POP (Package-on-Package) memory. The memory is a MCP (Multi Chip Package) that contains a dual Mobile DDR SDRAM stack. **Figure 33** shows the POP Memory concept.

**Figure 33. POP Memory**

The Memory device mounts on top of the processor. The configuration used on the board is a 200MHz 4Gb MDDR SDRAM device from Micron.

## 7.12 System Clocks

There are three main clocks needed for the operation of the board, 32KHz, 26MHz and McBSP_CLKS. **Figure 34** shows the components that make up the System Clocks. There are additional clocks needed elsewhere in the system, such as USB HUB, but those are discussed in separate sections.

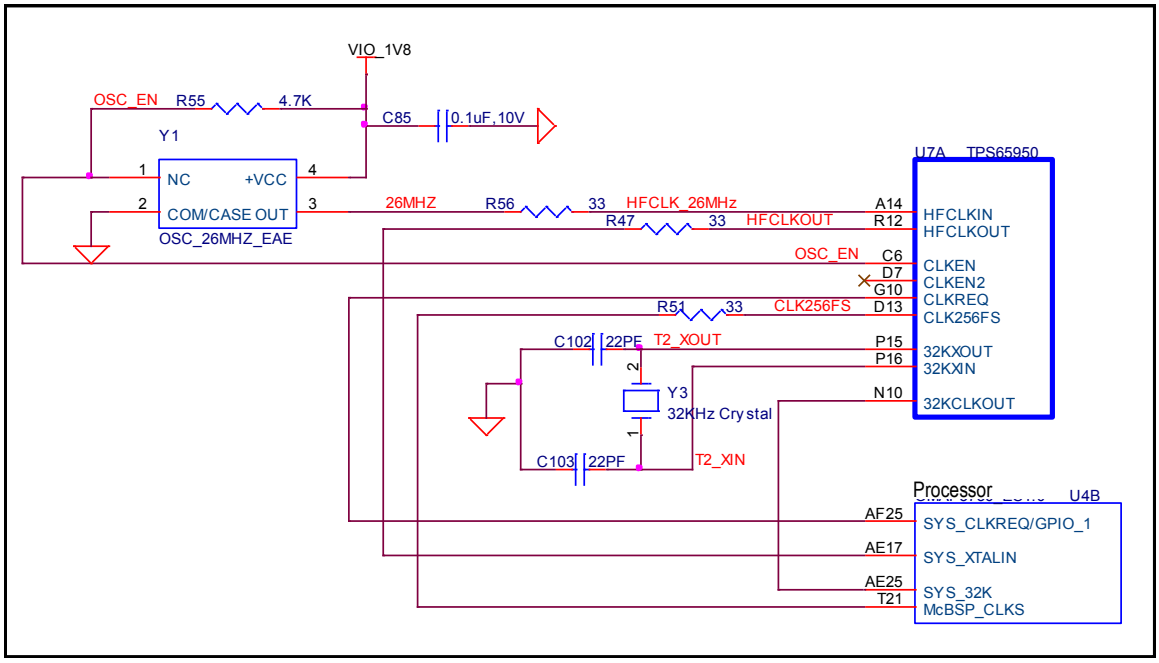


**Figure 34. System Clocks**

### 7.12.1 32KHz Clock

The 32KHz clock is needed for the TPS65950 and the processor and is provided by the **TPS65950** via the external 32KHz crystal, **Y2**. The **TPS65950** has a separate output from the crystal to drive the processor that buffers the resulting 32-kHz signal and provides it as **32KCLKOUT**, which is provided to the processor on ball **AE25**. The default mode of the 3**2KCLKOUT** signal is active, but it can be disabled if desired under SW control.

The 32.768-kHz clock drives the RTC embedded in the **TPS65950**. The RTC is not enabled by default; the host processor must set the correct date and time to enable the RTC.

### 7.12.2 26MHz Clock

This section describes the 26MHz clock section of the BeagleBoard.

#### *7.12.2.1 26MHz Source*

The BeagleBoard is designed to support two suppliers of the 26MHz oscillator. The **26MHz** clock is provided by an onboard oscillator, **Y1**. The **TPS65950** receives the external **HFCLKIN** signal on ball **A14** and uses it to synchronize or generate the clocks required to operate the **TPS65950** subsystems. The **TPS65950** must have this clock in order to function to the point where it can power up the BeagleBoard. This is the reason the **26MHz** clock is routed through the TPS65950.

#### *7.12.2.2 TPS65950 Setup*

When the **TPS65950** enters an active state, the Processor must immediately indicate the **HFCLKIN** frequency (26 MHz) by setting the HFCLK_FREQ bit field (bits [1:0]) in the CFG_BOOT register of the **TPS65950**. HFCLK_FREQ has a default of being not programmed, and in that condition, the USB subsection does not work. The three DCDC switching supplies (VIO, VDD1, and VDD2) operate from their free-running 3-MHz (RC) oscillators, and the PWR registers are accessed at a default 1.5-M byte. HFCLK_FREQ must be set by the processor during the initial power-up sequence. On the BeagleBoard, this is done by the internal boot ROM on startup.

#### *7.12.2.3 Processor 26MHz*

The 26MHz clock for the processor is provided by the TPS65950 on ball **R12** through **R38**, a 33 ohm resistor is providing to minimize any reflections on the clock line. The clock signal enters via ball **AE17** on the **PROCESSOR**.

### 7.12.3 McBSP_CLKS

An additional clock is also provided by the **TPS65950** called **McBSP_CL**KS. This clock is provided to the PROCESSOR in order to insure synchronization of the I2S interface between the processor and the **TPS65950**.

## 7.13 USB OTG Port

The BeagleBoard has a USB OTG (On-the-Go) port. It can be used as an OTG port, Client port, or Host port. The main use is as a client port, as that is the mode that will supply the power needed to power the BeagleBoard. With the addition of the USB Host ports, the need to use three OTG port as a Host, is not really needed.

***NOTE: In order to use the OTG in the Host mode, the BeagleBoard must be powered from the DC supply.***

### 7.13.1 USB OTG Overview

USB OTG is a supplement to the USB 2.0 specification. The standard USB uses a master/slave architecture, a USB host acting as a master and a USB peripheral acting as a slave. Only the USB host can schedule the configuration and data transfers over the link. The USB peripherals cannot initiate data transfers, they only respond to instructions given by a host.

USB OTG works differently in that gadgets don't need to be pure peripherals because they can sometimes act as hosts. An example might be connecting a USB keyboard or printer to BeagleBoard or a USB printer that knows how to grab documents from certain peripherals and print them. The USB OTG compatible devices are able to initiate the session, control the connection and exchange Host/Peripheral roles between each other.

The USB OTG supplement does not prevent the use of a hub, but it describes role swapping only in the case of a one-to-one connection where two OTG devices are directly connected. If a standard hub is used, the supplement notes that using it will lead to losing USB OTG role-swap capabilities making one device as the Default-Host and the other as the Default-Peripheral until the hub is disconnected.

The combination of the processor and the **TPS65950** allows the BeagleBoard to work as an OTG device if desired. The primary mode of operation however, is intended to be a client mode in order to pull power from the USB host which is typically a PC. As the Rev B does not have a Host USB port, this port will be used as a Host port in many applications.

### 7.13.2 USB OTG Design

**Figure 34** is the design of the USB OTG port on the BeagleBoard.

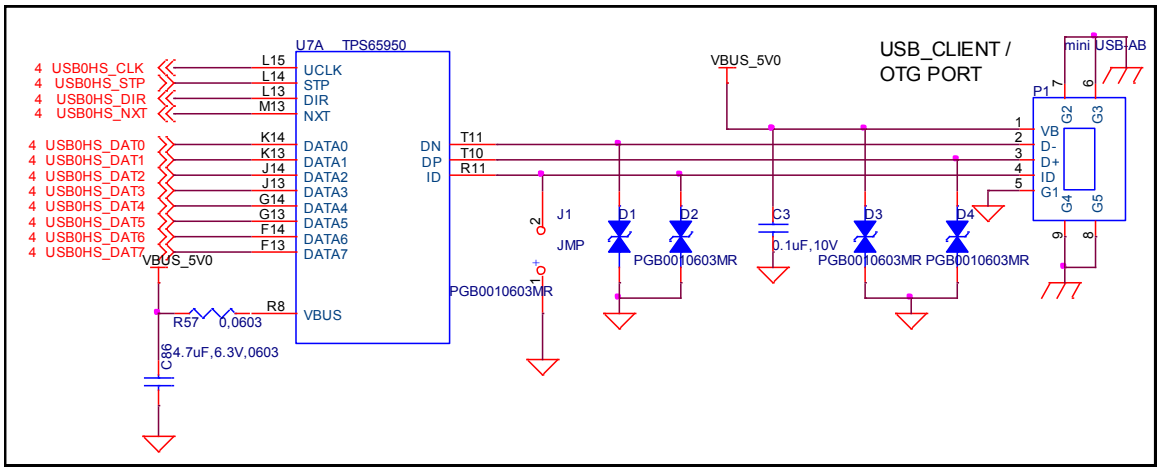



**Figure 35. USB OTG Design**

### 7.13.3 OTG ULPI Interface

ULPI is an interface standard for high-speed USB 2.0 systems. It defines an interface between USB link controller (processor) and the **TPS6595**0 that drives the actual bus. ULPI stands for UTMI+ low pin interface and is designed specifically to reduce the pin count of discrete high-speed USB PHYs. Pin count reductions minimize the cost and footprint of the PHY chip on the PCB and reduce the number of pins dedicated to USB for the link controller.

.

Unlike full- and low-speed USB systems, which utilize serial interfaces, high-speed requires a parallel interface between the controller and PHY in order to run the bus at 480Mbps. This leads to a corresponding increase in complexity and pin count. The ULPI used on the BeagleBoard keeps this down to only 12 signals because it combines just three control signals, plus clock, with an 8-bit bi-directional data bus. This bus is also used for the USB packet transmission and for accessing register data in the ULPI PHY.

#### *7.13.3.1 Processor Interface*

The controller for the ULPI interface is the Processor. It provides all of the required signals to drive the interface. **Table 7** describes the signals from the processor that are used for the USB OTG interface.

**Table 7. Processor ULPI Interface**

| Signal | Description | Type | Ball |
|---|---|---|---|
| hsusb0_clk | Dedicated for external transceiver 60-MHz clock input from PHY | I | T28 |
| hsusb0_stp | Dedicated for external transceiver Stop signal | O | T25 |
| hsusb0_dir | Dedicated for external transceiver Data direction control from PHY | I | R28 |
| hsusb0_nxt | Dedicated for external transceiver Next signal from PHY | I | T26 |
| hsusb0_data0 | Transceiver Bidirectional data bus | I/O | T27 |
| hsusb0_data1 | Transceiver Bidirectional data bus | I/O | U28 |
| hsusb0_data2 | Transceiver Bidirectional data bus | I/O | U27 |
| hsusb0_data3 | Transceiver Bidirectional data bus | I/O | U26 |
| hsusb0_data4 | Transceiver Bidirectional data bus | I/O | U25 |
| hsusb0_data5 | Transceiver Bidirectional data bus | I/O | V28 |
| hsusb0_data6 | Transceiver Bidirectional data bus | I/O | V27 |
| hsusb0_data7 | Transceiver Bidirectional data bus | I/O | V26 |

#### *7.13.3.2 TPS65950 Interface*

The **TPS65950** USB interfaces to the Processor over the ULPI interface. **Table 8** is a list of the signals used on the **TPS65950** for the ULPI interface.

**Table 8. TPS65950 ULPI Interface**

| Signal | Description | Type | Ball |
|---|---|---|---|
| UCLK | High speed USB clock | I/O | L15 |
| STP | High speed USB stop | I | L14 |
| DIR | High speed USB dir | O | L13 |
| NXT | High speed USB direction | O | M1 |
| DATA0 | High speed USB Data bit 0 | I/O | K14 |
| DATA1 | High speed USB Data bit 0 | I/O | K13 |
| DATA2 | High speed USB Data bit 0 | I/O | J14 |
| DATA3 | High speed USB Data bit 0 | I/O | J13 |
| DATA4 | High speed USB Data bit 0 | I/O | G14 |
| DATA5 | High speed USB Data bit 0 | I/O | G13 |
| DATA6 | High speed USB Data bit 0 | I/O | F14 |
| DATA7 | High speed USB Data bit 0 | I/O | F13 |

### 7.13.4 OTG Charge Pump

When the **TPS65950** acts as an A-device, the USB charge pump is used to provide 4.8 V/100 mA to the VBUS pin. When the **TPS65950** acts as a B-device, the USB charge pump is in high impedance. If used in the OTG mode as an A-device, the BeagleBoard will need to be powered from the DC supply. If acting as a B-device, there will not be a voltage source on the USB OTG port to drive the BeagleBoard. **Table 9** describes the charge pump pins.

**Table 9. USB OTG Charge Pump Pins**

| Signal | Description | Type | Ball |
|---|---|---|---|
| CP.IN | The charge pump input voltage. Connected to VBAT. | Power | R7 |
| CP.CAPP | The charge pump flying capacitor plus. | O | L14 |
| CP.CAPM | The charge pump flying capacitor minus. | O | T6 |
| CP.GND | The charge pump ground. | GND | R6 |

The charge pump is powered by the **VBAT** voltage rail. The charge pump generates a 4.8-V (nominal) power supply voltage to the **VBUS** pin. The input voltage range is 2.7 V to 4.5 V so the 4.2V VBAT is within this range. The charge pump operating frequency is 1 MHz. The charge pump integrates a short-circuit current limitation at 450 mA.

### 7.13.5 OTG USB Connector

The OTG USB interface is accessed through the miniAB USB connector. If you want to use the OTG port as a USB Host, **pin 4** of the connector must be grounded. The -xM Rev A version of Beagle provides jumper pad, **J6** that allows for a small piece of solder to be placed on the pads to perform this function. It should be noted that with the USB Host port on the -xM Rev A Beagle, the need to convert the OTG port to a host mode is greatly diminished.

### 7.13.6 OTG USB Protection

Each lead on the USB port has ESD protection. In order for the interface to meet the USB 2.0 Specification Eye Diagram, these protection devices must be low capacitance.

## 7.14 Onboard USB HUB

A new feature of the –xM board is the inclusion of an onboard USB 4 port hub with an integrated 10/100 Ethernet. This section describes the design of the HUB and the interface to the processor. This allows for the support of LS and FS USB devices without the need for an external USB HUB. **Figure 36** is a high level block diagram of the system design of the integrated HUB.

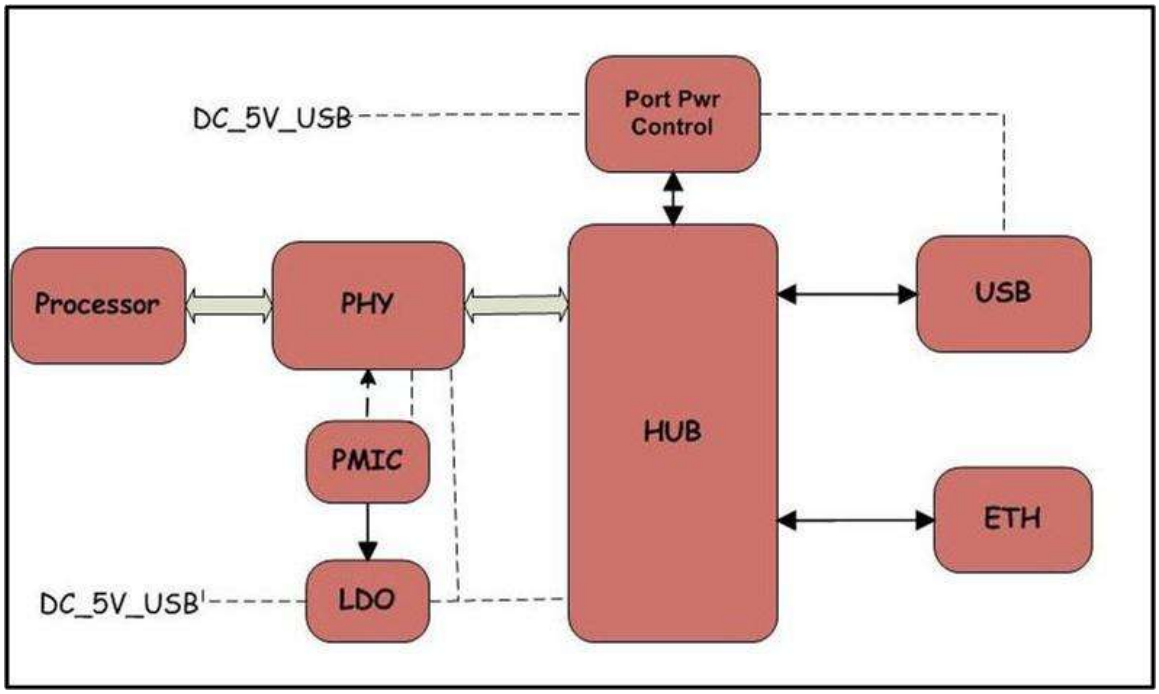



**Figure 36. USB HUB Block Diagram**

The following section covers each of the key function in the overall design.

- Power
- HS USB PHY
- HUB
- USB Port Power
- Ethernet

### 7.14.1 Power

The power for the HUB is provided by two sources. **Figure 37** is the design of the HUB power circuitry. The **HUB_3V3** rail, the main supply rail for the HUB, is provided by **U16**, a **TL1963A** LDO. Power for the LDO is provided by the **DC_5V_USB** rail from the overvoltage protection circuit. The LDO is set to provide 3.3V and is set by **R111** and **R113**. This rail can be turned on or off from the processor by using the I2C bus to communicate to the **TPS65950**. By default, the LDO is turned off.

The **TPS65950** provides the **USB_1V8** rail which is used by the USB PHY. The processor can turn on or off this rail by communicating with the **TPS65950** via the I2C bus.

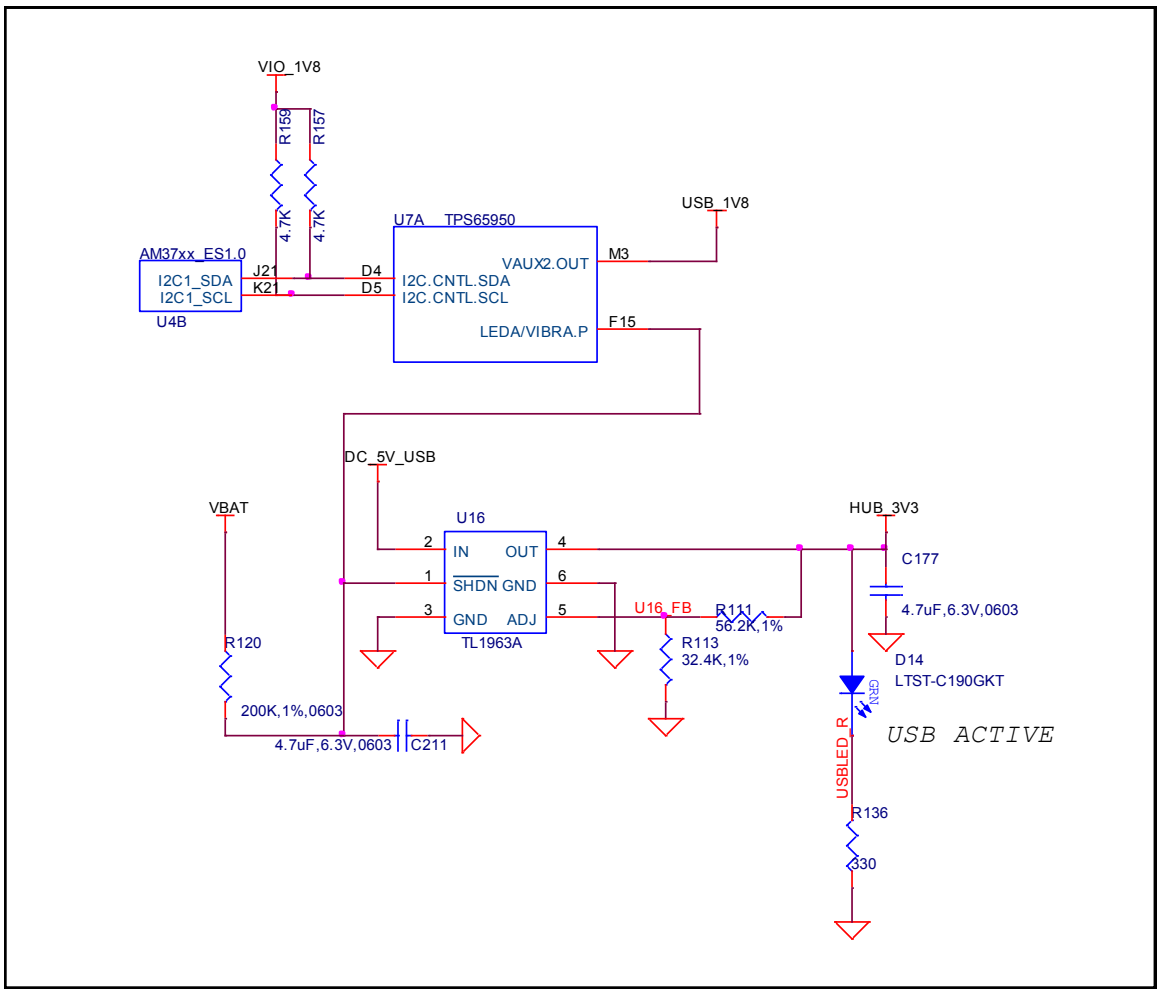



**Figure 37. HUB Power Circuitry**

A green LED**, D14**, indicates that power is applied to the HUB circuitry.

### 7.14.2 HS USB PHY

The configuration of the HS USB PHY is basically the same as on the Rev BeagleBoard design. A PHY is required between the processor ULPI interface and the USB HUB. **Figure 39** shows the processor and PHY interface.

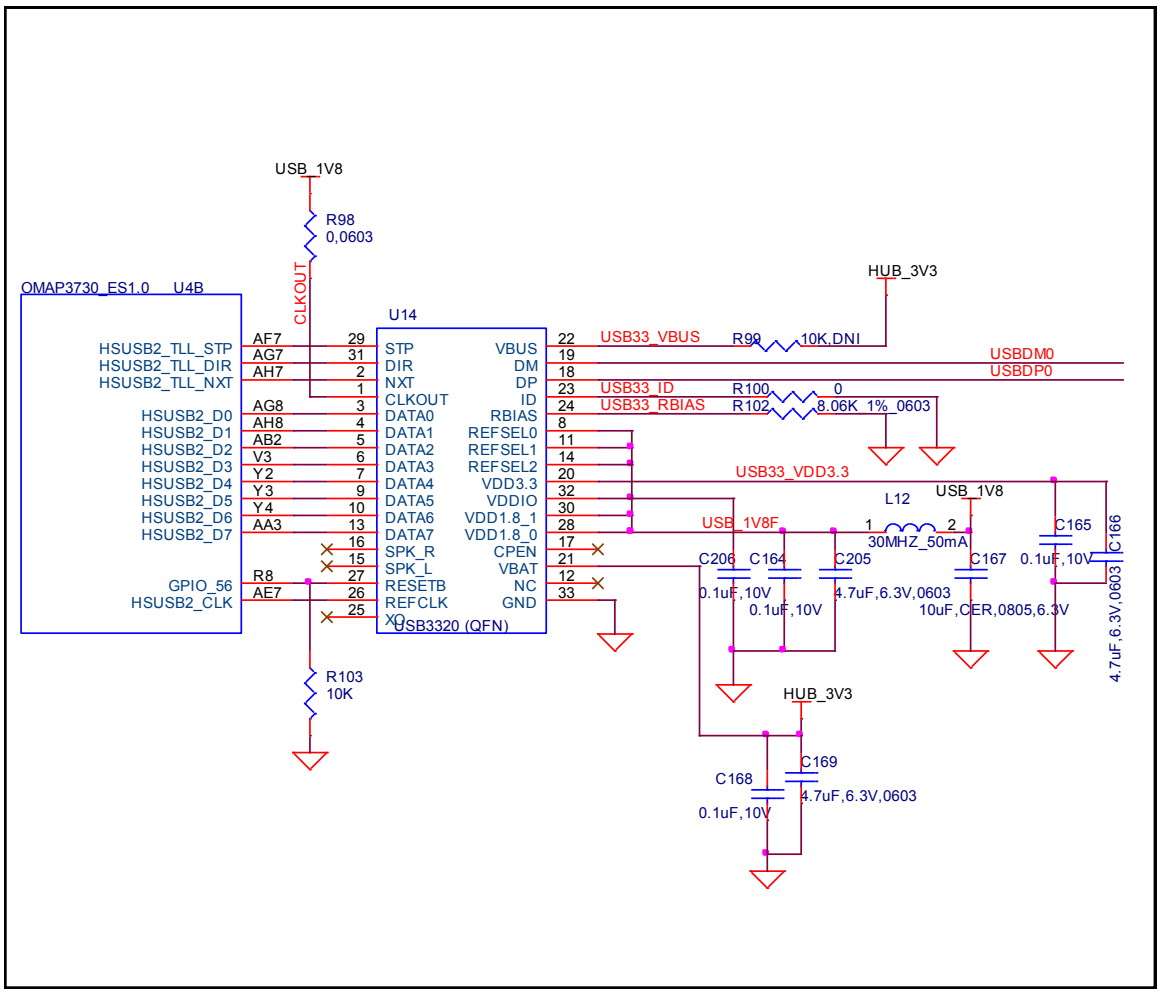



**Figure 38. USB PHY Design**

The interface to the processor is the HSUSB2 interface. The signals used on this interface are contained in **Table 10**.

**Table 10. USB Host Port OMAP Signals**

| Signal | Description | Input/Output |
|---|---|---|
| Hsusb2_clk | External transceiver 60-MHz clock output to PHY | O |
| Hsusb2_stp | External transceiver Stop signal | O |
| Hsusb2_dir | Transceiver data direction control from PHY | I |
| Hsusb2_nxt | Next signal from PHY | I |
| Hsusb2_data0 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data1 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data2 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data3 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data4 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data5 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data6 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Hsusb2_data7 | Bidirectional data bus signal for 12-pin ULPI operation | I/O |
| Gpio_147 | Enable/reset line to the USB PHY. | O |

The **husb2_clk** signal is an output only and is used to support a HS USB PHY that supports an input clock mode. The SMSC PHY device supports this mode and is used on the Beagle.

The PHY used in the design is a **USB3320** series device from SMSC. The **USB3320** is a highly integrated Hi-Speed USB2.0 Transceiver (PHY) that meets all of the electrical requirements to be used as a Hi-Speed USB Host. In this design, only the host mode of operation is being supported as it is used to connect to the HUB on the board.

In order to interface to the processor, the device must be used in the 60MHz clock mode. This is done by tying the **CLKOUT** signal on the USB PHY to VIO_1V8. On -XM Rev A, a zero ohm series resistor was added. This is not required, but was added as a "just in case" option if the CLKOUT signal was a source of noise in the PHY. It was proven not to be the case. The clock for the PHY is derived from the 60MHz signal generated by the processor. All of the signals and their functions align with the descriptions found in the processor interface section.

The USB3322 device requires two voltages, the **USB_1V8** rail to power the I/O rails and the **HUB_3V3** to power the rest of the device. The 3.3V rail for the device is generated internally and requires a filter and bypass cap to be connected externally. The USB_1V8 rail is derived from the **VAUX2** rail supplied by the **TPS65950** PMIC.

The **RBIAS** block in the PHY consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. The nominal voltage at **RBIAS** is 0.8V and therefore the resistor will dissipate approximately 80μW of power.

As we are not using this device to support the OTG protocol but instead as a host device, we ground the **ID** pin to force it into a Host mode at all times. The **USB3322** transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming.

### 7.14.3 USB HUB

The key component in the HUB design is a SMSC LAN9514 USB HUB plus Ethernet device. **Figure 40** is the HUB design.

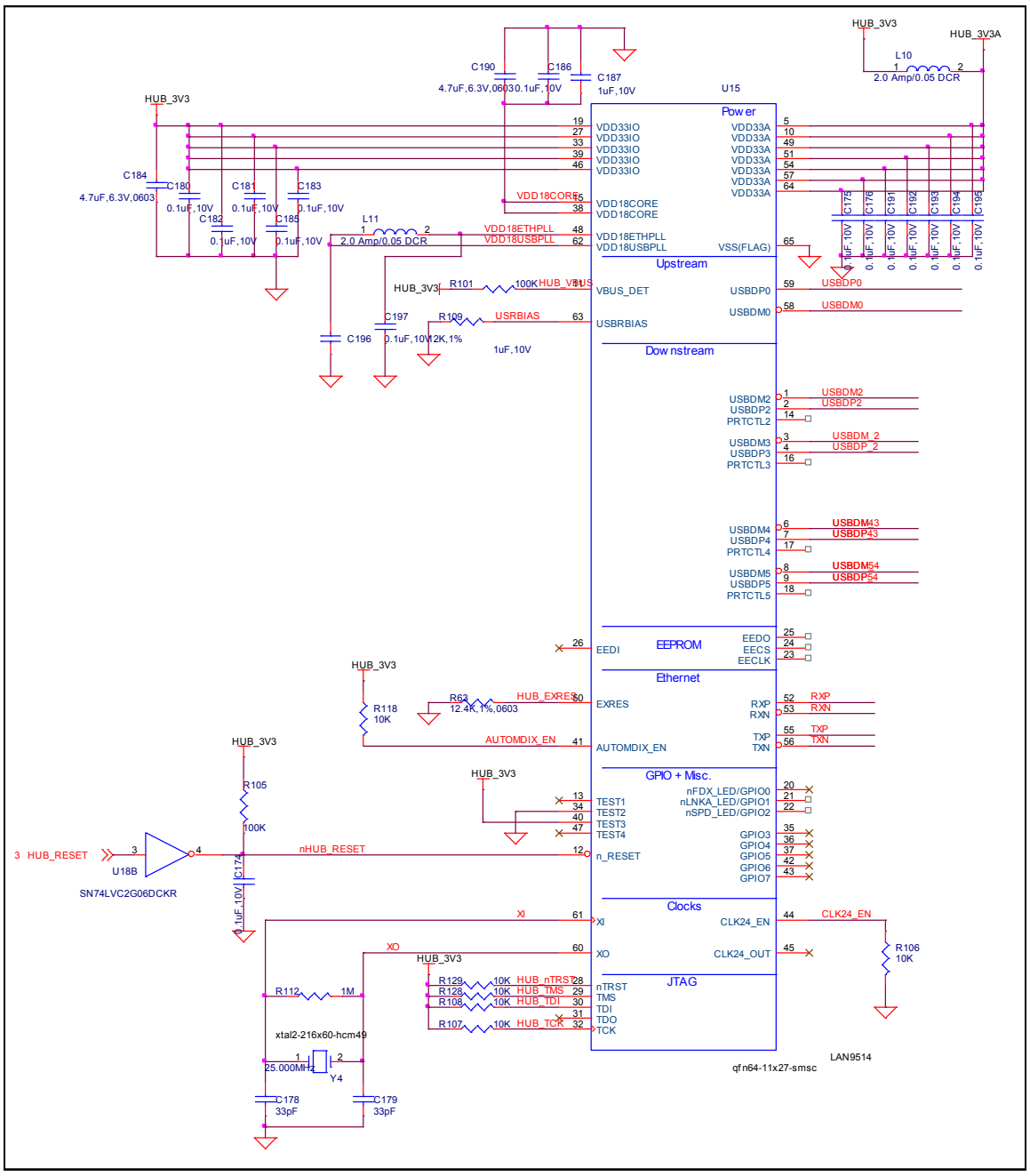



**Figure 39. USB HUB Design**

The LAN9514/LAN9514i is a high performance Hi-Speed USB 2.0 hub with a 10/100 Ethernet controller. The LAN9514/LAN9514i contains an integrated USB 2.0 hub, four integrated downstream USB 2.0 PHYs, an integrated upstream USB 2.0 PHY, a 10/100 Ethernet PHY, a 10/100 Ethernet Controller.

The main power supply for the LAN9514 is the HUB_3V3 supplied by the dedicated power regulator. Filtering is required on all input pins. A 1.8V core voltage is derived from an internal LDO and requires external filtering.

The LAN9514 requires an external 25MHZ crystal to generate the required internal clocks. The optional 24MHz clock output is not used on the board and is disabled.

The AUTOMIDX feature is enabled which allows for auto polarity detection. This enables the port to automatically switch the TX and RX leads if needed.

### 7.14.4 USB Port Connectors

There a two dual port type A USB connectors used on the –xM board each one provides connections for four signals, DP, DM, VBUS, and Ground. You will notice that there are no external ESD devices on the connector. The ESD protection is integrated into the USB HUB.

**Figure 41** is the design of the power control for each USB host port. Each port can be turned on or off from the **LAN9514** over the USB interface. U13, a TPS2045, is a four port FET with over current detection. The overcurrent detect output is tied to the enable pin from the LAN9514. In an over current condition the signal is immediately turned off without waiting for the processor to turn off the power. The **LAN9514** detects the overcurrent condition and keeps the over current condition turned off.

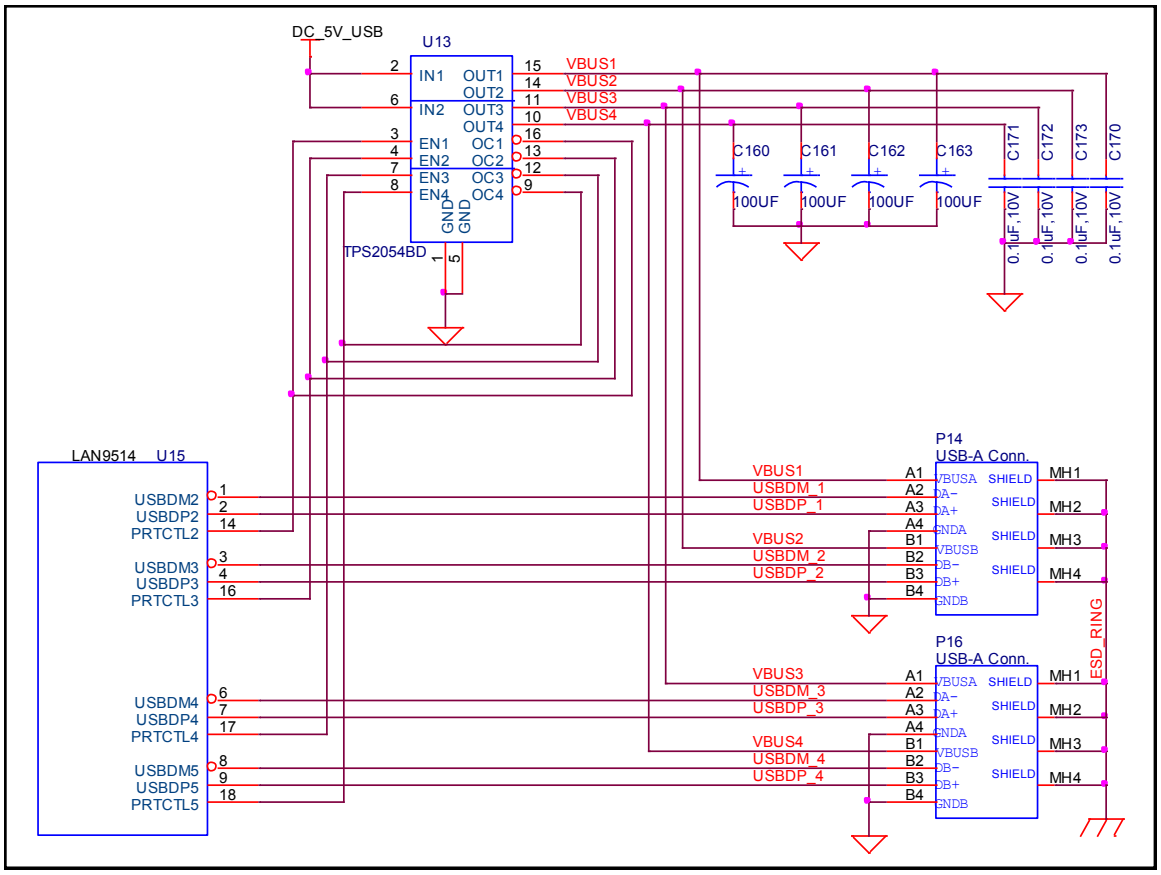



**Figure 40. USB Port Power Design**

Each USB Host port has its own dedicated FET and power control. A 100uf capacitor is connected to each USB power port for added surge current capabilities. A .1uf capacitor is provided for bypass capacitance on each rail.

### 7.14.5 Ethernet

**Figure 41** is the circuitry that applies to the Ethernet interface on the board. The **LAN9514** device while performing the function of the HUB also contains the Ethernet controller.

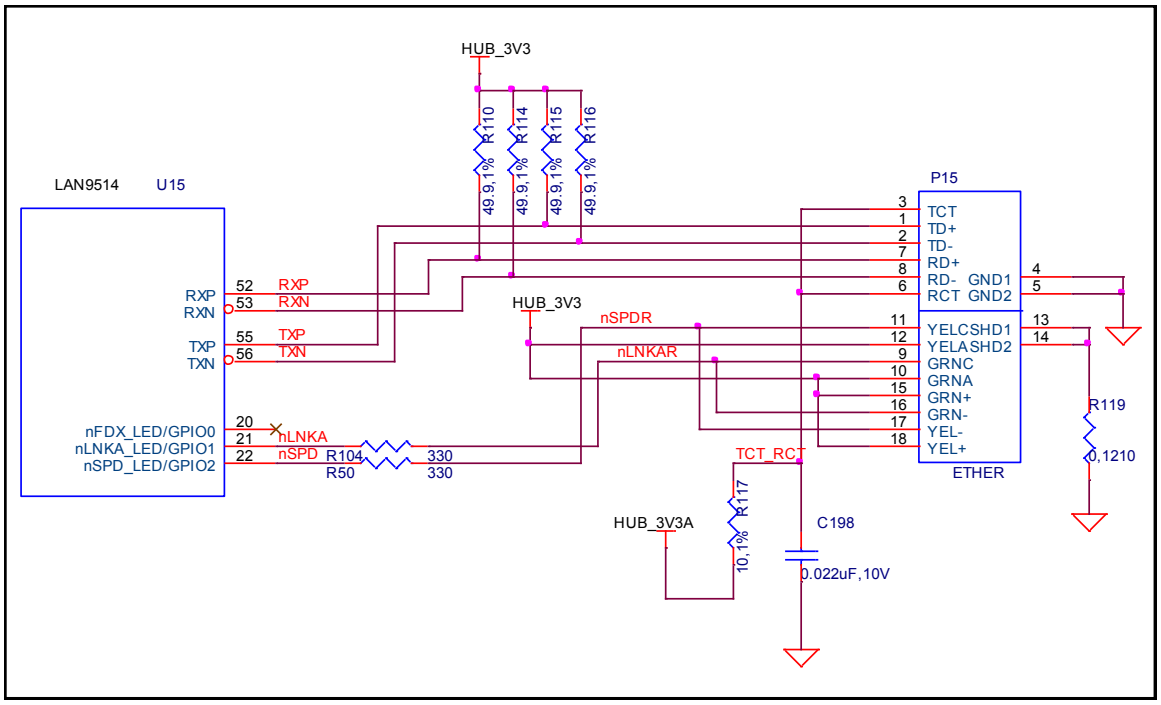



**Figure 41. USB Based Ethernet Design**

The 10/100 Ethernet controller provides an integrated Ethernet MAC and PHY which are fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant. A connector, P15, with integrated magnetics is used to provide the physical interface off the board. The Ethernet features auto polarity correction and Auto-MIDX.

## 7.15 microSD

The board provides a single microSD interface. Its primary use is for providing the boot source for SW. Unlike the BeagleBoard, it cannot be used for the typical SDIO or MMC functions. **Figure 42** is the microSD interface design on the BeagleBoard.

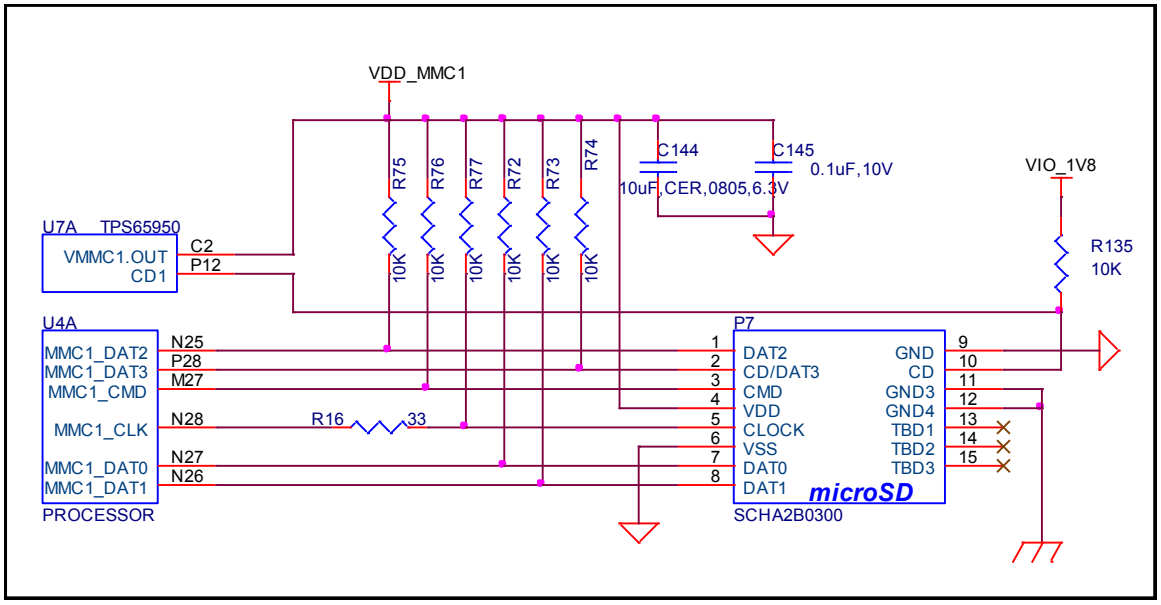



**Figure 42. microSD Interface**

### 7.15.1 microSD Power

The microSD connector is supplied power from the **TPS65950** using the **VMMC1** rail. The default setting on this rail is 3.0V as set by the Boot ROM and under SW control, can be set to 1.80V for use with 1.8V cards. The maximum current this rail can provide is 220mA as determined by the **TPS65950** regulator. Maximum current can be limited by the overall current available from the USB interface of the PC.

### 7.15.2 Processor Interface

There are no external buffers required for the microSD operation. The processor provides all of the required interfaces for the microSD interface. **Table 11** provides a description of the signals on the MMC card.

**Table 11. SD/MMC OMAP Signals**

| Signal Name | Description | I/O | Pin |
|---|---|---|---|
| MMC1_CLK | SD/MMC Clock output. | O | N28 |
| MMC1_CMD | SD/MMC Command pin | I/O | M27 |
| MMC1_DAT(0..7) | SD/MMC Data pins | I/O | N27,N26,N25,P28,P27, |

| | | | |
|---|---|---|---|
| | | | P26,R27,R25 |

### 7.15.3 Card Detect

When a card is inserted into the connector, the **Card Detect** pin is grounded. This is detected on pin **P12** of the **TPS65950**. An interrupt, if enabled, is sent to the processor via the interrupt pin. The SW can be written such that the system comes out of sleep or a reduced frequency mode when the card is detected.

### 7.15.4 Booting From SD/MMC Cards

The ROM code supports booting from the microSD cards with some limitations:

- Support for SD cards compliant with the Multimedia Card System Specification v4.2 from the MMCA Technical Committee and the Secure Digital I/O Card Specification v2.0 from the SD Association. Including high-capacity (size >2GB) cards: HC-SD and HC MMC.
- 3-V power supply, 3-V I/O voltage on port 1
- Initial 1-bit MMC mode, 4-bit SD mode.
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: 20 MHz
- Only one card connected to the bus
- FAT12/16/32 support, with or without master boot sector (MBR).

The high-speed microSD host controllers handle the physical layer while the ROM code handles the simplified logical protocol layer (read-only protocol). A limited range of commands is implemented in the ROM code. The MMC/SD specification defines two operating voltages for standard or high-speed cards. The ROM code only supports standard operating voltage range (3-V). The ROM code reads out a booting file from the card file system and boots from it.

## 7.16 Audio Interface

The BeagleBoard supports stereo in and out through the **TPS65950** which provides the audio CODEC.

**Figure 43** is the Audio circuitry design on the BeagleBoard.

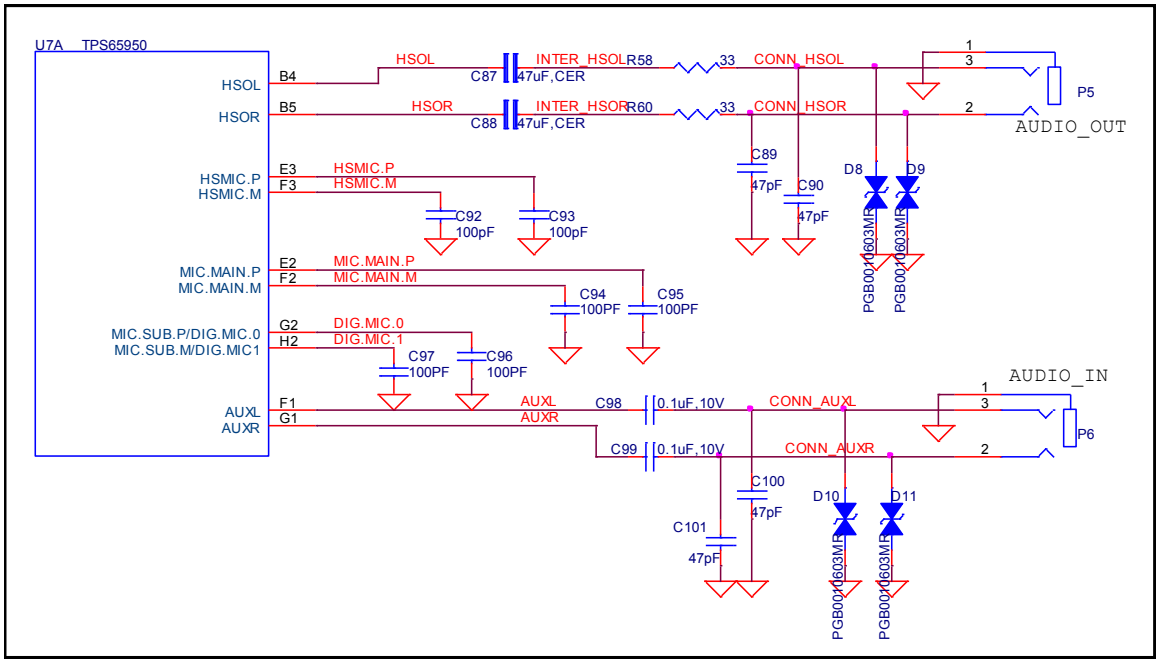



**Figure 43. Audio Circuitry**

### 7.16.1 Processor Audio Interface

There are five McBSP modules called McBSP1 through McBSP5 on the processor. **McBSP2** provides a full-duplex, direct serial interface between CODEC inside the **TPS65950**. It supports the I2S format to the TPS65950. In **Table 12** are the signals used on the processor to interface to the CODEC.

**Table 12. Processor Audio Signals**

| Signal Name | Description | I/O | Pin |
|---|---|---|---|
| mcbsp2_dr | Received serial data | I | R21 |
| mcbsp2_dx | Transmitted serial data | I/O | M21 |
| mcbsp2_clkx | Combined serial clock | I/O | N21 |
| mcbsp2_fsx | Combined frame synchronization | I/O | P21 |
| Mcbsp_clks | External clock input. Used to synchronize with the TPS65950 | I | T21 |

### 7.16.2 TPS65950 Audio Interface

The **TPS65950** acts as a master or a slave for the I2S interface. If the **TPS65950** is the master, it must provide the frame synchronization (I2S_SYNC) and bit clock (I2S_CLK) to the processor. If it is the slave, the **TPS65950** receives frame synchronization and bit clock. The **TPS65950** supports the I2S left-justified and right-justified data formats, but doesn't support the TDM slave mode.

In **Table 13** are all the signals used to interface to the processor.

**Table 13. Processor Audio Signals**

| Signal Name | Description | I/O | Pin |
|---|---|---|---|
| I2S.CLK | Clock signal (audio port) | I/O | L3 |
| I2S.SYNC | Synchronization signal (audio port) | IO | K6 |
| I2S.DIN | Data receive (audio port) | I | K4 |
| I2S. DOUT | Data transmit (audio port) | O | K3 |
| CLK256FS | Synchronization frame sync to the PROCESSOR | O | D13 |

A new feature on the –xM is the ability to access the audio signals for use on an external add on board. If this feature is to be used, you must disable via SW this interface on the TPS65950.

### 7.16.3 Audio Output Jack

A single 3.5mm jack is provided on BeagleBoard to support external stereo audio output devices such as headphones and powered speakers. This interface is not amplified and may require the use of amplified speakers in certain instances.

### 7.16.4 Audio Input Jack

A single 3.5mm jack is supplied to support external audio inputs including stereo or mono. If a microphone is o be used, it may require additional amplification of the signal for proper use.

## 7.17 DVI-D Interface

The LCD interface on the processor is accessible from the **DVI-D** interface connector on the board. **Figure 44** is the DVI-D interface design.

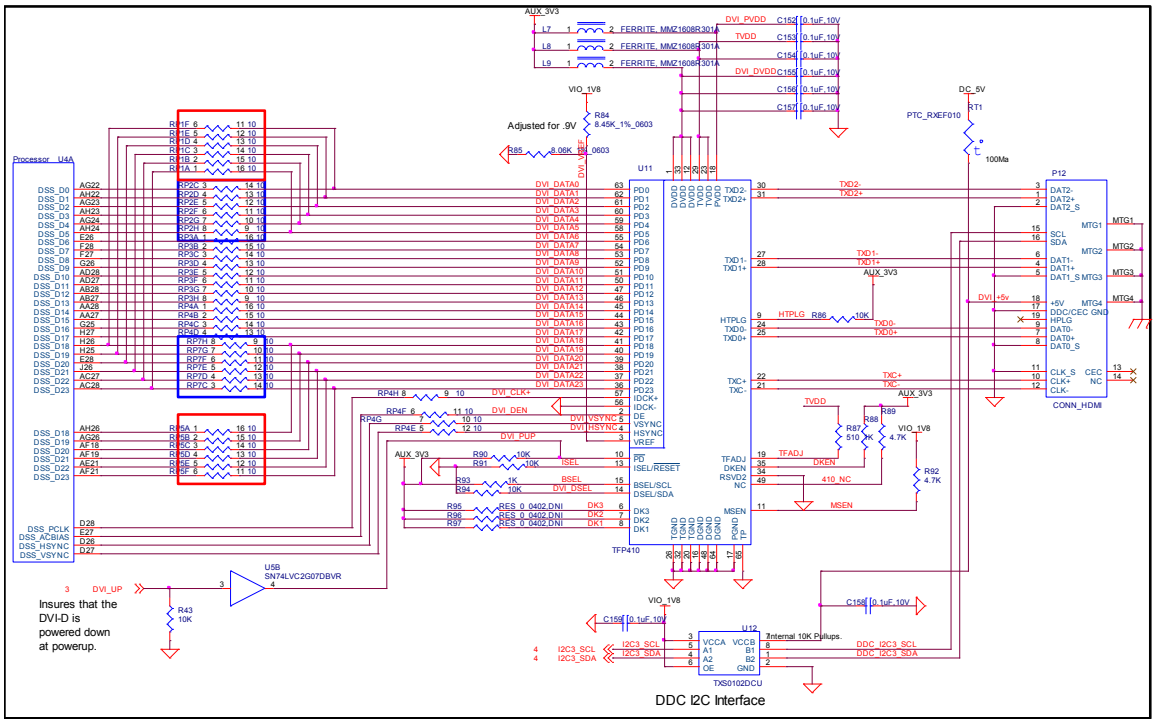



**Figure 44. DVI-D Interface**

One of the main changes in the DSS area on the –xM is the change of the DSS pin usage. The processor requires that different pins be used if 720p resolutions are required. These pins are different than those that are currently used on the BeagleBoard. The basic change requires that the **DSS_D0-D5** need to be moved to the pins that normally carry the **DSS_D18-D23** leads. In this case, the signals for **DSS_D18-D23** need to be moved to other pins. Reflected in **Figure 44** are four resistor packs inside either Red or Blue boxes. These are the loading options to enable the new mode used by the –xM or the legacy mode used by the BeagleBoard. The resistor packs in the RED boxes are installed and the BLUE boxes are not installed on the –xM to support the 720p resolution.

For legacy operation, you would need to install the BLUE boxes and leave out the RED boxes. The SW will take care of this automatically, but you may want to do this if your design were to need to work in the legacy mode.

### 7.17.1 Processor LCD Interface

The main driver for the DVI-D interface originates at the processor via the **DSS** pins. The PROCESSOR provides 24 bits of data to the DVI-D framer chip, **TFP410**. There are three other signals used to control the DVI-D that originate at the processor. These are I2C3_SCL, I2C3_SDA, and GPIO_170. All of the signals used are described in **Table 14.**

**Table 14. Processor LCD Signals**

| Signal | Description | | Type | Ball (Legacy) | Ball (720p) |
|---|---|---|---|---|---|
| dss_pclk | LCD Pixel Clock | | O | D28 | D28 |
| dss_hsync | LCD Horizontal Synchronization | | O | D26 | D26 |
| dss_vsync | LCD Vertical Synchronization | | O | D27 | D27 |
| dss_acbias | Pixel data enable (TFT) output | | O | E27 | E27 |
| dss_data0 | LCD Pixel Data bit 0 | BLUE0 | O | AG22 | H26 |
| dss_data1 | LCD Pixel Data bit 1 | BLUE1 | O | AH22 | H25 |
| dss_data2 | LCD Pixel Data bit 2 | BLUE2 | O | AG23 | E28 |
| dss_data3 | LCD Pixel Data bit 3 | BLUE3 | O | AH23 | J26 |
| dss_data4 | LCD Pixel Data bit 4 | BLUE4 | O | AG24 | AC27 |
| dss_data5 | LCD Pixel Data bit 5 | BLUE5 | O | AH24 | AC28 |
| dss_data6 | LCD Pixel Data bit 6 | BLUE6 | O | E26 | E26 |
| dss_data7 | LCD Pixel Data bit 7 | BLUE7 | O | F28 | F28 |
| dss_data8 | LCD Pixel Data bit 8 | GREEN0 | O | F27 | F27 |
| dss_data9 | LCD Pixel Data bit 9 | GREEN1 | O | G26 | G26 |
| dss_data10 | LCD Pixel Data bit 10 | GREEN2 | O | AD28 | AD28 |
| dss_data11 | LCD Pixel Data bit 11 | GREEN3 | O | AD27 | AD27 |
| dss_data12 | LCD Pixel Data bit 12 | GREEN4 | O | AB28 | AB28 |
| dss_data13 | LCD Pixel Data bit 13 | GREEN5 | O | AB2 | AB2 |
| dss_data14 | LCD Pixel Data bit 14 | GREEN6 | O | AA28 | AA28 |
| dss_data15 | LCD Pixel Data bit 15 | GREEN7 | O | AA27 | AA27 |
| dss_data16 | LCD Pixel Data bit 16 | RED0 | O | G25 | G25 |
| dss_data17 | LCD Pixel Data bit 17 | RED1 | O | H27 | H27 |
| dss_data18 | LCD Pixel Data bit 18 | RED2 | O | H26 | AH26 |
| dss_data19 | LCD Pixel Data bit 19 | RED3 | O | H25 | AG26 |
| dss_data20 | LCD Pixel Data bit 20 | RED4 | O | E28 | AF18 |
| dss_data21 | LCD Pixel Data bit 21 | RED5 | O | J26 | AF19 |
| dss_data22 | LCD Pixel Data bit 22 | RED6 | O | AC27 | AE21 |
| dss_data23 | LCD Pixel Data bit 23 | RED7 | O | AC28 | AF21 |
| GPIO_170 | Powers down the TFP410 when Lo. TFP410 is active when Hi. | | O | J25 | |
| I2C3_SCL | I2C3 clock line. Used to communicate with the monitor to determine setting information. | | I/O | AF14 | AF14 |
| I2C3_SDA | I2C3 data line. Used to communicate with the monitor to determine setting information. | | I/O | AG14 | AG14 |

10ohm series resistors are provide in the signal path to minimize reflections in the high frequency signals from the processor to the **TFP410**. These resistors are in the form of

resistor packs on the BeagleBoard. The maximum clock frequency of these signals is 65MHz.

It should be noted that on the Rev A2 version, the ability to shut off the DVI-D display is not supported. This will be fixed on the next letter revision of the board.

### 7.17.2 LCD Power

In order for the DSS outputs to operate correctly out of the processor, two voltage rails must be active, **VIO_1V8 and VDD_PLL2**. Both of these rails are controlled by the **TPS65950** and must be set to 1.8V. By default, **VDD_PLL2** is not turned and must be activated by SW. Otherwise some of the bits will not have power supplied to them.

### 7.17.3 TFP410 Power

Power to the TFP410 is supplied from the 3.3V regulator in **U1**, the **TPS2141**. In order to insure a noise free signal, there are three inductors, **L4**, **L5**, and **L6** that are used to filter the 3.3V rail into the TFP410.

### 7.17.4 TFP410 Framer

The **TFP410** provides a universal interface to allow a glue-less connection to provide the DVI-D digital interface to drive external LCD panels. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with the 1.8V and 24-bit interface output by the processor. The DVI interface on the BeagleBoard supports flat panel display resolutions up to XGA at 65 MHz in 24-bit true color pixel format.

**Table 15** is a description of all of the interface and control pins on the **TFP410** and how they are used on BeagleBoard.

**Table 15. TFP410 Interface Signals**

| Signal Name | Description | Type | Ball |
|---|---|---|---|
| DATA[23:12] | The upper 12 bits of the 24-bit pixel bus. | I | 36–47 |
| DATA[11:0] | The bottom 12 bits of the 24-bit pixel bus. | I | 50–55.56-53 |
| IDCK+ | Single ended clock input. | I | 57 |
| IDCK- | Tied to ground to support the single ended mode. | I | 56 |
| DE | Data enable. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC and VSYNC. | I | 2 |
| HSYNC | Horizontal sync input | I | 4 |
| VSYNC | Vertical sync input | I | 5 |
| DK3 | These three inputs are the de-skew inputs DK[3:1], used to adjust the setup and hold times of the pixel data inputs DATA[23:0], relative to the clock input IDCK±. | I | 6 |
| DK2 | | I | 7 |
| DK1 | | I | 8 |
| | A low level indicates a powered on receiver is detected at the | | |

| | | | |
|---|---|---|---|
| MSEN | differential outputs. A high level indicates a powered on receiver is not detected. | O | 11 |
| ISEL | This pin disables the I2C mode on chip. Configuration is specified by the configuration pins (BSEL, DSEL, EDGE, VREF) and state pins (PD, DKEN). | I | 13 |
| BSEL | Selects the 24bit and single-edge clock mode. | I | 13 |
| DSEL | Lo to select the single ended clock mode. | I | 14 |
| EDGE | A high level selects the primary latch to occur on the rising edge of the input clock IDCK | I | 9 |
| DKEN | A HI level enables the de-skew controlled by DK[1:3] | I | 35 |
| VREF | Sets the level of the input signals from the PROCESSOR. | I | 3 |
| PD | A HI selects normal operation and a LO selects the powerdown mode. | I | 10 |
| TGADJ | This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor RTFADJ connected to 3.3V. | I | 19 |

### 7.17.5 TFP410 Control Pins

There are twelve control pins that set up the TFP410 to operate with the processor. Most of these pins are set by HW and do not require any intervention by the processor to set them.

#### *7.17.5.1 ISEL*

The **ISEL** pin is pulled LO via **R99** to place the TFP410 in the control pin mode with the I2C feature disabled. This allows the other modes for the TFP410 to be set by the other control pins.

#### *7.17.5.2 BSEL*

The **BSEL** pin is pulled HI to select the 24 bit mode for the Pixel Data interface from the processor.

#### *7.17.5.3 DSEL*

The **DSEL** pin is pulled low to select the single ended clock mode from the **PROCESSOR**.

#### *7.17.5.4 EDGE*

The **EDGE** signal is pulled HI through **R82** to select the rising edge on the IDCK+ lead which is the pixel clock from the **PROCESSOR**.

#### *7.17.5.5 DKEN*

The **DKEN** signal is pulled HI to enable the de-skew pins. The de-skew pins, **DK1-DK3,** are pulled low by the internal pulldown resistors in the **TFP410**. This is the default mode

of operation. If desired, the resistors can be installed to pull the signals high. However, it is not expected that any of the resistors will need to be installed. The DK1-DK3 pins adjust the timing of the clock as it relates to the data signals.

#### *7.17.5.6 MSEN*

The **MSEN** signal, when low, indicates that there is a powered monitor plugged into the DVI-D connector. This signal is not connected to the processor and is provided as a test point only.

#### *7.17.5.7 VREF*

The **VREF** signal sets the voltage level of the **DATA**, **VSYNC**, **HSYNC**, **DE**, and **IDCK+** leads from the processor. As the processor is 1.8V, the level is set to .9V by **R64** and **R65**.

#### *7.17.5.8 PD*

The **PD** signal originates from the processor on the **GPIO_170** pin. Because the **P**D signal on the **TFP410** is 3.3V referenced, this signal must be converted to **3.3V**. This is done by **U4**, **SN74LVC2G07**, a non-inverting open drain buffer. If the **GPIO_170** pin is HI, then the open drain signal is inactive, causing the signal to be pulled HI by **R98**. When **GPIO_170** is taken low, the output of **U4** will also go LO, placing the **TFP410** in the power down mode. Even though **U4** is running at 1.8V to match the processor, the output will support being pulled up to **3.3V**. On power up, the TFP410 is disabled by **R109**, a 10K resistor. When the processor powers on, pin **J25** comes in the safe mode, meaning it is not being driven. **R109** insures that the signal is pulled LO, putting the TFP410 in the power down mode.

#### *7.17.5.9 TFADJ*

The **TFADJ** signal controls the amplitude of the DVI output voltage swing, determined by the value of **R95**.

#### *7.17.5.10 RSVD2*

This unused pin is terminated to ground as directed by the TFP410 data manual.

#### *7.17.5.11 NC*

This unused pin is pulled HI as directed by the TFP410 data manual.

### 7.17.6 DVI-D Connector

In order to minimize board size, a HDMI connector was selected for the DVI-D connection. The BeagleBoard does not support HDMI but only the DVI-D component of HDMI. The Cable is not supplied with the BeagleBoard but is available from numerous cable suppliers and is required to connect a display to the BeagleBoard.

#### *7.17.6.1 Shield Wire*

Each signal has a shield wire that is used in the cable to provide signal protection for each differential pair. This signal is tied directly to ground.

#### *7.17.6.2 DAT0+/DAT0-*

The differential signal pair **DAT0+/DAT0-** transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.

#### *7.17.6.3 DAT1+/DAT1-*

The differential signal pair **DAT1+/DAT1-** transmits the 8-bit green pixel data during active video.

#### *7.17.6.4 DAT2+/DAT2-*

The differential signal pair **DAT2+/DAT2-** transmits the 8-bit red pixel data during active.

#### *7.17.6.5 TXC+/TXC-*

The differential signal pair **TXC+/TXC-** transmits the differential clock from the TFP410.

#### *7.17.6.6 DDC Channel*

The **Display Data Channel** or **DDC (**sometimes referred to as EDID Enhanced Display ID**)** is a digital connection between a computer display and the processor that allows the display specifications to be read by the processor. The standard was created by the Video Electronics Standards Association (VESA). The current version of DDC, called DDC2B, is based on the I²C bus. The monitor contains EEPROM programmed by the manufacturer with information about the graphics modes that the monitor can display. This interface in the LCD panel is powered by the +5V pin on the connector through **RT1**, a resetable fuse. As the processor is 1.8V I/O, the I2C bus is level translated by **U11**, a **TXS0102**. It provides for a split rail to allow the signals to interface on both sides of the circuit. Inside of **TXS0102** is a pullup on each signal, removing the need for an external resistor.

#### *7.17.6.7 HDMI Support*

The digital portion of the DVI-D interface is compatible with HDMI and is electrically the same. A standard HDMI cable may be used to connect to the HDMI input of monitors or televisions. Whether or not the Beagle will support those monitors is dependent on the timings that are used on the BeagleBoard and those that are accepted by the monitor. This may require a change in the software running on the Beagle. The audio and encryption features of HDMI are not supported by the BeagleBoard.

#### *7.17.6.8 DVI to VGA*

The analog portion of DVI, which provides RGB analog signals, is **not supported** by the BeagleBoard. Buying a DVI to VGA adapter connector will not work on a VGA display. You will need an active DVI-D to VGA adapter. Another option for these signals is to buy a board that connects to the J4 and J5 expansion connectors and generates the RGB signals for the VGA display.

## 7.18 LCD Expansion Headers

Access is provided on the -XM Rev A to allow access to the LCD signals. **Table 16** shows the signals that are on the P11 connector. You will notice that the signals are not in a logical order or grouping. This is due to the routing on the PCB where we allowed the routing to take precedence to get it to route with no addition of layers to the design.

**Table 16. P11 LCD Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | DC_5V | PWR | DC rail from the Main DC supply |
| 2 | DC_5V | PWR | DC rail from the Main DC supply |
| 3 | DVI_DATA1 | O | LCD Pixel Data bit |
| 4 | DVI_DATA0 | O | LCD Pixel Data bit |
| 5 | DVI_DATA3 | O | LCD Pixel Data bit |
| 6 | DVI_DATA2 | O | LCD Pixel Data bit |
| 7 | DVI_DATA5 | O | LCD Pixel Data bit |
| 8 | DVI_DATA4 | O | LCD Pixel Data bit |
| 9 | DVI_DATA12 | O | LCD Pixel Data bit |
| 10 | DVI_DATA10 | O | LCD Pixel Data bit |
| 11 | DVI_DATA23 | O | LCD Pixel Data bit |
| 12 | DVI_DATA14 | O | LCD Pixel Data bit |
| 13 | DVI_DATA19 | O | LCD Pixel Data bit |
| 14 | DVI_DATA22 | O | LCD Pixel Data bit |
| 15 | I2C3_SDA | I/O | I2C3 Data Line |
| 16 | DVI_DATA11 | O | LCD Pixel Data bit |
| 17 | DVI_VSYNC | O | LCD Vertical Sync Signal |
| 18 | DVI_PUP | O | Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired. |
| 19 | GND | PWR | Ground bus |
| 20 | GND | PWR | Ground bus |

The current available on the DC_5V rail is limited to the available current that remains from the DC supply that is connected to the DC power jack on the board. Keep in mind that some of that power is needed by the USB Host power rail and if more power is needed for the expansion board, the main DC power supply current capability may need to be increased. All signals are 1.8V except the DVI_PUP which is a 3.3V signal.

**Table 17** shows the signals that are on connector P13.

**Table 17. P13 LCD Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | 3.3V | PWR | 3.3V reference rail |
| 2 | VIO_1V8 | PWR | 1.8V buffer reference rail. |
| 3 | DVI_DATA20 | O | LCD Pixel Data bit |
| 4 | DVI_DATA21 | O | LCD Pixel Data bit |
| 5 | DVI_DATA17 | O | LCD Pixel Data bit |
| 6 | DVI_DATA18 | O | LCD Pixel Data bit |
| 7 | DVI_DATA15 | O | LCD Pixel Data bit |
| 8 | DVI_DATA16 | O | LCD Pixel Data bit |
| 9 | DVI_DATA7 | O | LCD Pixel Data bit |
| 10 | DVI_DATA13 | O | LCD Pixel Data bit |
| 11 | DVI_DATA8 | O | LCD Pixel Data bit |
| 12 | nUSB_PWR | O | LO indicates power is from the USB port. HI indicates that power is from the DC jack. |
| 13 | DVI_DATA9 | | LCD Pixel Data bit |
| 14 | I2C3_SCL | I/O | I2C3 Clock Line |
| 15 | DVI_DATA6 | O | LCD Pixel Data bit |
| 16 | DVI_CLK+ | O | DVI Clock |
| 17 | DVI_DEN | O | Data Enable |
| 18 | DVI_HSYNC | O | Horizontal Sync |
| 19 | GND | PWR | Ground bus |
| 20 | GND | PWR | Ground bus |

The 1.8V rail is for level translation only and should not be used to power circuitry on the board. The 3.3V rail also has limited capacity on the power as well. If the **TFP410** is disabled on the Beagle, then 80mA is freed up for use on an adapter card connected to the LCD signals connectors. It is not required that the **TFP410** be disabled when running an adapter card, but the power should be taken into consideration when making this decision.

It is suggested that the 5V rail be used to generate the required voltages for an adapter card.

## 7.19 S-Video

A single S-Video port is provided on the BeagleBoard. **Figure 45** is the design of the S-Video interface.

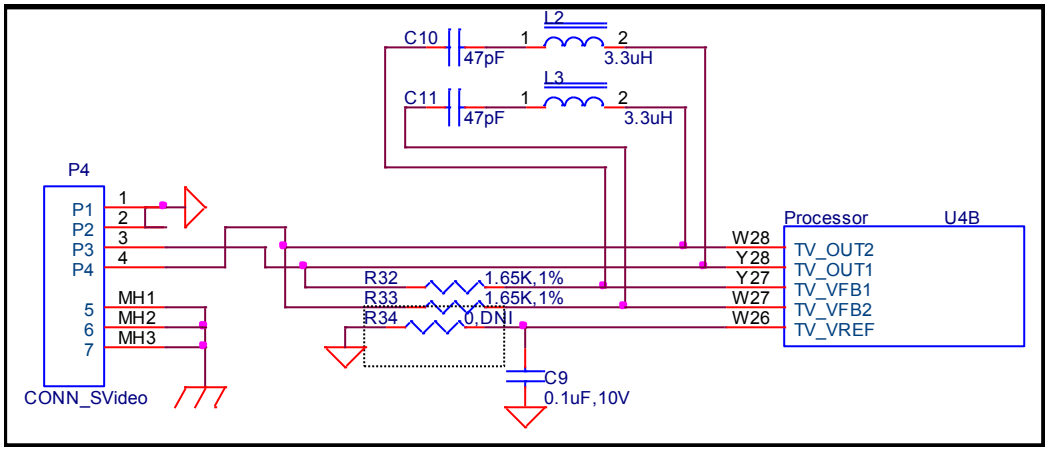



**Figure 45. S-Video Interface**

**Table 18** is the list of the signals on the S-Video interface and their definitions.

**Table 18. S-Video Interface Signals**

| Signal | I/O | Description |
|---|---|---|
| tv_out1 | O | TV analog output composite |
| tv_out2 | O | TV analog output S-VIDEO |
| tv_vref | I | Reference output voltage from internal bandgap |
| tv_vfb1 | O | Amplifier feedback node |
| tv_vfb2 | O | Amplifier feedback node |

Power to the internal DAC is supplied by the **TPS65950** via the **VDAC_1V8** rail. **Figure 37** reflects the filtering that is used on these rails, including the input VBAT rail.
A **47pf** CAP and **3.3uh** inductor are across the feedback resistors to improve the quality of the S-Video signal.

## 7.20 Camera Port

A new addition to the –xM is the camera port. This camera port uses the native camera interface of the processor. The connector configuration is designed to be compatible with the camera modules from Leopard Imaging. USB cameras may also be used if desired, but this interface has many HW assisted features and can support camera modules from VGA to 5MP resolutions. **Figure 46** is the Camera interface design.

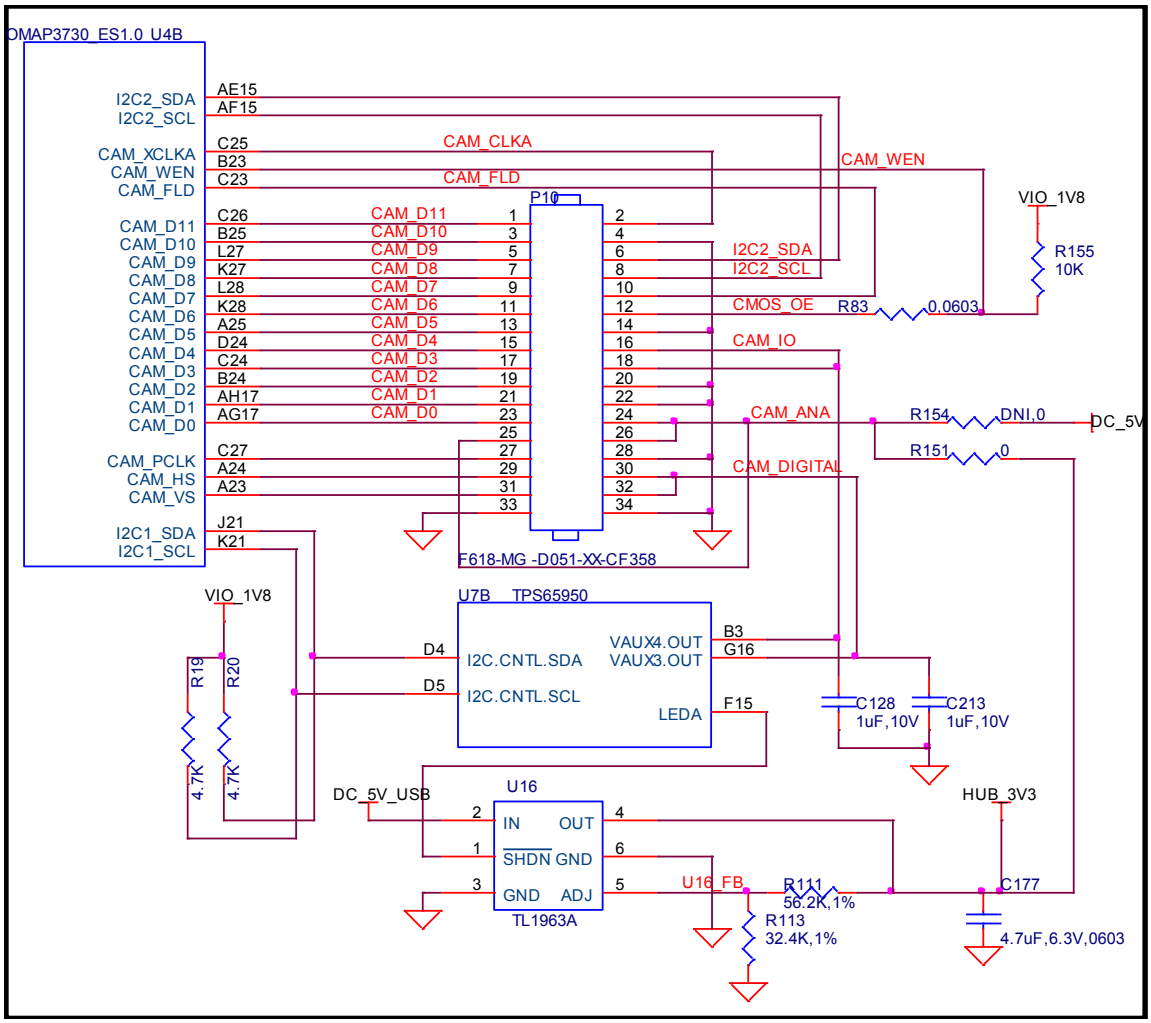



**Figure 46. Camera Port Interface**

The design of the camera interface is described in more detail in the remainder of this section.

### 7.20.1 Camera Power

There are three main power sources required by the camera module. Each of these are described in the following sections.

#### *7.20.1.1 CAM_ANA Power*

The DC input can be either 5V or 3.3V. It is selected by installing either **R151** or **R154**. The default is set at 3.3V and is controlled by turning on and off the USB HUB power rail at **U16**. The power is controlled by setting the **LEDA** signal on the **TPS65950**. Access to this register is via the **I2C1** interface on the processor.

The **5V** is on whenever a power source is applied to the board and cannot be controlled. This makes the 3.3V rail more suitable as it allows you to totally remove the power form the camera module.

#### *7.20.1.2 CAM_DIGITAL Power*

The digital power is a 1.8V rail that is supplied by the **TPS65950**. The power is controlled via the **I2C1** interface from the processor by setting the **VAUX3** regulator to 1.8V. This is used for the internal logic in the camera module.

#### *7.20.1.3 CAM_IO Power*

The I/O power is a 1.8V rail that is supplied by the **TPS65950**. The power is controlled via the **I2C1** interface from the processor by setting the **VAUX4** regulator to 1.8V. This will set the level of all of the interface signals to the processor. If this rail is set to a voltage higher than 1.8V, it will damage the processor if the camera module is inserted.

### 7.20.2 Camera I2C Port

The processor uses the **I2C2** port to communicate to the camera module to set the registers in the device. There are no pullups on the board for the I2C to prevent conflict with add on boards that do have the pullups. If an add-on board is not used, the SW will need to enable the internal pullups on the I2C2 signals in order for the interface to work.

### 7.20.3 Processor Camera Port Interface

**Table 19** shows the signals that are the interface between the processor and the camera modules. The I/O status of each pin is defined from the perspective of the processor.

The **cam_wen** signal is labeled as CMOS_OE on the schematic. All of the current camera modules do not use this signal and this signal has no affect on the operation of the camera modules. It is provided for future use.

**Table 19. Camera Interface Signals**

| Signal | Function | Description | I/O | Processor |
|---|---|---|---|---|
| cam_hs | HS | Camera Horizontal Synchronization | I/O | A24 |
| cam_vs | VS | Camera Vertical Synchronization | I/O | C25 |
| cam_xclka | Clock | Camera Clock Output | O | |
| cam_d0 | Camera Data | Camera image data bit 0 | I | AG17 |
| cam_d1 | Camera Data | Camera image data bit 1 | I | AH17 |
| cam_d2 | Camera Data | Camera image data bit 2 | I | B24 |
| cam_d3 | Camera Data | Camera image data bit 3 | I | C24 |

| | | | | |
|---|---|---|---|---|
| cam_d4 | Camera Data | Camera image data bit 4 | I | D24 |
| cam_d5 | Camera Data | Camera image data bit 5 | I | A25 |
| cam_d6 | Camera Data | Camera image data bit 6 | I | K28 |
| cam_d7 | Camera Data | Camera image data bit 7 | I | L28 |
| cam_d8 | Camera Data | Camera image data bit 8 | I | K27 |
| cam_d9 | Camera Data | Camera image data bit 9 | I | L27 |
| cam_d10 | Camera Data | Camera image data bit 10 | I | B25 |
| cam_d11 | Camera Data | Camera image data bit 11 | I | C26 |
| cam_fld | RESET | Camera field identification | I/O | C23 |
| cam_pclk | Pixel Clock | Camera pixel clock | I | C27 |
| cam_wen | | Camera Write Enable | I | B23 |

The **cam_fld** signal is used as a RESET signal to the camera board. When used as a reset, the pin should be set up as a GPIO pin.

**Table 20** shows the mapping of the pins on the camera sensors to the pins on the processor. In order to work with the different modules, you must take into account the order of the bits. The table covers the currently available camera modules that are compatible with the Beagle –xM. You will notice some of the lettering in red. These are signals that are not used by the camera module. In order for the data to be correct, these signals need to be tied low by enabling the internal pulldown resistors.

**Table 20. Camera Pin Signal Mapping**

| Resolution | | | VGA | 1.3MP | 2MP | 3MP | 5MP |
|---|---|---|---|---|---|---|---|
| Camera Module Part Number | | | LI-LBCMVGA | LI-LBCM1M1 | LI-LBCM2M1 | LI-BCM3M1 | LI-LBCM5M1 |
| Data Width---> | | | 10 | 10 | 10 | 8 | 12 |
| PIN | NAME | I/O/V | | | | | |
| 1 | D11 | I | D9 | D9 | D9 | D7 | D11 |
| 2 | MCLK | O | MCLK | MCLK | MCLK | MCLK | MCLK |
| 3 | D10 | I | D8 | D8 | D8 | D6 | D10 |
| 4 | GND | PWR | GND | GND | GND | GND | GND |
| 5 | D9 | I | D7 | D7 | D7 | D5 | D9 |
| 6 | SDATA | I/O | SDATA | SDATA | SDATA | SDATA | SDATA |
| 7 | D8 | I | D6 | D6 | D6 | D4 | D8 |
| 8 | SCLK | I/O | SCLK | SCLK | SCLK | SCLK | SCLK |
| 9 | D7 | I | D5 | D5 | D5 | D3 | D7 |
| 10 | RESET | O | RESET | RESET | RESET | RESET | RESET |
| 11 | D6 | I | D4 | D4 | D4 | D2 | D6 |
| 12 | OE | O | OE | OE | OE | OE | OE |
| 13 | D5 | I | D3 | D3 | D3 | D1 | D5 |
| 14 | GND | PWR | GND | GND | GND | GND | GND |
| 15 | D4 | I | D2 | D2 | D2 | D0 | D4 |
| 16 | CAM_IO | PWR | CAM_IO | CAM_IO | CAM_IO | CAM_IO | CAM_IO |
| 17 | D3 | I | D1 | D1 | D1 | PULL-DOWN | D3 |
| 18 | CAM_IO | PWR | CAM_IO | CAM_IO | CAM_IO | CAM_IO | CAM_IO |
| 19 | D2 | I | D0 | D0 | D0 | PULL-DOWN | D2 |
| 20 | GND | PWR | GND | GND | GND | GND | GND |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **21** | D1 | I | PULL-DOWN | PULL-DOWN | PULL-DOWN | PULL-DOWN | D1 |
| **22** | GND | PWR | GND | GND | GND | GND | GND |
| **23** | D0 | I | PULL-DOWN | PULL-DOWN | PULL-DOWN | PULL-DOWN | D0 |
| **24** | CAM_ANA | PWR | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA |
| **25** | CAM_ANA | PWR | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA |
| **26** | CAM_ANA | PWR | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA | CAM_ANA |
| **27** | PCLK | I | PCLK | PCLK | PCLK | PCLK | PCLK |
| **28** | GND | PWR | GND | GND | GND | GND | GND |
| **29** | HS | I | HS | HS | HS | HS | HS |
| **30** | CAM_DIG | PWR | CAM_DIG | CAM_DIG | CAM_DIG | CAM_DIG | CAM_DIG |
| **31** | VS | I | VS | VS | VS | VS | VS |
| **32** | CAM_DIG | PWR | CAM_DIG | CAM_DIG | CAM_DIG | CAM_DIG | CAM_DIG |
| **33** | GND | PWR | GND | GND | GND | GND | GND |
| **34** | GND | PWR | GND | GND | GND | GND | GND |

### 7.20.4 Camera Modules

The camera module can be purchased from Leopard Imaging or one of their distributors. It uses the same modules as the LeopardBoard DM355 version. The figure below shows the different modules that can be used. The part numbers can be found in **Table 20**.

**Figure 47. Camera Modules**

At this time, only the VGA camera board has been confirmed to work on the –xM board. Other boards will be added as the SW drivers are completed. The 3MP module is next on the list. It is expected that all of the listed modules will work and no complications are expected as they are all compatible at the hardware level.

## 7.21 RS232 Port

A single RS232 port is provided on the BeagleBoard and provides access to the TX and RX lines of **UART3** on the processor. **Figure 48** shows the design of the RS232 port.

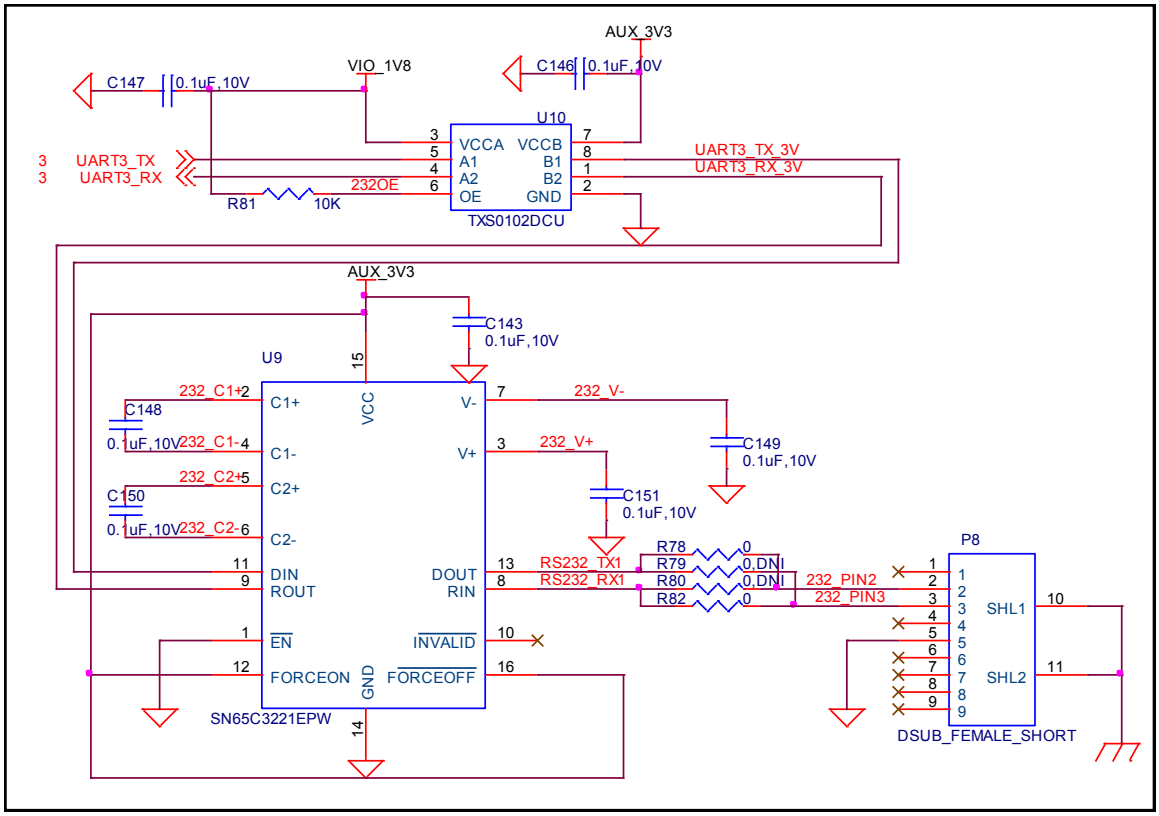



**Figure 48. RS232 Interface Design**

### 7.21.1 Processor Interface

Two lines, **UART3_Tx** and **UART3_Rx**, are provided by the processor. The **UART3** function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate and also supports auto bauding.

### 7.21.2 Level Translator

All of the I/O levels from the processor are **1.8V** while the transceiver used runs at 3.3V. This requires that the voltage levels be translated. This is accomplished by the **TXS0102** which is a two-bit noninverting translator that uses two separate configurable power-supply rails. The A port tracks VCCA, 1.8V and the B port tracks VCCB, 3.3V. This allows for low-voltage bidirectional translation between the two voltage nodes. When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. In this design, the OE is tied high via a 10K ohm resistor to insure that it is always on.

#### 7.21.3 RS232 Transceiver

The RS232 transceiver used is the **SN65C322** which consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The **SN65C3221** operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ms to 150 V/ms. While the processor can easily drive a 1Mbit/S rate, your results may vary based on cabling, distance, and the loads and drive capability on the other end of the RS232 port.

The transceiver is powered from the 3.3V rail and is active at power up. This allows the port to be used for UART based peripheral booting over the port.

#### 7.21.4 Connector

Access to the RS232 port is through a 9 pin DB9 connector, **P9**. This is new on the –xM version and replaces the 10 pin header. A standard male to female straight DB9 cable can be used or a USB to DB9 adapter can be plugged direct into the board.

### 7.22 Indicators

There are five green indicators on the BeagleBoard:

- Power
- PMU_STAT
- USER0
- USER1
- HUB Power

All of the green LEDs are programmable under software control. **Figure 49** shows the connection of all of these indicators.

There is also a single RED LED on the board. Turning on this LED is not something that a person should try to do as it indicates that the user is not paying attention and has plugged in a potentially damaging power supply into the power jack.

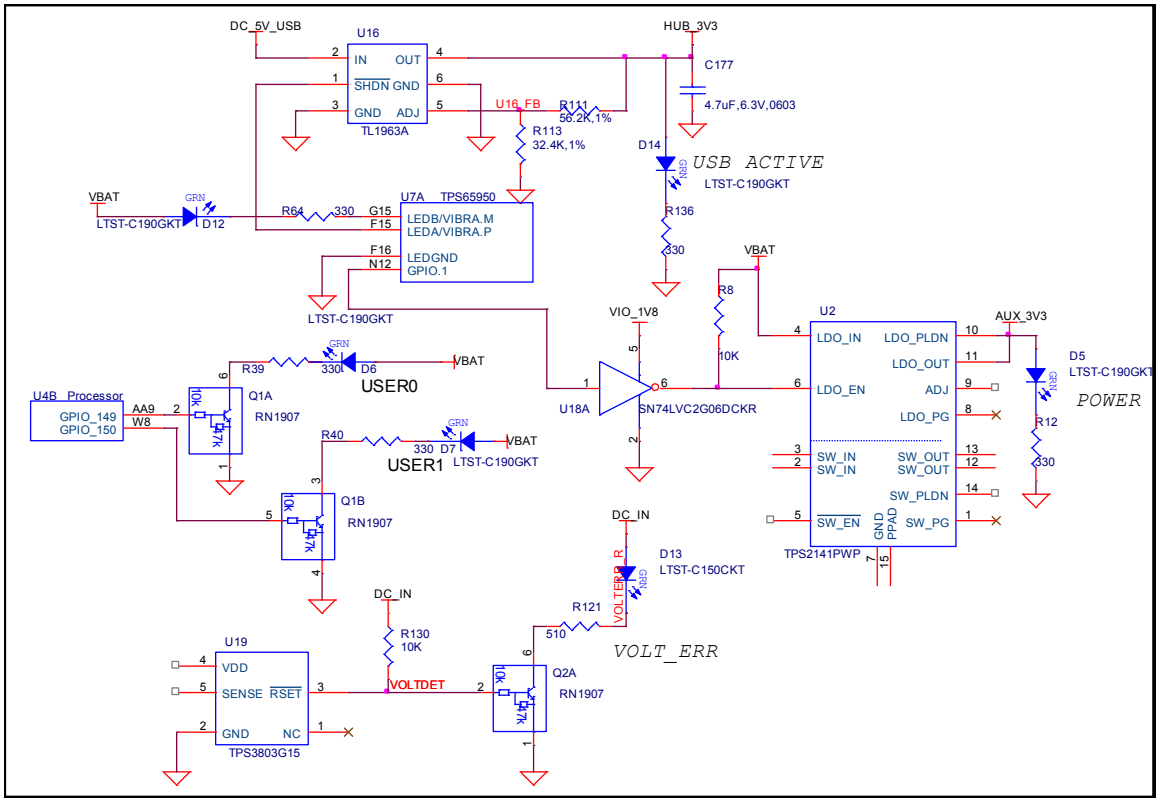



**Figure 49. Indicator Design**

### 7.22.1 Power Indicator

This indicator, **D5**, connects from the **3.3V** rail supply and ground. It indicates that the entire power path is supplying the power to the board. Indicator **D5** does not indicate which power source is being used to supply the main power to the board but only that it is active. Software does have the ability to turn off this regulator and thereby turning off the LED. By default this is always disabled on power up.

### 7.22.2 PMU Status Indicator

This output is driven from the **TPS65950** using the **LED.B** output. The **TPS65950** provides LED driver circuitry to power two LED circuits that can provide user indicators. The first circuit can provide up to 160 mA and the second, 50 mA. Each LED circuit is independently controllable for basic power (on/off) control and illumination level (using PWM). The second driver, **LED.B**, is used to drive the LED that is connected to the VBAT rail through a resistor.

The PWM inside the **TPS65950** can be used to alter the brightness of the LED if desired or it can be turned on or off by the processor using the I2C bus. The PWM is programmable, register-controlled, duty cycle based on a nominal 4-Hz cycle which is derived from an internal 32-kHz clock. It is possible to set the LED to flash automatically without software control if desired.

### 7.22.3 User Indicators

There are two user LEDs, **D6** and **D7**, that can be driven directly from a GPIO pin on the processor. These can be used for any purpose by the software. The output level of the processor is 1.8V and the current sink capability is not enough to drive an LED with any level of brightness. A transistor pair, **RN1907** is used to drive the LEDs from the **VBAT** rail. A logic level of 1 will turn the LED on.

### 7.22.4 HUB Power Indicator

The HUB power LED, **D14**, is turned on whenever the USB HUB power is active. This output is driven from the **TPS65950** using the **LED.**A output. The processor can control the LED by communicating via the I2C to the **TPS65950**.

### 7.22.5 Overvoltage Indicators

The Over Voltage LED, **D13**, turns on whenever the DC voltage exceeds 5.3V. The detection circuit, **TPS3803,** turns on the LED.

## 7.23 JTAG

A JTAG header is provided to allow for advanced debugging on the BeagleBoard by using a JTAG based debugger. **Figure 50** shows the interconnection to the processor.

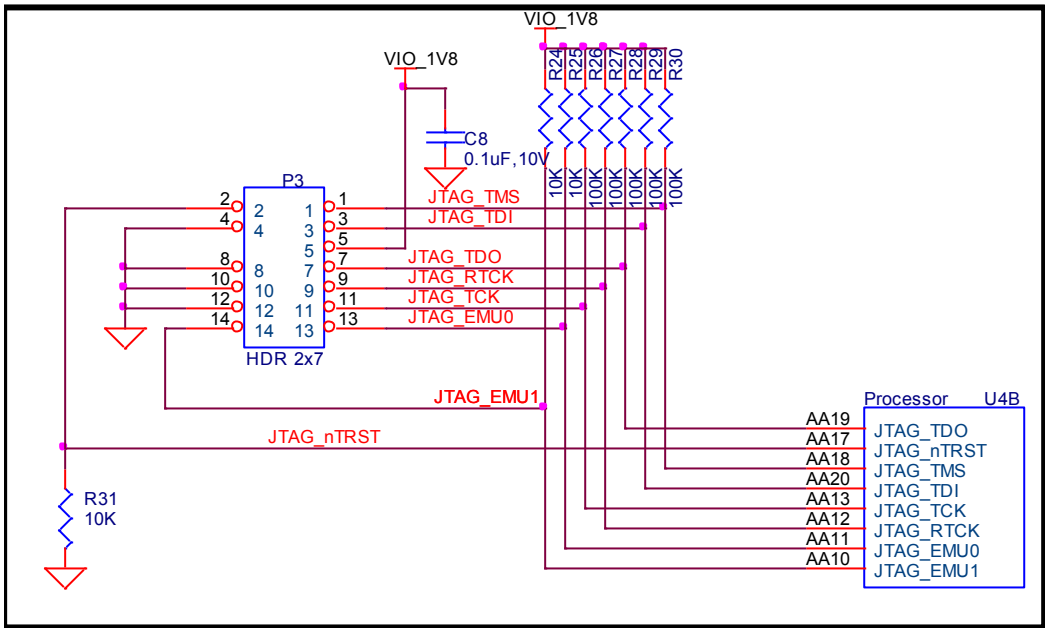



**Figure 50. JTAG Interface**

### 7.23.1 Processor Interface

The JTAG interface connects directly to the OMAP processor. All signals are a 1.8V level. **Table 21** describes the signals on the JTAG connector.

**Table 21. JTAG Signals**

| Signal | Description | I/O |
|---|---|---|
| JTAG_TMS | Test mode select | I/O |
| JTAG_TDI | Test data input | I |
| JTAG_TDO | Test Data Output | O |
| JTAG_RTCK | ARM Clock Emulation | O |
| JTAG_TCK | Test Clock | I |
| JTAG_nTRST | Test reset | I |
| JTAG_EMU0 | Test emulation 0 | I/O |
| JTAG_EMU1 | Test emulation 1 | I/O |

### 7.23.2 JTAG Connector

The JTAG interface uses a 14 pin connector. All JTAG emulator modules should be able to support this interface. Contact your emulator supplier for further information or if an adapter is needed.

## 7.24 Main Expansion Header

The expansion header is provided to allow a limited number of functions to be added to the BeagleBoard via the addition of a daughtercard.

**Figure 51** is the design of the expansion connector and the interfaces to the processor.

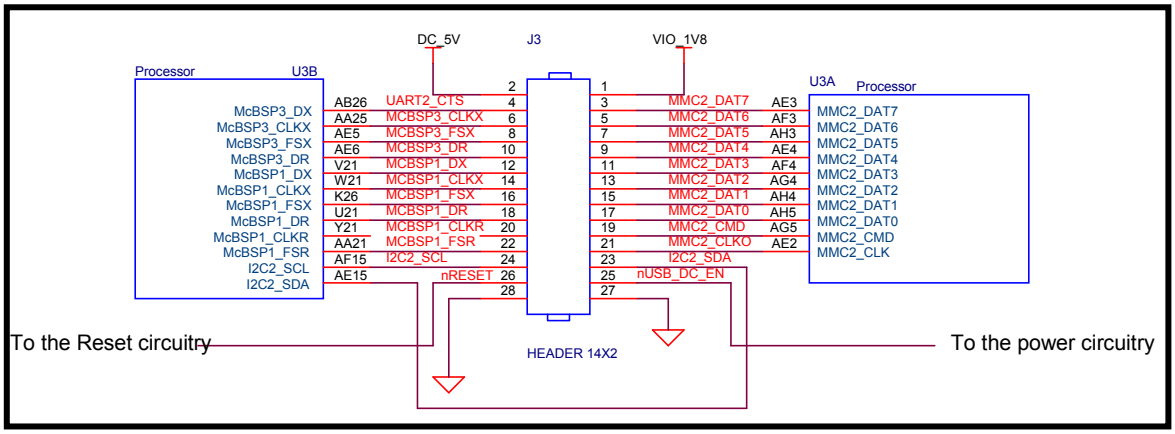



**Figure 51. Main Expansion Header Processor Connections**

**CAUTION:** The voltage levels on the expansion header are 1.8V. Exposure of these signals to a higher voltage will result in damage to the board and a voiding of the warranty.

### 7.24.1 Processor Interface

The main purpose of the expansion connector is to route additional signals from the processor. **Table 22** shows all of the signals that are on the expansion header. As the processor has a multiplexing feature, multiple signals can be connected to certain pins to add additional options as it pertains to the signal available. Each pin can be set individually for a different mux mode. This allows any of the listed mux modes to be set on a pin by pin basis by writing to the pin mux register in software. Following is the legend for **Table 22**.

**X**= there is no signal connected when this mode is selected

**Z**= this is the safe mode meaning neither input to output. This is the default mode on power up.

***=** this indicates that there is a signal connected when this mode is selected, but it has no useful purpose without other pins being available. Access to these other pins is not provided on the expansion connector.

The first column is the pin number of the expansion connector.

The second column is the pin number of the processor.

The columns labeled 0-7 represent each of the pin mux modes for that pin. By setting this value in the control register, this signal will be routed to the corresponding pin of the expansion connector. These setting are on a pin by pin basis. Any pin can be set with the mux register setting, and the applicable signal will be routed to the pin on the expansion connector.

**Table 22. Expansion Connector Signals**

| EXP | Processor | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | | VIO_1V8 | | | | | | | |
| 2 | | DC_5V | | | | | | | |
| 3 | AE3 | MMC2_DAT7 | * | * | * | GPIO_139 | * | * | Z |
| 4 | AB26 | UART2_CTS | McBSP3_DX | GPT9_PWMEVT | X | GPIO_144 | X | X | Z |
| 5 | AF3 | MMC2_DAT6 | * | * | * | GPIO_138 | * | X | Z |
| 6 | AA25 | UART2_TX | McBSP3_CLKX | GPT11_PWMEVT | X | GPIO_146 | X | X | Z |
| 7 | AH3 | MMC2_DAT5 | * | * | * | GPIO_137 | * | X | Z |
| 8 | AE5 | McBSP3_FSX | UART2_RX | X | X | GPIO_143 | * | X | Z |
| 9 | AE4 | MMC2_DAT4 | * | X | * | GPIO_136 | X | X | Z |
| 10 | AB25 | UART2_RTS | McBSP3_DR | GPT10_PWMEVT | X | GPIO_145 | X | X | Z |
| 11 | AF4 | MMC2_DAT3 | McSPI3_CS0 | X | X | GPIO_135 | X | X | Z |
| 12 | V21 | McBSP1_DX | McSPI4_SIMO | McBSP3_DX | X | GPIO_158 | X | X | Z |
| 13 | AG4 | MMC2_DAT2 | McSPI3_CS1 | X | X | GPIO_134 | X | X | Z |
| 14 | W21 | McBSP1_CLKX | X | McBSP3_CLKX | X | GPIO_162 | X | X | Z |
| 15 | AH4 | MMC2_DAT1 | X | X | X | GPIO_133 | X | X | Z |
| 16 | K26 | McBSP1_FSX | McSPI4_CS0 | McBSP3_FSX | x | GPIO_161 | X | X | Z |
| 17 | AH5 | MMC2_DAT0 | McSPI3_SOMI | X | X | GPIO_132 | X | X | Z |
| 18 | U21 | McBSP1_DR | McSPI4_SOMI | McBSP3_DR | X | GPIO_159 | X | X | Z |
| 19 | AG5 | MMC2_CMD | McSPI3_SIMO | X | X | GPIO_131 | X | X | Z |
| 20 | Y21 | McBSP1_CLKR | McSPI4_CLK | X | X | GPIO_156 | X | X | Z |
| 21 | AE2 | MMC2_CLKO | McSPI3_CLK | X | X | GPIO_130 | X | X | Z |
| 22 | AA21 | McBSP1_FSR | X | * | Z | GPIO_157 | X | X | Z |
| 23 | AE15 | I2C2_SDA | X | X | X | GPIO_183 | X | X | Z |
| 24 | AF15 | I2C2_SCL | X | X | X | GPIO_168 | X | X | Z |
| 25 | 25 | REGEN | | | | | | | |
| 26 | 26 | Nreset | | | | | | | |
| 27 | 27 | GND | | | | | | | |
| 28 | 28 | GND | | | | | | | |

### 7.24.2 Expansion Signals

This section provides more detail on each of the signals available on the expansion connector. They are grouped by functions in **Table 23** along with a description of each signal and the MUX setting to activate the pin. If you use these signals in their respective groups and that is the only function you use, all of the signals are available. Whether or not the signals you need are all available, depends on the muxing function on a per-pin basis. Only one signal per pin is available at any one time.

## Table 23. Expansion Connector Signal Groups

| Signal | Description | I/O | EXP | OMAP | Mux |
|---|---|---|---|---|---|
| **SD/MMC Port 2** | | | | | |
| MMC2_DAT7 | SD/MMC data pin 7. | I/O | 3 | AE3 | 1 |
| MMC2_DAT6 | SD/MMC data pin 6. | I/O | 5 | AF3 | 1 |
| MMC2_DAT5 | SD/MMC data pin 5. | I/O | 7 | AH3 | 1 |
| MMC2_DAT4 | SD/MMC data pin 4. | I/O | 9 | AE4 | 1 |
| MMC2_DAT3 | SD/MMC data pin 3. | I/O | 11 | AF4 | 1 |
| MMC2_DAT2 | SD/MMC data pin 2. | I/O | 13 | AG4 | 1 |
| MMC2_DAT1 | SD/MMC data pin 1. | I/O | 15 | AH4 | 1 |
| MMC2_DAT0 | SD/MMC data pin 0. | I/O | 17 | AH5 | 1 |
| MMC2_CMD | SD/MMC command signal. | I/O | 19 | AG5 | 1 |
| MMC_CLKO | SD/MMC clock signal. | O | 21 | AE2 | 1 |
| **McBSP Port 1** | | | | | |
| McBSP1_DR | Multi channel buffered serial port receive | I | 18 | | |
| McBSP1_CLKS | ---------- | N/A | N/A | | |
| McBSP1_FSR | Multi channel buffered serial port transmit frame sync RCV | I/O | 22 | | |
| McBSP1_DX | Multi channel buffered serial port transmit | I/O | 12 | | |
| McBSP1_CLKX | Multi channel buffered serial port transmit clock | I/O | 14 | | |
| McBSP1_FSX | Multi channel buffered serial port transmit frame sync XMT | I/O | 16 | | |
| McBSP1_CLKR | Multi channel buffered serial port receive clock | I/O | 20 | | |
| **I2C Port 2** | | | | | |
| I2C2_SDA | I2C data line. | IOD | 23 | | |
| I2C2_SCL | I2C clock line | IOD | 24 | | |
| **McBSP Port 3** | | | | | |
| McBSP3_DR | Multi channel buffered serial port receive | I | 10,18 | | |
| McBSP3_DX | Multi channel buffered serial port transmit | I/O | 4,12 | | |
| McBSP3_CLKX | Multi channel buffered serial port receive clock | I/O | 6,14 | | |
| McBSP3_FSX | Multi channel buffered serial port frame sync transmit | I/O | 8,16 | | |
| **General Purpose I/O Pins** | | | | | |
| GPIO_130 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 21 | | |
| GPIO_131 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 19 | | |
| GPIO_132 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 17 | | |
| GPIO_133 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 15 | | |
| GPIO_134 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 13 | | |
| GPIO_135 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 11 | | |
| GPIO_136 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 9 | | |
| GPIO_137 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 7 | | |
| GPIO_138 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 5 | | |
| GPIO_139 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 3 | | |
| GPIO_143 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 8 | | |
| GPIO_144 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 4 | | |
| GPIO_145 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 10 | | |
| GPIO_146 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 6 | | |
| GPIO_156 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 20 | | |
| GPIO_158 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 12 | | |
| GPIO_159 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 18 | | |
| GPIO_161 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 16 | | |
| GPIO_162 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 14 | | |
| GPIO_168 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 24 | | |
| GPIO_183 | GP Input/Output pin. Can be used as an interrupt pin. | I/O | 23 | | |
| **McSPI Port 3** | | | | | |
| McSPI3_CS0 | Multi channel SPI chip select 0 | O | 11 | | |
| McSPI3_CS1 | Multi channel SPI chip select 1 | O | 13 | | |
| McSPI3_SIMO | Multi channel SPI slave in master out | I/O | 19 | | |
| McSPI3_SOMI | Multi channel SPI slave out master in | I/O | 17 | | |
| McSPI3_CLK | Multi channel SPI clock | I/O | 21 | | |
| McSPI Port 4 | | | | | |
| McSPI4_SIMO | Multi channel SPI slave in master out | I/O | 12 | | |
| McSPI4_SOMI | Multi channel SPI slave out master in | I/) | 18 | | |
| McSPI4_CS0 | Multi channel SPI chip select 0 | O | 16 | | |
| McSPI4_CLK | Multi channel SPI clock | I/O | 20 | | |
| UART Port 2 | | | | | |
| UART2_CTS | UART clear to send. | I/O | 4 | | |
| UART2_RTS | UART request to send | O | 10 | | |

| | | | | | |
|---|---|---|---|---|---|
| UART2_RX | UART receive | I | 8 | | |
| UART2_TX | UART transmit | O | 6 | | |
| GPT PWM | | | | | |
| GPT9_PWMEVT | PWM or event for GP timer 9 | O | 4 | | |
| GPT11_PWMEVT | PWM or event for GP timer 11 | O | 10 | | |
| GPT10_PWMEVT | PWM or event for GP timer 10 | O | 8 | | |

### 7.24.3 Power

The expansion connector provides two power rails. The first is the **VIO_1.8V** rail which is supplied by the **TPS65950**. This rail is limited in the current it can supply from the **TPS65950** and what remains from the current consumed by the BeagleBoard and is intended to be used to provide a rail for voltage level conversion only. It is not intended to power a lot of circuitry on the expansion board. All signals from the BeagleBoard are at 1.8V.

The other rail is the **DC_5V**. The same restriction exits on this rail as mentioned in the USB section. The amount of available power to an expansion board depends on the available power from the DC supply or the USB supply from the PC.

### 7.24.4 Reset

The **nRESET** signal is the main board reset signal. When the board powers up, this signal will act as an input to reset circuitry on the expansion board. After power up, a system reset can be generated by the expansion board by taking this signal low. This signal is a 1.8V level signal.

### 7.24.5 Power Control

There is an additional open-drain signal on the connector called **REGEN**. The purpose of this signal is to provide a means to control power circuitry on the expansion card to turn on and off the voltages. This insures that the power on the expansion board is turned on at the appropriate time. Depending on what circuitry is provided on the expansion board, an additional delay may be needed to be added before the circuitry is activated. Refer to the processor and **TPS65950** documentation for more information.

## 7.25 LCD Expansion Header

If you choose not to use the LCD headers for access to the LCD signals or for the DVI-D interface, they can also be used for other functions on the board based on the pin mux setting of each pin. **Table 24** shows the options for **P11** and **Table 25** shows the options for **P135**. The MUX: column indicates which MUX mode must be set for each pin to make the respective signals accessible on the pins of the processor.

**Table 24. P11 GPIO Signals**

| Pin# | Signal | MUX:0 | MUX:2 | MUX:4 |
|---|---|---|---|---|
| 3 | DVI_DATA1 | DATA1 | UART1_RTS | GPIO71 |
| 4 | DVI_DATA0 | DATA0 | UART1_CTS | GPIO70 |
| 5 | DVI_DATA3 | DATA3 | - | GPIO73 |
| 6 | DVI_DATA2 | DATA2 | - | GPIO72 |
| 7 | DVI_DATA5 | DATA5 | UART3_TX | GPIO75 |
| 8 | DVI_DATA4 | DATA4 | UART3_RX | GPIO74 |
| 9 | DVI_DATA12 | DATA12 | | GPIO82 |
| 10 | DVI_DATA10 | DATA10 | - | GPIO79 |
| 11 | DVI_DATA23 | DATA23 | - | GPIO93 |
| 12 | DVI_DATA14 | DATA14 | - | GPIO84 |
| 13 | DVI_DATA19 | DATA19 | McSPI3_SIMO | GPIO89 |
| 14 | DVI_DATA22 | DATA22 | McSPI3_CS1 | GPIO92 |
| 15 | I2C3_SDA | I2C3_SDA | - | - |
| 16 | DVI_DATA11 | DATA11 | - | GPIO81 |
| 17 | DVI_VSYNC | VSYNC | - | GPIO68 |
| 18 | DVI_PUP | DVI_PUP | - | - |

**Table 25. P13 GPIO Signals**

| Pin# | Signal | MUX:0 | MUX:2 | MUX:4 |
|---|---|---|---|---|
| 3 | DVI_DATA20 | DATA20 | McSPI3_SOMI | GPIO90 |
| 4 | DVI_DATA21 | DATA21 | McSPI3_CS0 | GPIO91 |
| 5 | DVI_DATA17 | DATA17 | - | GPIO87 |
| 6 | DVI_DATA18 | DATA18 | McSPI3_CLK | GPIO88 |
| 7 | DVI_DATA15 | DATA15 | - | GPIO85 |
| 8 | DVI_DATA16 | DATA16 | - | GPIO86 |
| 9 | DVI_DATA7 | DATA7 | UART1_RX | GPIO77 |
| 10 | DVI_DATA13 | DATA13 | - | GPIO83 |
| 11 | DVI_DATA8 | DATA8 | - | GPIO78 |
| 12 | NC | - | - | - |
| 13 | DVI_DATA9 | DATA9 | - | GPIO79 |
| 14 | I2C3_SCL | I2C3_SCL | | - |
| 15 | DVI_DATA6 | DATA6 | UART1_TX | GPIO_76 |
| 16 | DVI_CLK+ | PCLK | - | GPIO66 |
| 17 | DVI_DEN | DEN | - | GPIO69 |
| 18 | DVI_HSYNC | HSYNC | - | GPIO67 |

## 7.26 Auxiliary Expansion Header

New to the –xM version is the addition of expansion header called the Auxiliary Expansion Header. As is the case with many of the signals on the various connectors, these pins have multiple functions mapped per pin. **Table 26** below is the pin out of the MMC Connector. In order to access other signals on these pins, the pin muxing register will need to be set as needed on a per pin basis.

**Table 26. P17 Auxiliary Expansion Signals**

| PIN | SIGNAL | PROC | 0 | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|---|
| 1 | | | VIO_1V8 | | | | | |
| 2 | | | VMMC2 | | | | | |
| 3 | MMC3_DAT2 | AF13 | ETK_D6 | MCBSP5_DX | MMC3_DAT2 | HSUSB1_D6 | GPIO_20 | |
| 4 | MMC3_DAT7 | AH14 | ETK_D7 | MCSPI3_CS1 | MMC3_DAT7 | HSUSB1_D3 | GPIO_21 | MM1_TXEN_N |
| 5 | MMC3_DAT3 | AE13 | ETK_D3 | MCSPI3_CLK | MMC3_DAT3 | HSUSB_D7 | GPIO_17 | |
| 6 | GPIO_16 | AH12 | ETK_D2 | MCSPI3_CS0 | | HSUSB1_D2 | GPIO_16 | MM1_TXDAT |
| 7 | GPIO_15 | AG12 | ETK_D1 | MCBSPI3_SOMI | | HSUSB1_D1 | GPIO_15 | MM1_TXSE0 |
| 8 | MMC3_DAT1 | AH9 | ETK_D5 | MCBSP5_FSX | MMC3_DAT1 | HSUSB1_D5 | GPIO_19 | |
| 9 | MMC3_DAT5 | AG9 | ETK_D9 | SERCURE_IND | MMC3_DAT5 | HSUSB1_NXT | GPIO_23 | MM1_RX |
| 10 | MMC3_DAT4 | AF11 | ETK_D0 | MCSPI3_SIMO | MMC3_DAT4 | HSUSB1_D0 | GPIO_14 | MM1_RXRCV |
| 11 | MMC3_DAT0 | AE11 | ETK_D4 | MCBSP5_DR | MMC3_DAT0 | HSUSB1_D4 | GPIO_18 | |
| 12 | MMC3_CMD | AE10 | ETK_CTL | | MMC3_CMD | HSUSB1_CLK | GPIO_13 | |
| 13 | MMC3_DAT6 | AF9 | ETK_D8 | DRM_SECURE | MMC3_DAT6 | HSUSB1_DIT | GPIO_22 | |
| 14 | MMC3_CLK | AF10- | ETK_CLK | MCBSP5_CLKX | MMC3_CLK | HSUSB1_STP | GPIO_12 | MM1_RXDP |
| 15 | HDQ | J25 | HDQ | SYS_ALTCLK | | | GPIO_170 | |
| 16 | DMAREQ3 | P8 | | DMAREQ3 | | GPT11_PWM | GPIO_57 | |
| 17 | AUX_DC | | AUX_ADC | | | | | |
| 18 | PWR_CNTRL | | PWR_CNTRL | | | | | |
| 19 | | | GND | | | | | |
| 20 | | | GND | | | | | |

The following sections provide a brief description of the functions of the pins available. For a more complete description, please refer to the datasheet or Technical Reference Manuals. Not all of these signals can be used at the same time. Only one signal can be used per pin at one time based on the setting of the pin mux registers in the processor. Make sure that you set the correct mux mode when using these signals for their various configurations.

### 7.26.1 MCBSP5 Signals

Access to McBSP5 is provided as an option on the connector. **Table 27** below shows the pins that the McBSP5 interface appears on. In order to access these signals, the mux mode for each pin must be set to 1.

**Table 27. P17 McBSP5 Expansion Signals**

| PIN | SIGNAL | I/O | DESCRIPTION | PROC PINS |
|---|---|---|---|---|
| **3** | MCBSP5_DX | O | Transmitted Data | AF13 |
| **8** | MCBSP5_FSX | O | Frame Sync | AH9 |
| **11** | MCBSP5_DR | I | Received Data | AE11 |
| **14** | MCBSP5_CLKX | O | Serial Clock | AF10- |

### 7.26.2 MMC3 Signals

These signals can be used to provide an additional SD/MMC interface on an expansion board. All of these signals are 1.8V, so if you plan to use the signals as an SD/MMC interface, then a level shifter will be required. In order to access these signals, they must be in Mux mode 2. **Table 28** is a description of these signals.

**Table 28. P17 MMC3 Expansion Signals**

| PIN | SIGNAL | I/O | PROC | DESCRIPTION |
|---|---|---|---|---|
| **3** | MMC3_DAT2 | I/O | AF13 | Bidirectional data pin. |
| **4** | MMC3_DAT7 | I/O | AH14 | Bidirectional data pin. |
| **5** | MMC3_DAT3 | I/O | AE13 | Bidirectional data pin. |
| **8** | MMC3_DAT1 | I/O | AH9 | Bidirectional data pin. |
| **9** | MMC3_DAT5 | I/O | AG9 | Bidirectional data pin. |
| **10** | MMC3_DAT4 | I/O | AF11 | Bidirectional data pin. |
| **11** | MMC3_DAT0 | I/O | AE11 | Bidirectional data pin. |
| **12** | MMC3_CMD | O | AE10 | Command indicator signal |
| **13** | MMC3_DAT6 | I/O | AF9 | Bidirectional data pin. |
| **14** | MMC3_CLK | O | AF10- | Clock |

This interface could also be used to communicate to an FPGA or a WLAN device that uses the SDIO style interface.

### 7.26.3 ETK Signals

The ETK signals can be used to provide additional debugging information. For more information on the use of these signals, please refer to the processor Technical reference Manual. **Table 29** has the signals for the ETK interface that are provided.

**Table 29. P17 Auxiliary ETK Signals**

| PIN | SIGNAL | I/O | PROC | DESCRIPTION |
|---|---|---|---|---|
| **3** | ETK_D6 | O | AF13 | Trace data pin. |
| **4** | ETK_D7 | O | AH14 | Trace data pin. |
| **5** | ETK_D3 | O | AE13 | Trace data pin. |
| **6** | ETK_D2 | O | AH12 | Trace data pin. |
| **7** | ETK_D1 | O | AG12 | Trace data pin. |
| **8** | ETK_D5 | O | AH9 | Trace data pin. |
| **9** | ETK_D9 | O | AG9 | Trace data pin. |
| **10** | ETK_D0 | O | AF11 | Trace data pin. |
| **11** | ETK_D4 | O | AE11 | Trace data pin. |
| **12** | ETK_CTL | O | AE10 | Trace control signal. |
| **13** | ETK_D8 | O | AF9 | Trace data pin. |
| **14** | ETK_CLK | O | AF10- | Trace clock. |

### 7.26.4 HSUSB1 Signals

These signals are the other High Speed USB port found on the processor. It is the same interface that is used to communicate to the UBS PHY on the board, but a different port. **Table 30** gives the signals that are used for this interface. In order for these pins to be used, the pin mux must be set to **Mode 3**.

**Table 30. P17 High Speed USB Expansion Signals**

| PIN | SIGNAL | I/0 | PROC | DESCRIPTION |
|---|---|---|---|---|
| **3** | HSUSB1_D6 | I/O | AF13 | Bidirectional Data |
| **4** | HSUSB1_D3 | I/O | AH14 | Bidirectional Data |
| **5** | HSUSB_D7 | I/O | AE13 | Bidirectional Data |
| **6** | HSUSB1_D2 | I/O | AH12 | Bidirectional Data |
| **7** | HSUSB1_D1 | I/O | AG12 | Bidirectional Data |
| **8** | HSUSB1_D5 | I/O | AH9 | Bidirectional Data |
| **9** | HSUSB1_NXT | I | AG9 | Next signal |
| **10** | HSUSB1_D0 | I/O | AF11 | Bidirectional Data |
| **11** | HSUSB1_D4 | I/O | AE11 | Bidirectional Data |
| **12** | HSUSB1_CLK | O | AE10 | 60MHZ Clock output |
| **13** | HSUSB1_DIR | I | AF9 | Data direction signal |
| **14** | HSUSB1_STP | O | AF10- | Stop signal |

### 7.26.5 Alternate Clock

The **SYS_ALTCLK** signal can be used to provide an alternate system clock into the processor. This can be used for things such as the GPTIMERS, USB, or as a clock for the NTSC/PAL S-Video output.

### 7.26.6 HDQ 1-Wire

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slaves (HDQ/1-Wire external compliant devices).

### 7.26.7 ADC

There is one A to D converter pin provided on the Auxiliary Expansion Header. This pin is labeled **AUX_ADC** and connects to the **ADCIN6** pin of the **TPS65950** and can be controlled and read by the processor using the I2C1 interface. There are voltage level restrictions to this pin, so refer to the **TPS65950** documentation before using this pin.

### 7.26.8 GPIO Signals

Most of the signals can also be configured as either inputs or outputs from the processor. **Table 31** shows the GPIO pin options that can be used on each pin of the connector.

**Table 31. P17 Auxiliary GPIO Signals**

| PIN | SIGNAL | I/O | PROC | DESCRIPTION |
|---|---|---|---|---|
| **3** | GPIO_20 | I/O | AF13 | General Purpose Input/Output |
| **4** | GPIO_21 | I/O | AH14 | General Purpose Input/Output |
| **5** | GPIO_17 | I/O | AE13 | General Purpose Input/Output |
| **6** | GPIO_16 | I/O | AH12 | General Purpose Input/Output |
| **7** | GPIO_15 | I/O | AG12 | General Purpose Input/Output |
| **8** | GPIO_19 | I/O | AH9 | General Purpose Input/Output |
| **9** | GPIO_23 | I/O | AG9 | General Purpose Input/Output |
| **10** | GPIO_14 | I/O | AF11 | General Purpose Input/Output |
| **11** | GPIO_18 | I/O | AE11 | General Purpose Input/Output |
| **12** | GPIO_13 | I/O | AE10 | General Purpose Input/Output |
| **13** | GPIO_22 | I/O | AF9 | General Purpose Input/Output |
| **14** | GPIO_12 | I/O | AF10- | General Purpose Input/Output |
| **15** | GPIO_170 | I/O | J25 | General Purpose Input/Output |
| **16** | GPIO_57 | I/O | P8 | General Purpose Input/Output |

### 7.26.9 DMAREQ

**Pin 16** of the expansion connector can also be configured for a **DMAREQ** pin. Refer to the processor Technical Reference Manual for more information on how to use this signal.

## 7.27 Audio Expansion Header

Also new to the –xM is the addition of the Audio Header that provides access to the **McBSP2** bus that connects to the **TPS65950**. This is the primary audio bus for the processor. For further information on these signals, refer to **Section 8.16.2**

# 8.0 Connector Pinouts and Cables

This section provides a definition of the pinouts and cables to be used with all of the connectors and headers on the BeagleBoard.

**THERE ARE NO CABLES SUPPLIED WITH THE BEAGLEBOARD.**

## 8.1 Power Connector

**Figure 52** is a picture of the BeagleBoard power connector with the pins identified. The supply must have a 2.1mm center hot connector with a 5.5mm outside diameter.

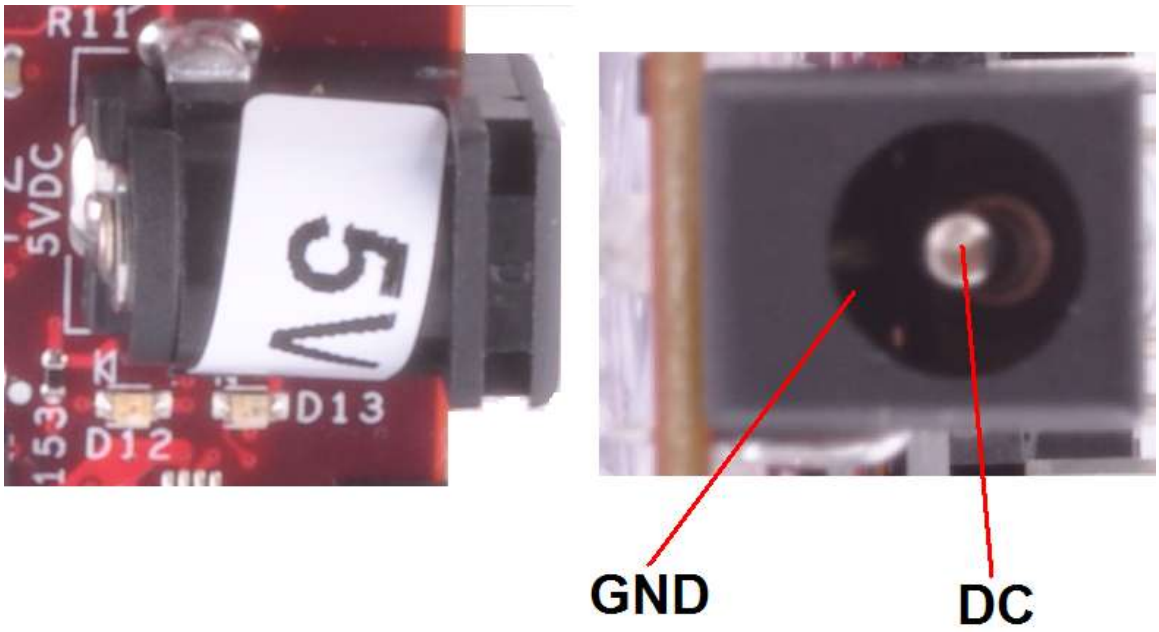



**Figure 52. Power Connector**

The supply must be at least 1A with a maximum of 3A. If the expansion connector is used, more power will be required depending on the load of the devices connected to the expansion connector.

## 8.2 USB OTG

**Figure 53** is a picture of the BeagleBoard USB OTG connector with the pins identified.

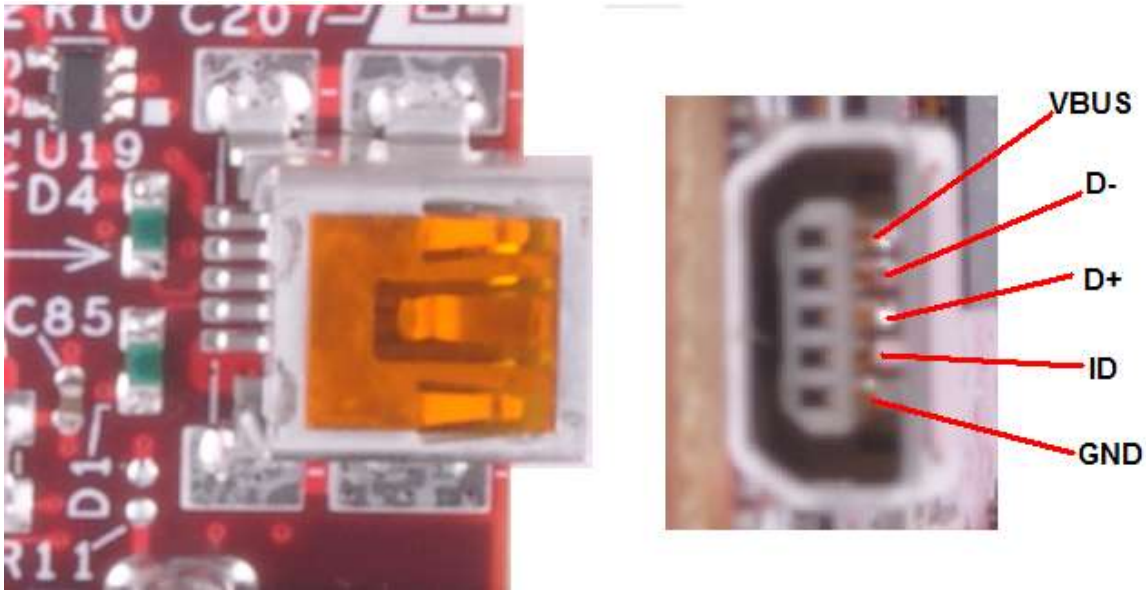



**Figure 53. USB OTG Connector**

The shorting pads, **J1**, to convert the OTG port to a Host mode are found in **Figure 54**.

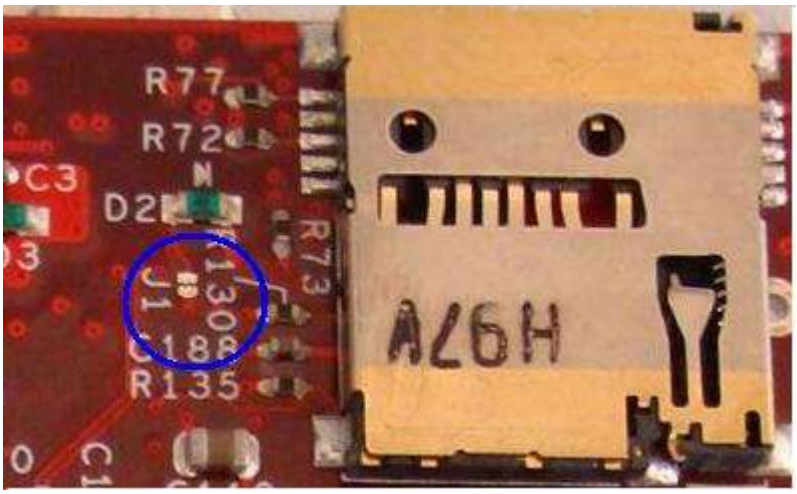



**Figure 54. OTG Host Shorting Pads**

## 8.3 S-Video

**Figure 55** is the S-Video connector on the BeagleBoard.

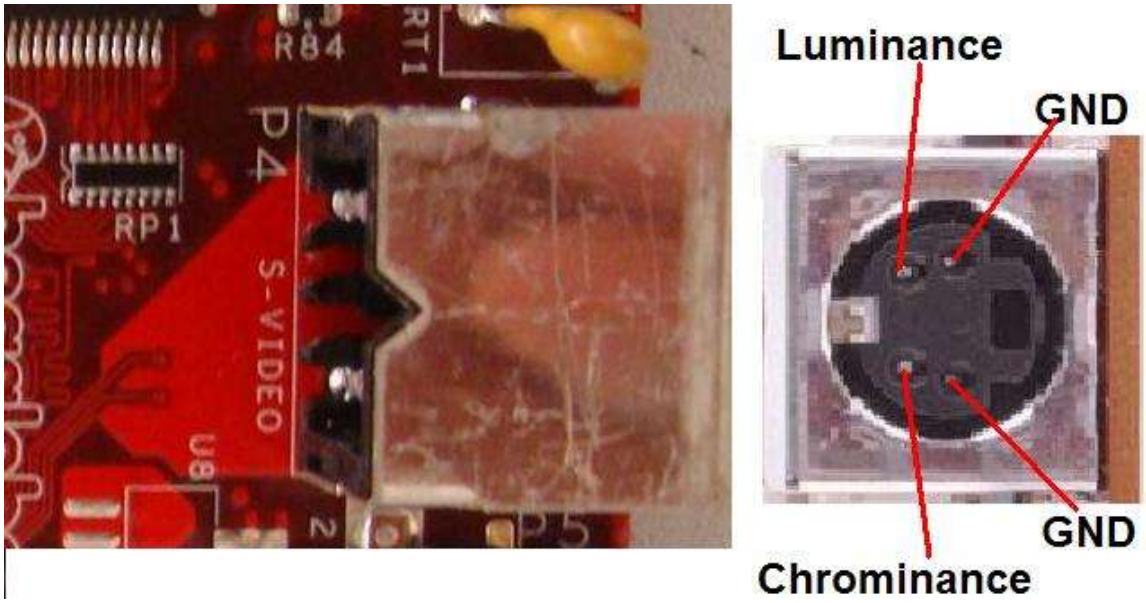



**Figure 55. S-Video Connector**

## 8.4 DVI-D

**Figure 56** is the pinout of the DVI-D connector on BeagleBoard.

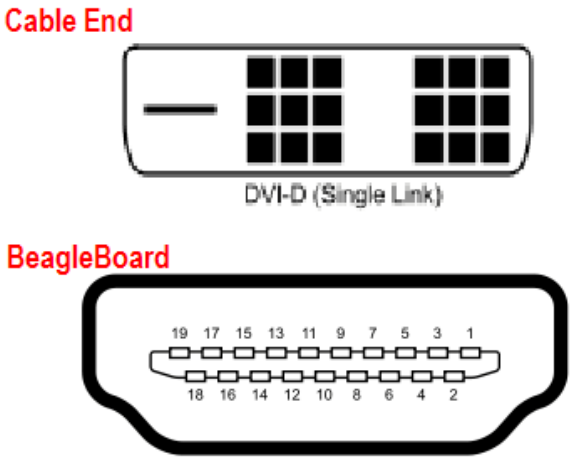



**Figure 56. DVI-D Connector**

**Table 32** is the pin numbering of the two ends of the cable as it relates to the signals used in the DVI-D interface itself.

**Table 32. DVI-D to HDMI Cable**

| SIGNAL | DVI-D PIN# | HDMI PIN# |
|---|---|---|
| DATA 2- | 1 | 3 |
| DATA 2+ | 2 | 1 |
| SHIELD | 3 | 2 |
| | 4 | |
| | 5 | |
| DDS CLOCK | 6 | 15 |
| DDS DATA | 7 | 16 |
| | 8 | |
| DATA 1- | 9 | 6 |
| DATA 1+ | 10 | 4 |
| SHIELD | 11 | 5 |
| | 12 | |
| | 13 | |
| 5V | 14 | 18 |
| GROUND (5V) | 15 | 17 |
| | 16 | |
| DATA 0- | 17 | 9 |
| SIGNAL | DVI-D PIN# | DVI-D PIN# |
| DATA 0+ | 18 | 7 |
| SHIELD | 19 | 5 |
| | 20 | |
| | 21 | |
| | 22 | |
| CLOCK+ | 23 | 10 |
| CLOCK- | 24 | 12 |

**DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.**

**Figure 57** is one of the cables that can be used to connect to an LCD monitor.

**Figure 57. DVI-D Cable**

A standard HDMI cable may be used as well as long as it is used with an adapter if you are connecting to a monitor via the DVI-D port. **Figure 58** shows this configuration.

**Figure 58. DVI-D Cable**

In some cases, the HDMI to HDMI connector could be used to connect direct to a monitor equipped with a HDMI port. It some cases, the BeagleBoard may not work if the display timing is not accepted by the display. It should also be noted that no audio will be provided over this interface.

## 8.5 LCD

This section covers the pair of headers that provide access to the raw 1.8V DSS signals from the processor. This provides the ability to create adapters for such things as different LCD panels, LVDS interfaces, etc.

### 8.5.1 Connector Pinout

The **Table 33** and **34** define the pinout of the LCD connectors. All signal levels are 1.8V with the exception of DVI_PUP signal which is 3.3V.

**Table 33. P11 LCD Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | DC_5V | PWR | DC rail from the Main DC supply |
| 2 | DC_5V | PWR | DC rail from the Main DC supply |
| 3 | DVI_DATA1 | O | LCD Pixel Data bit |
| 4 | DVI_DATA0 | O | LCD Pixel Data bit |
| 5 | DVI_DATA3 | O | LCD Pixel Data bit |
| 6 | DVI_DATA2 | O | LCD Pixel Data bit |
| 7 | DVI_DATA5 | O | LCD Pixel Data bit |
| 8 | DVI_DATA4 | O | LCD Pixel Data bit |
| 9 | DVI_DATA12 | O | LCD Pixel Data bit |
| 10 | DVI_DATA10 | O | LCD Pixel Data bit |
| 11 | DVI_DATA23 | O | LCD Pixel Data bit |
| 12 | DVI_DATA14 | O | LCD Pixel Data bit |
| 13 | DVI_DATA19 | O | LCD Pixel Data bit |
| 14 | DVI_DATA22 | O | LCD Pixel Data bit |
| 15 | I2C3_SDA | I/O | I2C3 Data Line |
| 16 | DVI_DATA11 | O | LCD Pixel Data bit |
| 17 | DVI_VSYNC | O | LCD Vertical Sync Signal |
| 18 | DVI_PUP | O | Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired. |
| 19 | GND | PWR | Ground bus |
| 20 | GND | PWR | Ground bus |

**Table 34. P13 LCD Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | 3.3V | PWR | 3.3V reference rail |
| 2 | VIO_1V8 | PWR | 1.8V buffer reference rail. |
| 3 | DVI_DATA20 | O | LCD Pixel Data bit |
| 4 | DVI_DATA21 | O | LCD Pixel Data bit |
| 5 | DVI_DATA17 | O | LCD Pixel Data bit |
| 6 | DVI_DATA18 | O | LCD Pixel Data bit |
| 7 | DVI_DATA15 | O | LCD Pixel Data bit |
| 8 | DVI_DATA16 | O | LCD Pixel Data bit |
| 9 | DVI_DATA7 | O | LCD Pixel Data bit |
| 10 | DVI_DATA13 | O | LCD Pixel Data bit |
| 11 | DVI_DATA8 | O | LCD Pixel Data bit |
| 12 | NC | | No connect |
| 13 | DVI_DATA9 | | LCD Pixel Data bit |
| 14 | I2C3_SCL | I/O | I2C3 Clock Line |
| 15 | DVI_DATA6 | O | LCD Pixel Data bit |
| 16 | DVI_CLK+ | O | DVI Clock |
| 17 | DVI_DEN | O | Data Enable |
| 18 | DVI_HSYNC | O | Horizontal Sync |
| 19 | GND | PWR | Ground bus |
| 20 | GND | PWR | Ground bus |

**Figure 59** shows where pins 1 and 2 are located on each connector, front and back sides shown. The top side pins make for convenient test points if needed.

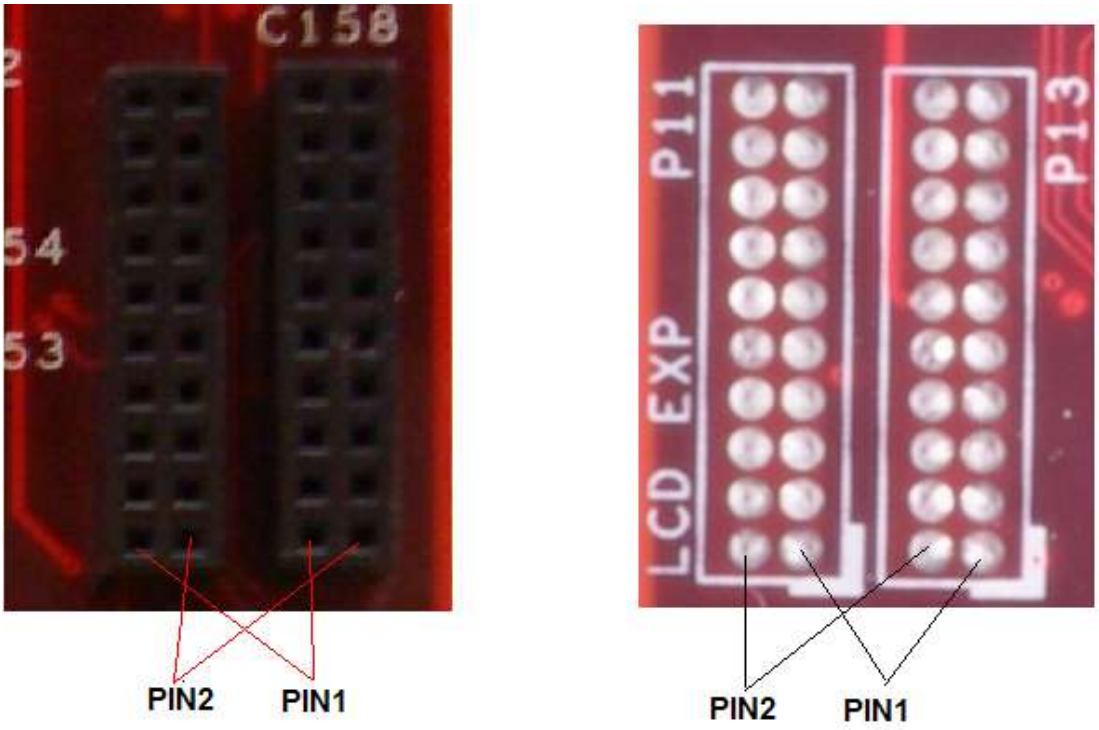



**Figure 59. LCD Expansion Connector Pins**

### 8.5.2 Camera

**Table 35** is the pinout of the camera connector on the board. **Figure 60** shows the pin number and location of the camera connector.

**Table 35. P10 Camera Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | CAM_D11 | I | Camera Data 11 |
| 2 | CAM_CLKA | O | Camera main clock |
| 3 | CAM_D10 | I | Camera Data 10 |
| 4 | GND | PWR | Ground |
| 5 | CAM_D9 | I | Camera Data 9 |
| 6 | I2C_SDA | | Camera control data |
| 7 | CAM_D8 | I | Camera Data 8 |
| 8 | I2C_SCL | I/O | Camera control clock |
| 9 | CAM_D7 | I | Camera Data 7 |
| 10 | CAM_FLD | I | Camera Reset |
| 11 | CAM_D6 | I | Camera Data 6 |
| 12 | CAM_WEN | I | Camera Output enable |
| 13 | CAM_D5 | I | Camera Data 5 |
| 14 | GND | PWR | Ground |
| 15 | CAM_D4 | I | Camera Data 4 |
| 16 | CAM_2V8 | PWR | Camera 2.8V core voltage |
| 17 | CAM_D3 | I | Camera Data 3 |
| 18 | CAM_2V8 | PWR | Camera 2.8V core voltage |
| 19 | CAM_D2 | I | Camera Data 2 |
| 20 | GND | PWR | Ground |
| 21 | CAM_D1 | I | Camera Data 1 |
| 22 | GND | PWR | Ground |
| 23 | CAM_D0 | I | Camera Data 0 |
| 24 | DC_5V | PWR | 5V supply |
| 25 | DC_5V | PWR | 5V supply |
| 26 | DC_5V | PWR | 5V supply |
| 27 | CAM_PCLK | I | Camera Pixel Clock |
| 28 | GND | PWR | Ground |
| 29 | CAM_HS | I | Camera Horizontal Sync |
| 30 | CAM_1V8 | PWR | 1.8V IO rail |
| 31 | CAM_VS | I | Camera vertical Sync |
| 32 | CAM_1V8 | PWR | 1.8V IO rail |
| 33 | GND | PWR | Ground |
| 34 | GND | PWR | Ground |

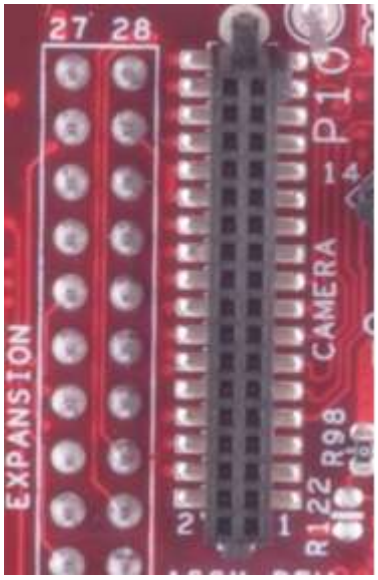



**Figure 60. Camera Connector**

**Figure 61** is the front of the camera module. The camera should face to the edge of the board (Left) when installed. The camera module is not supplied with the BeagleBoard.


**Figure 61. Camera Module**

### 8.5.3 Audio McBSP2 Port

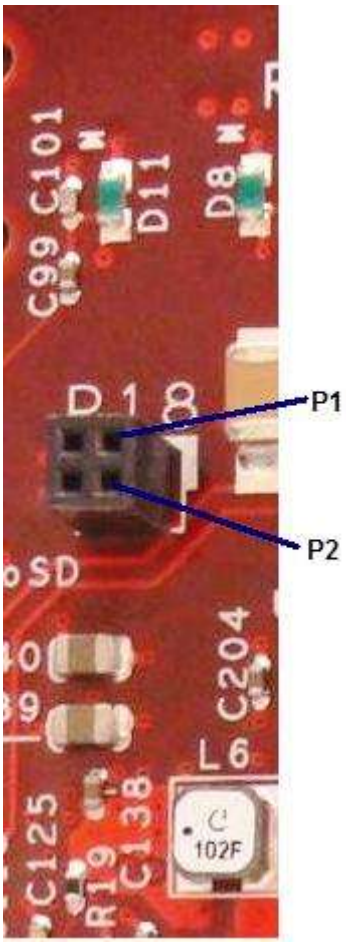
New to the –xM version is the addition of a four pin connector that provides access to the McBSP2 audio serial interface. While other McBSP ports can be used for audio, McBSP2 is the most desirable due its large buffers. **Table 36** is the pin out of the connector.

**Table 36. P10 McBSP2 Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | McBSP2_DX | O | Transmit Out |
| 2 | McBSP2_FSX | O | Frame Sync |
| 3 | McBSP2_DR | I | Receive In |
| 4 | McBSP2_CLKX | O | Clock |

**Figure 62** is the pin number location of P10.

**Figure 62. McBSP Audio Connector**



### 8.5.4 Auxiliary Access Header

**Table 37** gives the signal names of the pins on the Auxiliary Access Connector.

**Table 37. P17 Auxiliary Access Signals**

| Pin# | Signal | I/O | Description |
|---|---|---|---|
| 1 | VIO_1V8 | PWR | 1.8V IO Rail |
| 2 | VMMC2 | PWR | 1.85V to 3.15V Rail. Configurable via SW. |
| 3 | MMC3_DAT2 | I/O | MMC interface data pin. |
| 4 | MMC_DAT7 | I/O | MMC interface data pin. |
| 5 | MMC3_DAT3 | I/O | MMC interface data pin. |
| 6 | GPIO_16 | I/O | General purpose I/O pin |
| 7 | GPIO_15 | I/O | General purpose I/O pin |
| 8 | MMC3_DAT | I/O | MMC interface data pin. |
| 9 | MMC_DAT5 | I/O | MMC interface data pin. |
| 10 | MMC3_DAT4 | I/O | MMC interface data pin. |
| 11 | MMC_DAT0 | I/O | MMC interface data pin. |
| 12 | MMC3_CMD | O | MMC CMD signal pin |
| 13 | MMC_DAT6 | I/O | MMC interface data pin. |
| 14 | MMC3_CLK | O | MMC clock pin |
| 15 | HDQ | I/O | I-wire interface pin |
| 16 | DMAREQ3 | I/O | DMA request input pin |
| 17 | AUX_ADC | I | ADC on TPS65950 |
| 18 | PWR_CNTRL | I | Control pin for on/off button to the TPS65950 |
| 19 | GND | PWR | |
| 20 | GND | PWR | |

**Figure 63** shows the location of P17.

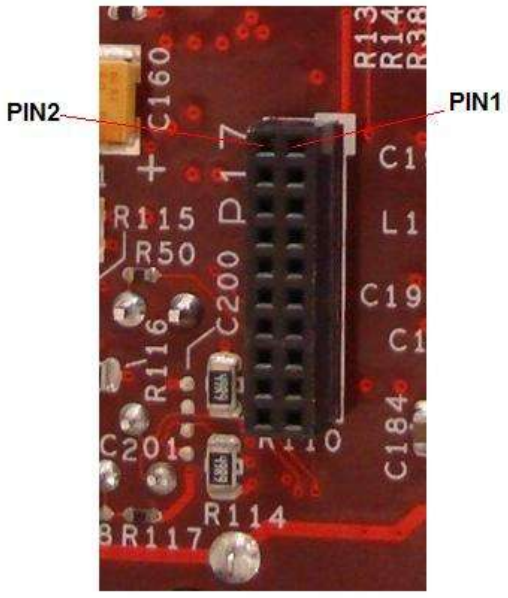



**Figure 63. Auxiliary Access Connector**

### 8.5.5 LCD and Expansion Measurements

**Figure 64** provides some of the dimensions that can assist in the location of the LCD headers. It is strongly recommended that the CAD data be used in order to determine their location exact. **Table 38** provides the values for each lettered dimension.

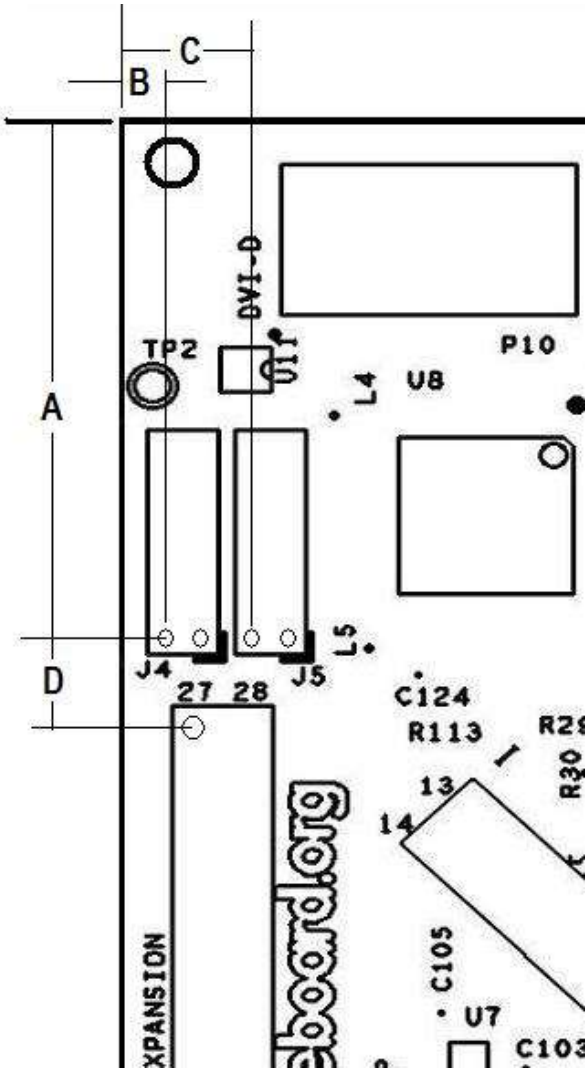



**Figure 64. Top Mount LCD Adapter**

**Table 38. Connector Dimensions**

| Dimension | Inches | Millimeters |
|---|---|---|
| A | 1.21 | 27.56 |
| B | 0.118 | 2.99 |
| C | 0.296 | 7.52 |
| D | 0.190 | 4.83 |

### 8.5.6 Mounting Scenarios

This section provides a few possible mounting scenarios for the LCD connectors. It should be noted that the voltage level of these signals are 1.8V. It will require that they be buffered in order to drive other voltage levels.

**Figure 65** shows the board being mounted under the BeagleBoard.

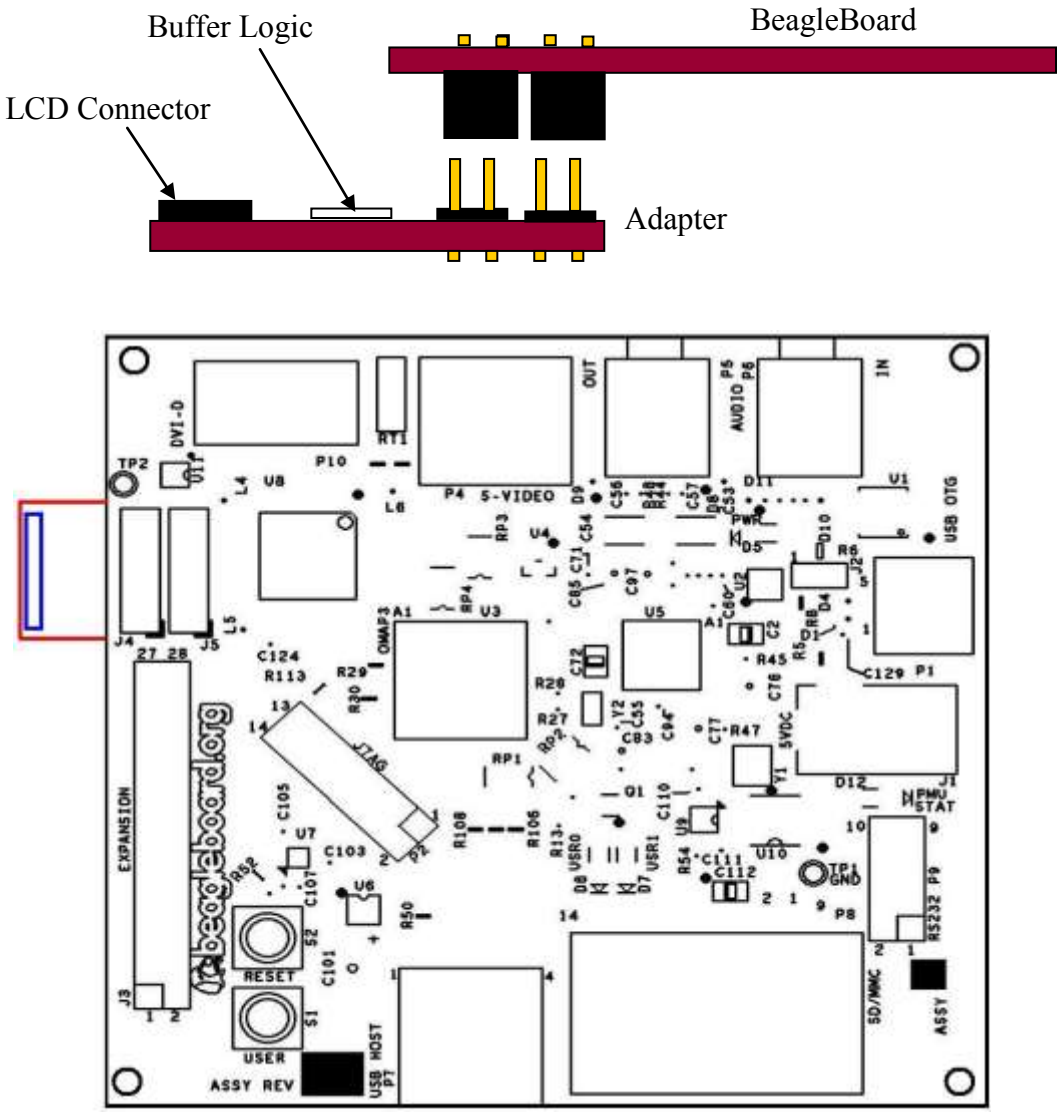



**Figure 65. Bottom Mount LCD Adapter**

## 8.6 Audio Connections

**Figure 66** is the audio input jack required to connect to the BeagleBoard.

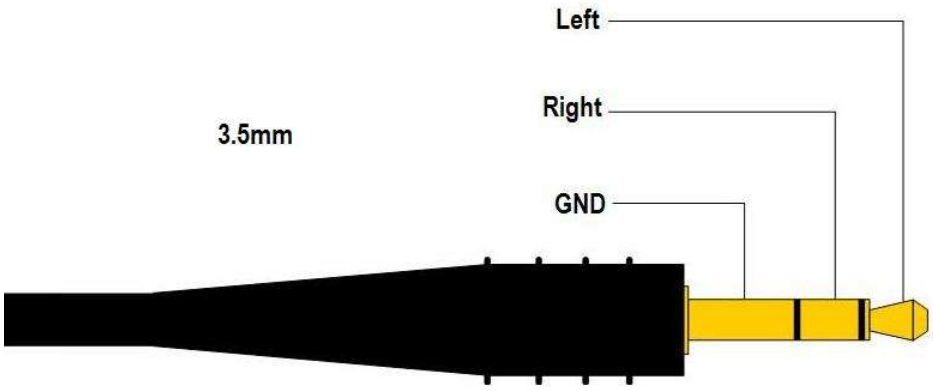



**Figure 66. Audio In Plug**

**Figure 67** is the actual connector used on the BeagleBoard.

**Figure 67. Audio In Connector**

## 8.7 Audio Out

**Figure 68** is the audio out jack required to connect to the BeagleBoard.

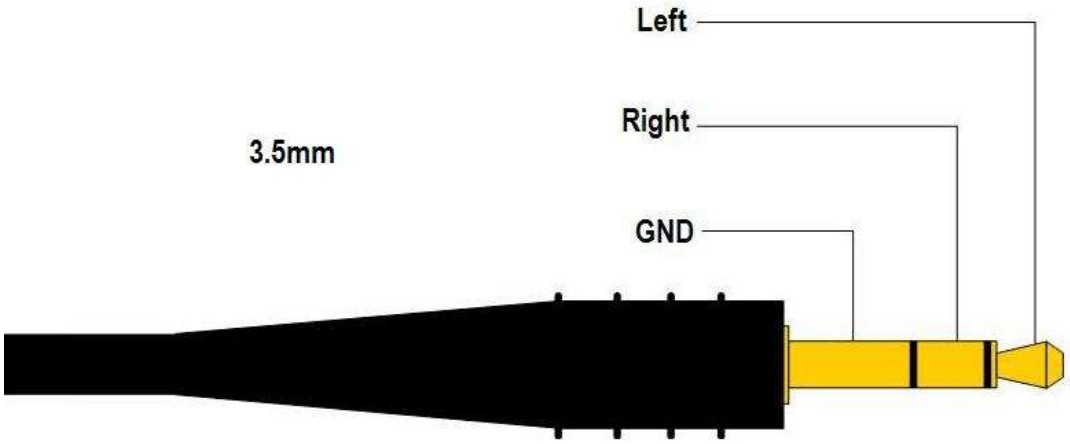



**Figure 68. Audio Out Plug**

**Figure 69** is the actual connector used on the BeagleBoard.

**Figure 69. Audio Out Connector**

## 8.8 JTAG

**Figure 70** is the JTAG connector pin out showing the pin numbering.

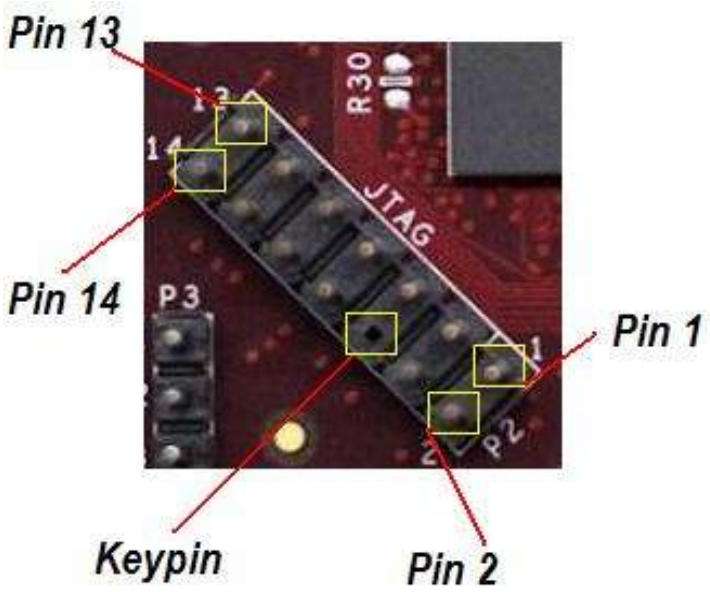



**Figure 70. JTAG Connector Pinout**

**Table 39** gives a definition of each of the signals on the JTAG header.

**Table 39. JTAG Signals**

| Pin | Signal | Description | I/O |
|---|---|---|---|
| 1 | JTAG_TMS | Test mode select | I/O |
| 3 | JTAG_TDI | Test data input | I |
| 7 | JTAG_TDO | Test Data Output | O |
| 9 | JTAG_RTCK | ARM Clock Emulation | O |
| 11 | JTAG_TCK | Test Clock | I |
| 2 | JTAG_nTRST | Test reset | I |
| 13 | JTAG_EMU0 | Test emulation 0 | I/O |
| 14 | JTAG_EMU1 | Test emulation 1 | I/O |
| 5 | VIO | Voltage pin | PWR |
| 4,8,10,12,14 | GND | Ground | PWR |

All of the signals are 1.8V only. The JTAG emulator must support 1.8V signals for use on the BeagleBoard.

If a 20 pin connector is provided on the JTAG emulator, then a 20 pin to 14 pin adapter must be used. You may also use emulators that are either equipped with a 14 pin connector or are universal in nature.

**Figure 71** shows an example of a 14 pin to 20 pin adapter.

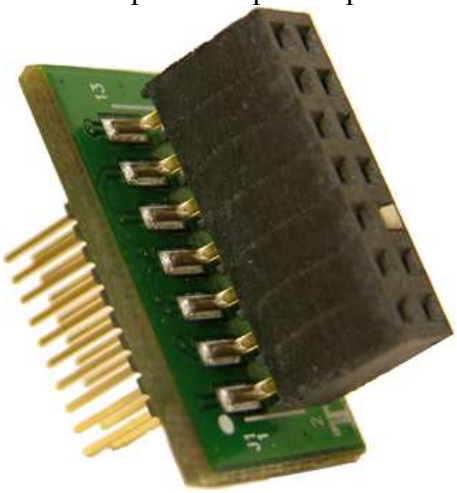
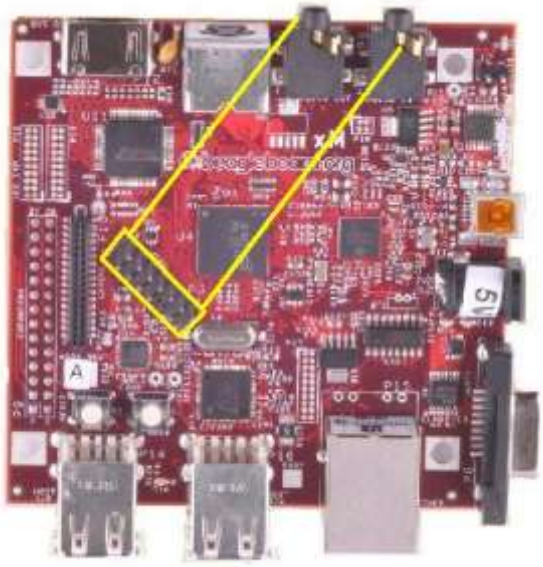


**Figure 71. JTAG 14 to 20 Pin Adapter**

**Figure 72** shows how the JTAG cable is to be routed when connected to the BeagleBoard.

**Figure 72. JTAG Cable Placement**



## 8.9 Battery Installation

### 8.9.1 Battery

The board was designed to use the MS412FE-FL26E battery from Seiko Instruments. This is a Lithium Rechargeable Battery with a 1mAH capacity. **Figure 73** is a picture of the battery. It is also possible that the user may choose to install a higher capacity Lithium battery.

**Figure 73. Optional Battery**

### 8.9.2 Battery Installation

THE FOLLOWING STRUCTIONS ASSUME THE USER HAS PREVIOUS EXPERIENCE WITH BATTERIES. BATTERY INSTALLATION IS THE SOLE RESPONSABILTY OF THE USER. INSTALLATION OF THE BATTERY BY THE USER IS AT THEIR OWN RISK. FAILURE TO FOLLOW THE INSTRUCTIONS CAN RESULT IN DAMAGE TO THE BOARD. THIS DAMAGE IS NOT COVERED UNDER THE WARRANTY.

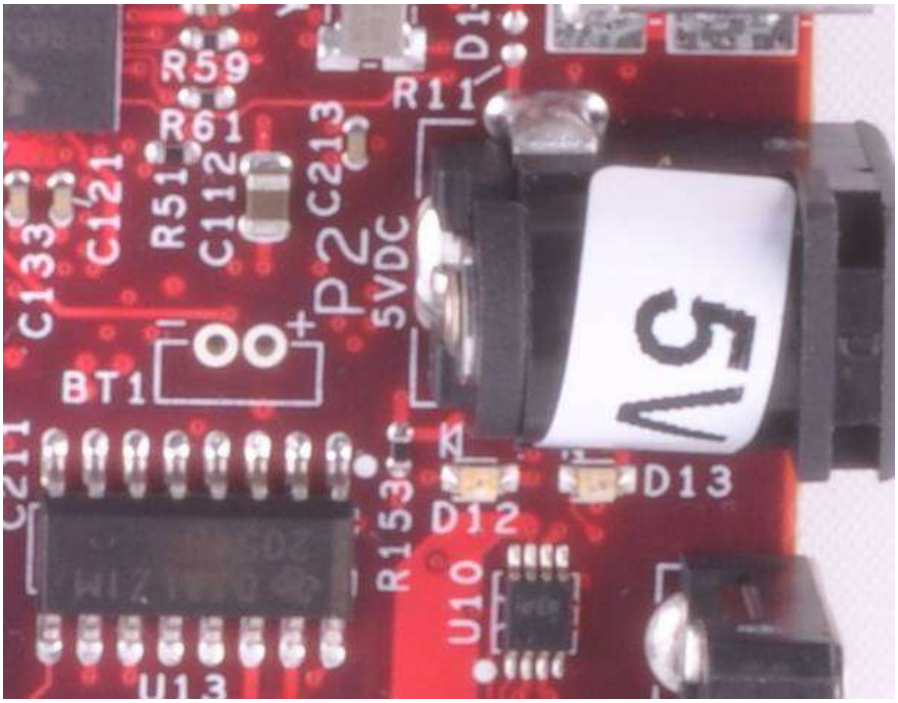



**Figure 74. Optional Battery Location**

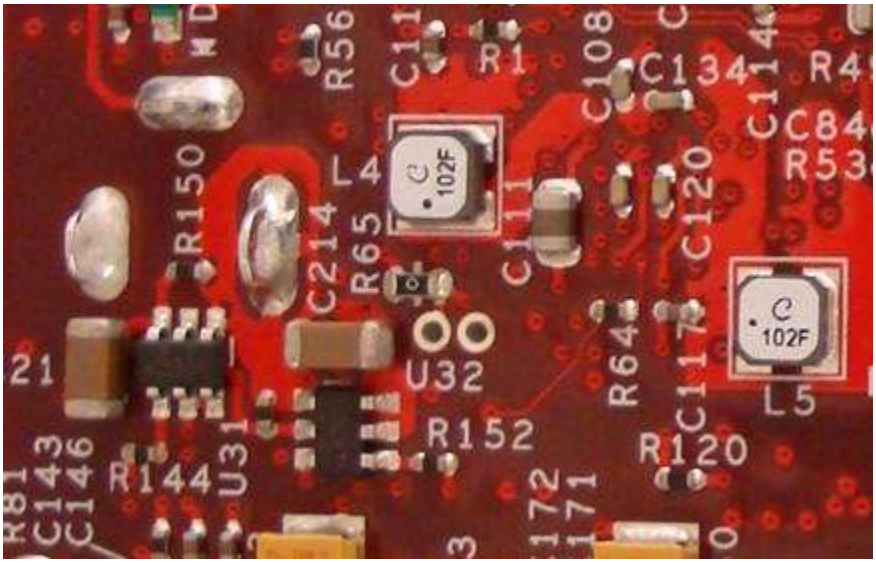



**Figure 75. Resistor R65**

Following are the steps required to install the battery.

1) Remove all cables from the board.
2) Remove **R65** from the board as shown on **Figure 75**.
3) Using **Figure 73**, locate the positive (+) lead of the battery.
4) Insert the (+) lead into the hole that is marked (+) on **Figure 74**.

## 9.0 BeagleBoard Accessories

Throughout this manual various items are mentioned as not being provided with the standard BeagleBoard package or as options to extend the features of the BeagleBoard. The concept behind BeagleBoard is that different features and functions can be added to BeagleBoard by bringing your own peripherals. This has several key advantages:

- User can choose which peripherals to add.
- User can choose the brand of peripherals based on driver availability and ability to acquire the particular peripheral
- User can add these peripherals at a lower cost than if they were integrated into the BeagleBoard.

This section covers these accessories and add-ons and provides information on where they may be obtained. Obviously things can change very quickly as it relates to devices that may be available. Please check BeagleBoard.org for an up to date listing of these peripherals.

Inclusion of any products in this section does not guarantee that they will operate with all SW releases. It is up to the user to find the appropriate drivers for each of these products. Information provided here is intended to expose the capabilities of what can be done with the BeagleBoard and how it can be expanded.

Inclusion of any product in this section is not an endorsement of the product by Beagleboard.org, but is provided as a convenience only to the users of the BeagleBoard-xM board.

All pricing information provided is subject to change and in most cases is likely to be lower depending on the products purchased and from where they are purchased.

Covered in this section are the following accessories:

- DC Power Supplies
- Serial Ribbon cable
- USB Hubs
- USB Thumb Drives
- DVI-D Cables
- DVI-D Monitors
- SD/MMC Cards
- USB to Ethernet

- USB to WiFi
- USB Bluetooth
- Expansion Cards

**NO CABLES OR POWER SUPPLIES ARE PROVIDED WITH THE BEAGLEBOARD**.

## 9.1 DC Power Supply

Tabletop or wall plug supplies can be used to power BeagleBoard. **Table 40** provides the specifications for the BeagleBoard DC supply. Supplies that provide additional current than what is specified can be used if additional current is needed for add on accessories. The amount specified is equal to that supplied by a USB port.

**Table 40. DC Power Supply Specifications**

| Specification | Requirement | Unit |
|---|---|---|
| Voltage | 5.0 | V |
| Current | 1.5 (minimum) | A |
| Connector | 2.1mm x 5.5mm Center hot | |

It is recommended that a supply higher than 1.5A be used if higher current peripherals are expected to be used or if expansion boards are added. The onboard USB hub and Ethernet do consume additional power and if you plan to load the USB Host ports, more power will be required..

**Table 41** lists some power supplies that will work with the BeagleBoard.

**Table 41. DC Power Supplies**

| Part # | Manufacturer | Supplier | Price |
|---|---|---|---|
| EPS050100-P6P | CUI | Digi-Key | $7 |
| DPS050200UPS-P5P-SZ | CUI | Digi-Key | $16 |

**Figure 76** is a picture of the type of power supply that will be used on the BeagleBoard.

**Figure 76. DC Power Supply**

## 9.2 DVI Cables

In order to connect the DVI-D interface to a LCD monitor, a HDMI to DVI-D cable is required. **Figure 77** is a picture of a HDMI to DVI-D cable.

**Figure 77. HDMI to DVI-D Cable**

## 9.3 DVI-D Monitors

There are many monitors that can be used with the BeagleBoard. With the integrated EDID feature, timing data is collected from the monitor to enable the SW to adjust its timings. **Table 42** shows a short list of the monitors that have been tested to date on the BeagleBoard at the 1024x768 resolution. Please check on BeagleBoard.org for an up to date listing of the DVI-D monitors as well as information on the availability of drivers.

**Table 42. DVI-D Monitors Tested**

| Manufacturer | Part Number | Status |
|---|---|---|
| Dell | 2407WFPb | Tested |
| Insignia | NS-LCD15 | Tested |
| Dell | 1708FP | Tested |
| LG | FLATRON W2243T | Tested |

**DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.**

The digital portion of the DVI-D interface is compatible with HDMI and is electrically the same. A standard HDMI cable may be used to connect to the HDMI input of monitors. Whether or not the Beagle will support those monitors is dependent on the timings that are used on the Beagle and those that are accepted by the monitor. This may require a change in the software running on the Beagle. The audio and encryption features of HDMI are not supported by the Beagle.

The analog portion of DVI which provides RGB analog type signals is not supported by the Beagle. Buying a DVI to VGA adapter connector will not work on a VGA display. You will need an active DVI-D to VGA adapter.

## 9.4 microSD Cards

**Table 43** is a list of SD/MMC cards that have been tested on BeagleBoard. Please check BeagleBoard.org for an up to date listing of the SD/MMC cards that have been tested as well as information on the availability of drivers if required.

**Table 43. SD/MMC Cards Tested**

| Manufacturer | Type | Part Number | Status |
|---|---|---|---|
| Patriot | 4GB | | Tested |
| | | | |

## 9.5 USB to WiFi

There are several USB to WiFi adapters on the market and **Figure 78** shows a few of these devices. These devices can easily add WiFi connectivity to BeagleBoard by using the USB OTG port in the host mode. This will require a special cable to convert the miniAB connector to a Type A or a hub can also be used. These are provided as examples only. Check BeagleBoard.org for information on devices that have drivers available for them.


**Figure 78. USB to WiFi**

**Table 44** provides a list of USB to WiFi adapters that could be used with the BeagleBoard. Inclusion of these items in the table does not guarantee that they will work, but is provided as examples only. Please check BeagleBoard.org for an up to date listing of the USB to WiFi devices as well as information on the availability of drivers.

**Table 44. USB to WiFi Adapters**

| Product | Manufacturer | Status |
|---|---|---|
| 4410-00-00AF | Zoom | Not Tested |
| HWUG1 | Hawkins | Not Tested |
| TEW-429Uf | Trendnet | Not Tested |

It should be noted that the availability of Linux drivers for various WiFi devices is limited. Before purchasing a particular device, please verify the availability of drivers for that device.

## 9.6 USB to Bluetooth

There are several USB to Bluetooth adapters on the market and **Figure 79** shows a few of these devices. These devices can easily add Bluetooth connectivity to BeagleBoard by using the USB OTG port in the host mode. This will require a special cable to convert the miniAB connector to a Type A or a hub can also be used. These are provided as examples only. Check BeagleBoard.org for information on devices that have drivers available for them and their test status.

**Figure 79. USB to Bluetooth**

**Table 45** provides a list of USB to Bluetooth adapters that could be used with the BeagleBoard. Inclusion of these items in the table does not guarantee that they will work, but is provided as examples only. Please check BeagleBoard.org for an up to date listing of the USB to Bluetooth devices as well as information on the availability of drivers.

**Table 45. USB to Bluetooth Adapters**

| Product | Manufacturer | Status |
|---|---|---|
| TBW-105UB | Trendnet | Not Tested |
| ABT-200 | Airlink | Not Tested |
| F8T012-1 | Belkin | Not Tested |

# 10.0 Mechanical Information

## 10.1 BeagleBoard Dimensions

This section provides information on the mechanical aspect of the BeagleBoard. **Figure 80** is the dimensions of the BeagleBoard. Despite the change in the overall dimensions of the board, the mounting holes and the replacement of the main expansion and LCD headers are the same as is found on the BeagleBoard board.

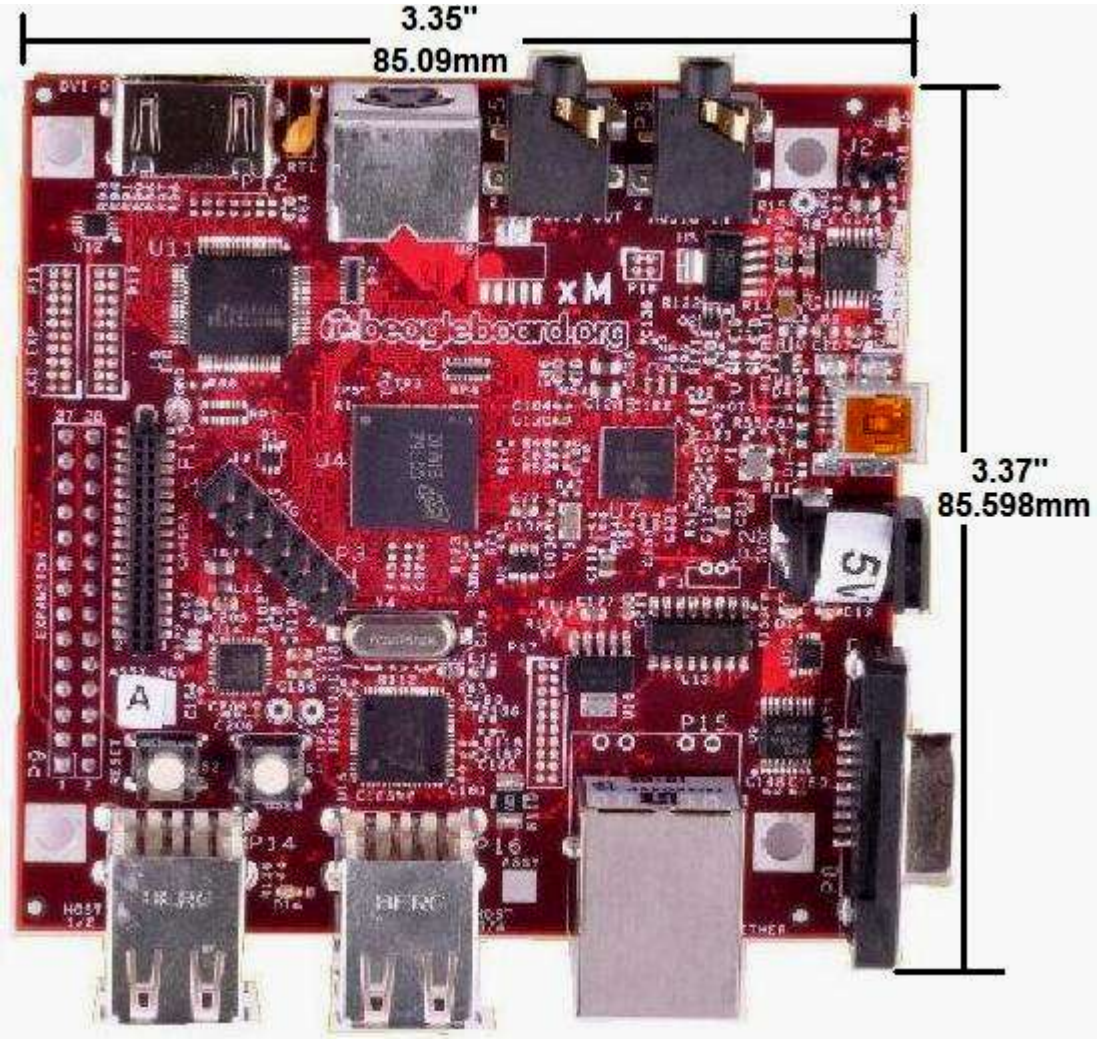



**Figure 80. BeagleBoard Dimension Drawing**

## 10.2 BeagleBoard Expansion Card Design Information

This section provides information on what is required from a mechanical and electrical aspect to create expansion cards for the BeagleBoard that are designed to connect to the Expansion header on the BeagleBoard. Users are free to create their own cards for private or commercial use, but in order to be supported by the Software they must conform to these standards if such support is desired.

### 10.2.1 Mounting Method

The standard method to provide a daughtercard for the BeagleBoard is for it to be mounted UNDER the Beagle Board as described in **Figure 81.**

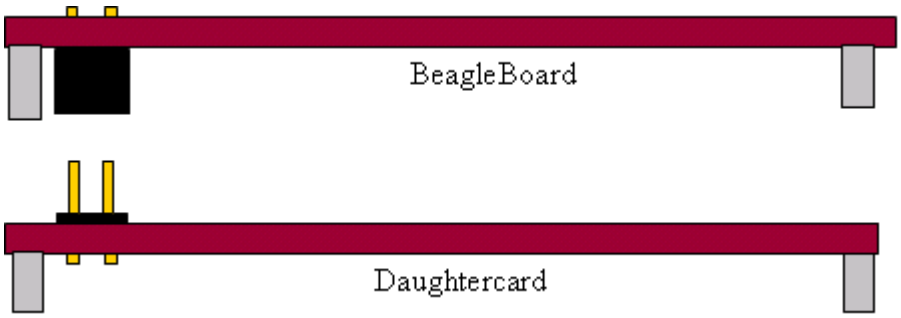



**Figure 81. BeagleBoard Bottom Stacked Daughter Card**

All BeagleBoard-xM produced will have the connectors pre mounted onto the bottom of the BeagleBoard as described above. The –xM has additional connectors on the back of the board. **Figure 82** shows their location.

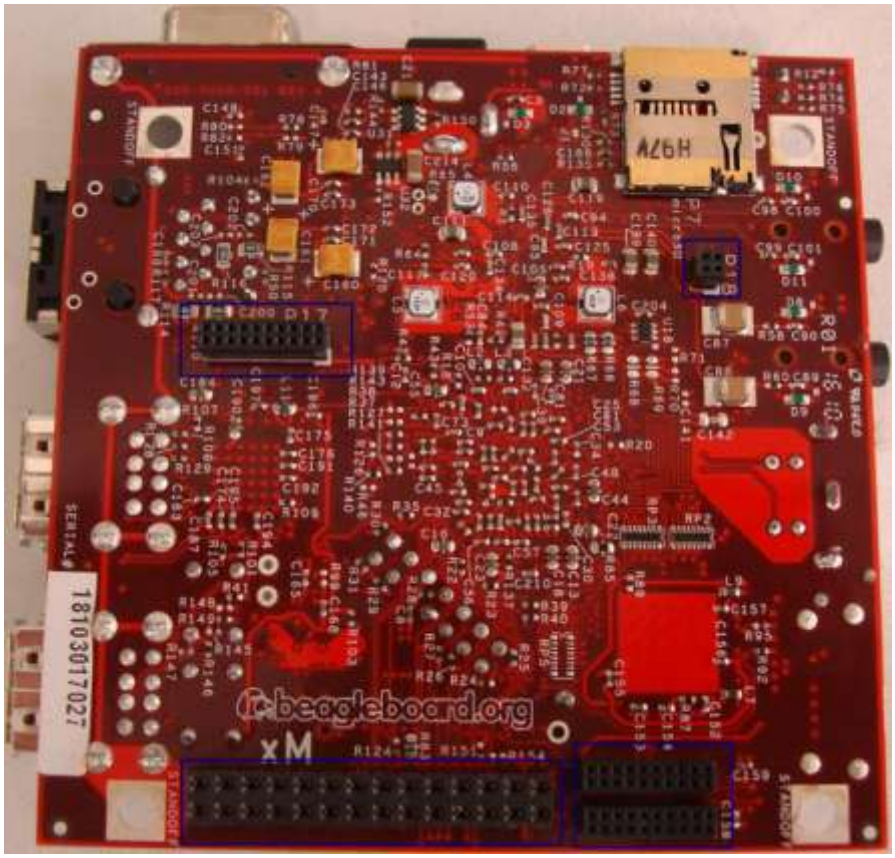



**Figure 82. BeagleBoard-xM Expansion Headers**

### 10.2.2 Expansion EEPROM

All expansion cards designed for use with the BeagleBoard are required to have a EEPROM located on the board. This is to allow for the identification of the card by the Software in order to set the pin muxing on the expansion connector to be compatible with the expansion card.

The schematic for the EEPROM is in **Figure 83** below.

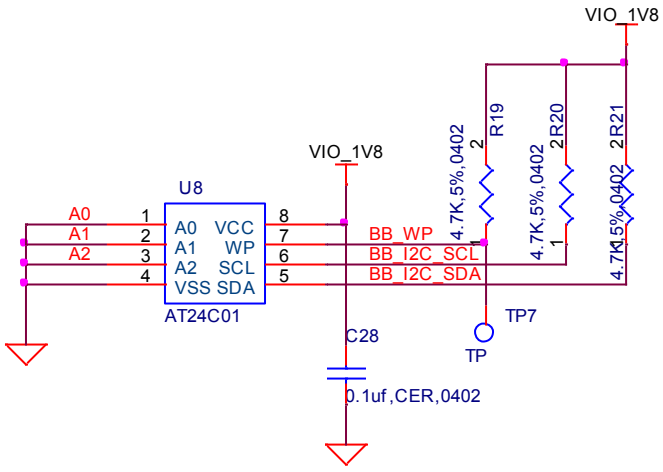



**Figure 83. BeagleBoard Expansion Board EEPROM Schematic**

The EEPROM must be write protected. It is suggested that a testpoint be used to allow for the WP to be disabled during test to allow the required data to be written to the EEPROM. The EEPROM is to be connected to I2C2 as found on the main expansion connector.

The EEPROM that is designated is the AT24C01 or ATC24C01B. The AT24C01 is designated as "Not Recommended for New Design" but can still be used. The AT24C01B is the replacement part and is available in several different packages, all of which can be used.

- TSSOP 8
- PDIP 8
- UDFN 8
- SOIC 8
- SOT23 5
- dBGA2 8

The contents of the EEPROM are not specified in this document.

## 11.0 Board Verification Test Points

There are several test points that may be useful if it becomes necessary to troubleshoot the BeagleBoard-xM board. **Figure 84** shows the top side test points.

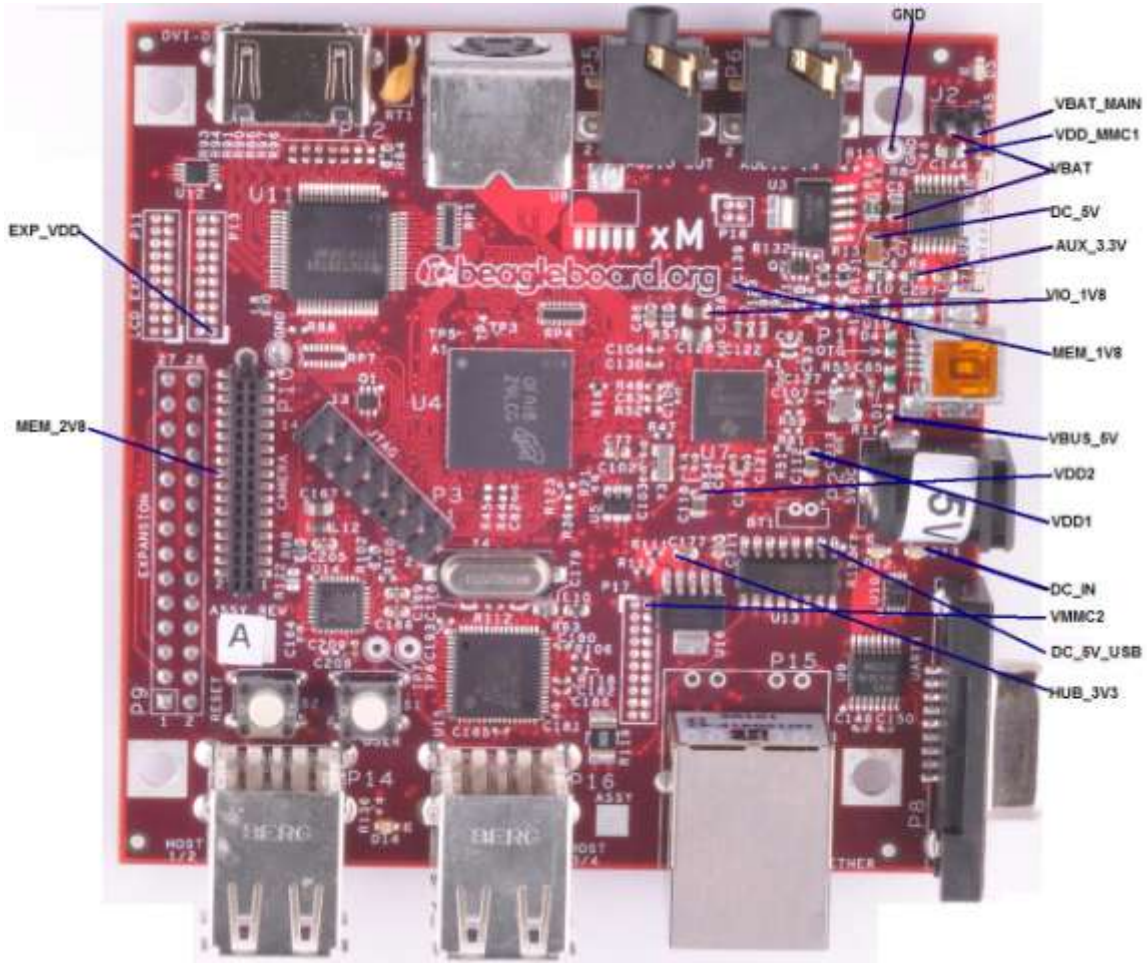



**Figure 84. BeagleBoard Voltage Access Points**

Some of these voltages may not be present depending on the state of the TWL4030 as set by the processor. Others may be at different voltage levels depending on the same factor.

**Table 46** provides the ranges of the voltages and the definition of the conditions as applicable.

**Table 46. Voltages**

| Voltage | Min | Nom | Max | Conditions |
|---|---|---|---|---|
| VIO_1V8 | 1.78 | 1.8 | 1.81 | |
| VDD_SIM | 1.78 | 1.8 | 1.81 | |
| VBUS_5V0 | 4.9 | 5.0 | 5.2 | From the host PC. May be lower or higher. |
| VOCORE_1V3 | 1.15 | 1.2 | 1.4 | Can be set via SW. Voltage levels may vary. |
| VBAT | 4.1 | 4.2 | 4.3 | |
| VDAC_1V8 | 1.78 | 1.8 | 1.81 | |
| VDD_PLL1 | 1.78 | 1.8 | 1.81 | |
| VDD_PLL2 | 1.78 | 1.8 | 1.81 | |
| VDD2 | 1.15 | 1.2 | 1.25 | |
| 3.3V | 3.28 | 3.3 | 3.32 | |
| VMMC1 (3V) | 2.9 | 3.0 | 3.1 | 3.0V at power up. Can be set to via SW. |
| VMMC1(1.8V) | 1.78 | 1.8 | 1.81 | |

### 11.1.1 Signal Access Points

**Figure 85** shows the access points for various signals on BeagleBoard.

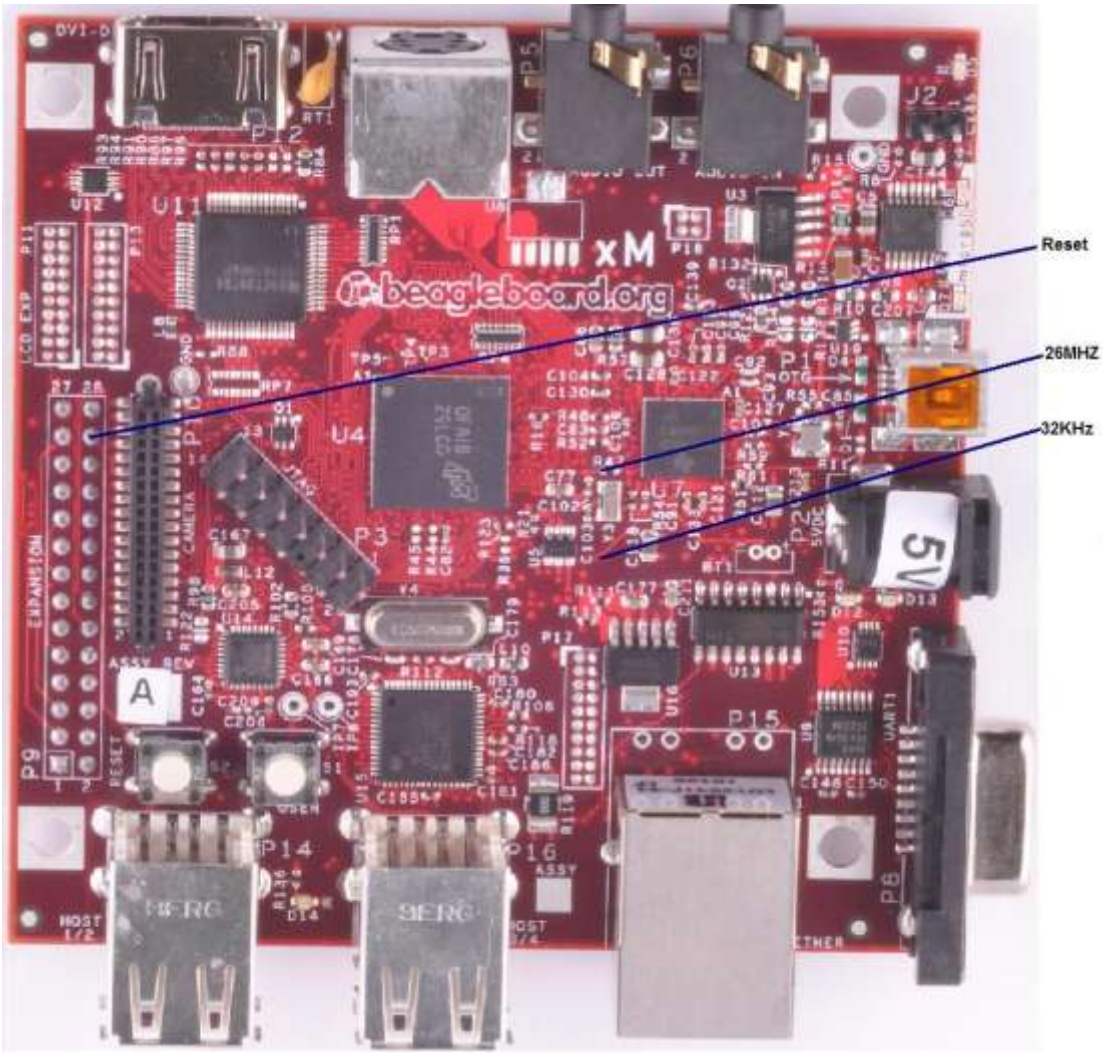



**Figure 85. BeagleBoard Signal Access Points**

## 11.2 Troubleshooting Guide

**Table 47** provides a list of possible failure modes and conditions and suggestions on how to diagnose them and ultimate determine whether the HW is operational or not.

**Table 47. Troubleshooting**

| Symptoms | Possible Problem | Action |
|---|---|---|
| JTAG does not connect. | Verify that the Power LED is on. | If off and running over USB, the PC may have shut down the voltage due to excessive current as related to what it is capable of providing. Remove the USB cable and re insert.<br><br>If running on a DC supply make sure that voltage is being supplied. |
| | JTAG interface needs to be reset. | Reset the BeagleBoard. |
| UBoot does not start, and no activity on the RS232 monitor. | Incorrect serial cable configuration. | Verify straight thru cable configuration. |
| | If a 60 is displayed over the serial cable, processor is booting. Issue could be the SD/MMC card. | Make sure the SD/MMC card is installed all they way into the connector. |
| | | Make sure the card is formatted correctly and that the MLO file is the first file written to the SD card. |
| USB Host Connection Issues via OTG. | Cheap USB Cable. OTG cables are typically not designed for higher current. The expect 100mA max. | Measure the voltage at the card to determine the voltage drop across the cable. If it the level is below 4.35V, the USB power is not guaranteed to work. |

## 12.0 Known Issues

This section provides information on any known issues with the BeagleBoard HW and the overall status. **Table 48** provides a list of the know issues on the BeagleBoard.

**Table 48. Known Issues**

| Affected Revision | Issue | Description | Workaround | Final Fix |
|---|---|---|---|---|
| A | DVI Powerdown | DVI power down signal is not operational | None | B |
| A | USB Hub reset | Reset signal to hub is not operational | Hub can be powered off and on to create a reset scenario | No Plan |

## 13.0 PCB Component Locations

**Figures 86** and **Figure 87** contain the bottom and top side component locations of the BeagleBoard.

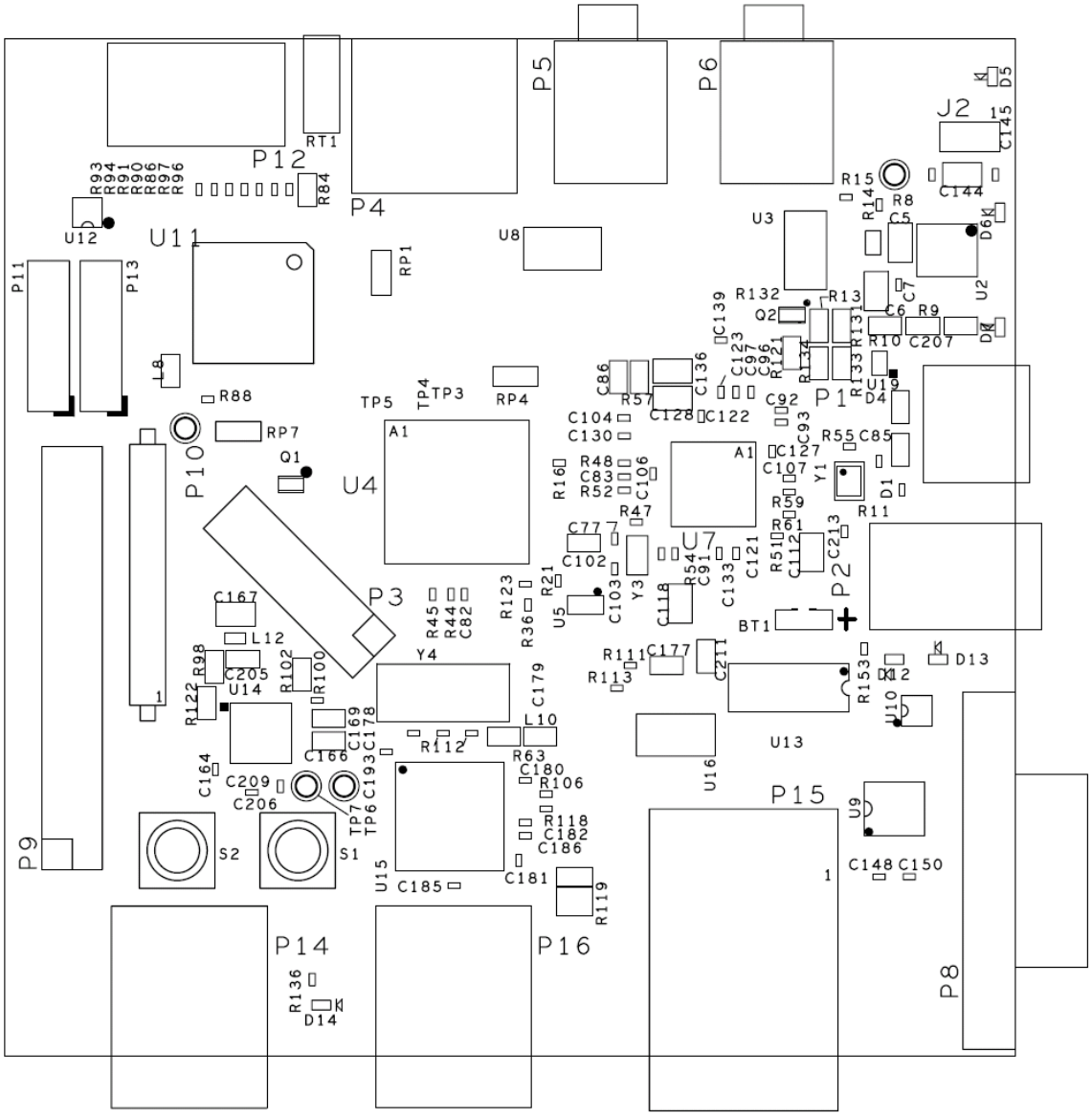



**Figure 86. BeagleBoard Top Side Components**

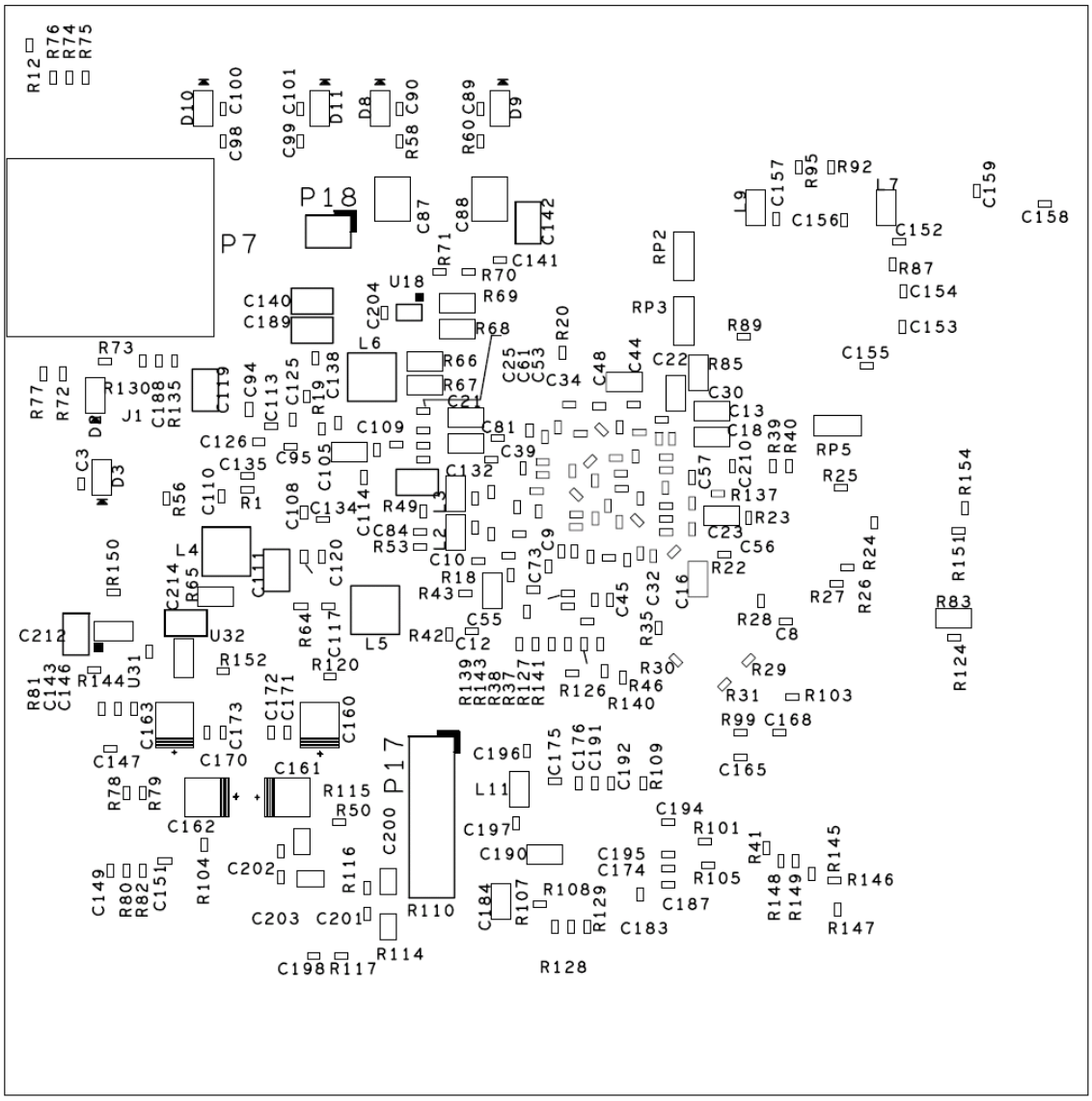



**Figure 87. BeagleBoard Bottom Side Components**

## 14.0 Schematics

The following pages contain the PDF schematics for the BeagleBoard. This manual will be periodically updated, but for the latest documentation be sure and check BeagleBoard.org for the latest schematics.

OrCAD source files are provided for BeagleBoard on BeagleBoard.org at the following link.

http://beagleboard.org/hardware/design

*These design materials are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss. THERE IS NO WARRANTY FOR THE DESIGN MATERIALS, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.*
*We mean it, these design materials may be totally unsuitable for any purposes.*

| REV | DESCRIPTION | DATE | BY |
|---|---|---|---|
| | FEATURE CHANGES<br>1. Added 4 port LS/FS/HS HUB to provide four USB Host ports.<br>2. Made connection for the 1.8V rail on the USB PHY to go to VAUX2.<br>3. Added camera connector that is compatible to the Leopard Imaging Camera modules.<br>4. Added power mmanagement capabilities to allow shut downn of serial port, DVI-D and power LED.<br>5. Switched to DM3730 processor and 512MB memory.<br>6. Added ability to turn off 26MHZ oscillator.<br>7. Increased overall board size to accomodate the changes.<br>8. Changed serial connector to a female DB9.<br>9. Added a 10/100 Ethernet port. | 8/31/09 | GC |
| A1 | 1. Disabled the DVI-D power down due to use of wrong GPIO pin. Pin is in the MMC group and it cannot be switched to 1.8V without impacting the SD card slot.<br>2. Disables HUB reset due to a timing issue with SW. When active the LAN9514 would not work correctly and the Ethernet function is broken. | 5/13/10 | GC |
| A2 | 1. Changed C9 to DNI and changed R34, 4.7K to installed to enable the S-Video operation. | 6/15/10 | GC |
| A3 | NO MAJOR FEATURE CHANGES.<br>1. PCB Layout changes.<br>2. Added R157 in series with MMC2_CLK.<br>3. Added R158 to isolate shunt FET to reduce power in DC mode.<br>4. Added optional pullup resistors on I2C2_SCL and I2C_SDA into the layout.<br>5. Moved DVI_PUP signal to TPS65950. Previous location could not be used due to a conflict with the MMC function on the pins. | 6/23/10 | GC |
| B | NO MAJOR FEATURE CHANGES.<br>1. Changed DM3730 from an ES1.0 to a ES1.1. | 10/26/2010 | GC |
| C | REPLACED OVERVOLTAGE CIRCUIT<br>1. Deleted U19, U31, and U32<br>2. Deleted C214 and C212<br>3. Added new U31 and U32, a NCP349MNAE overvoltage protection device<br>ADDED DC POWER DETECTION<br>1. Moved Q2A to level shift nUSB_PWR<br>2. Connected Q2A output to the TPS65950 GPIO as indication that the board is DC powered when LOW.<br>CHANGED SD CONNECTOR DUE TO EOL OF CURRENT PART.<br>1. Replaced uSD connector with new part number.<br>2. Delete C188, R131, R133,R132, R134, R152, R153, R15, R144, R120, C211.<br>CHANGED PROCESSOR TO ES1.2<br>CHANGED USB HUB DEFAULT MODE<br>1. Changed DC control of HUB to come up OFF. Requires SW to activate. | 12/7/2010 | GC |

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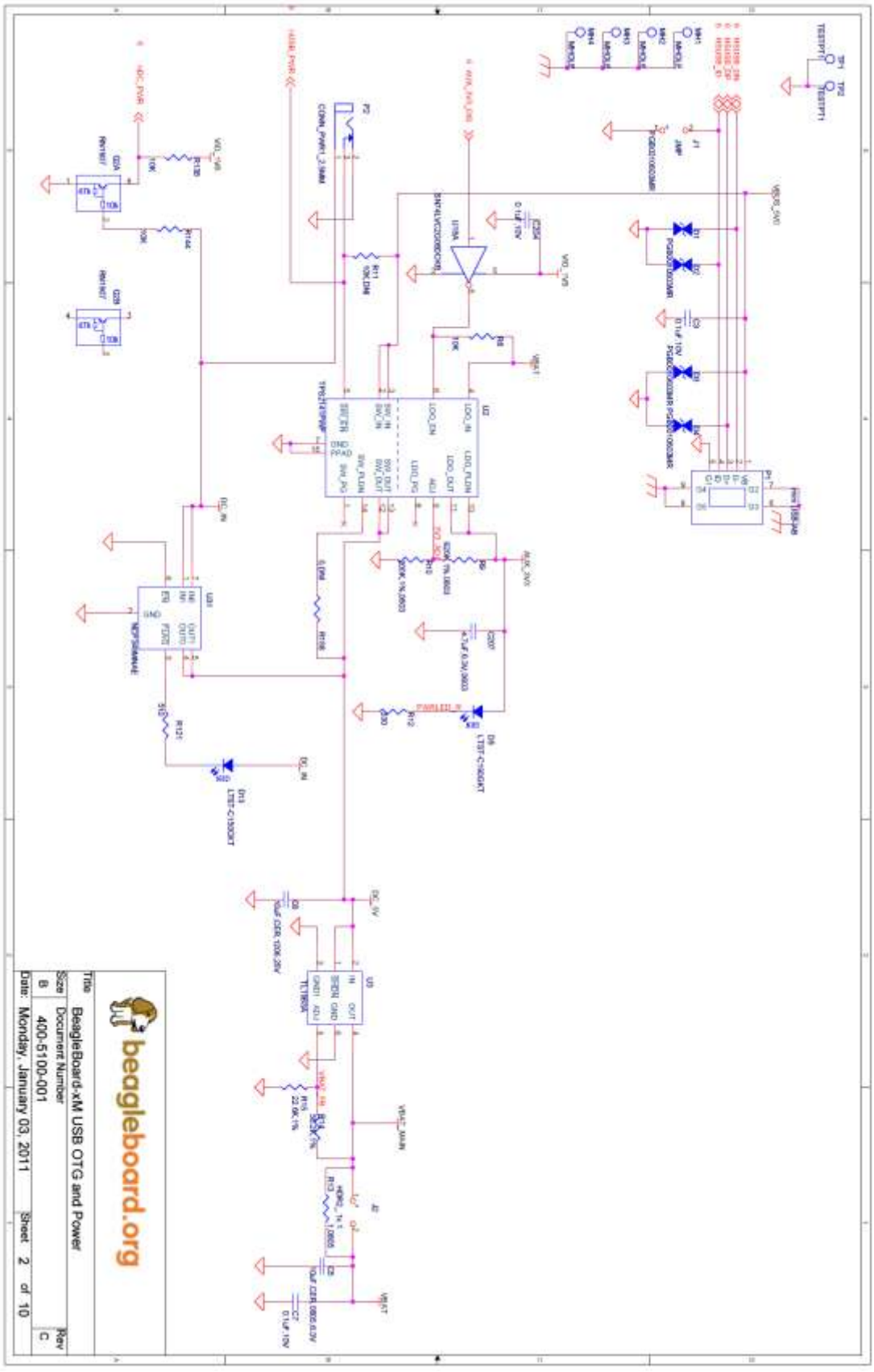
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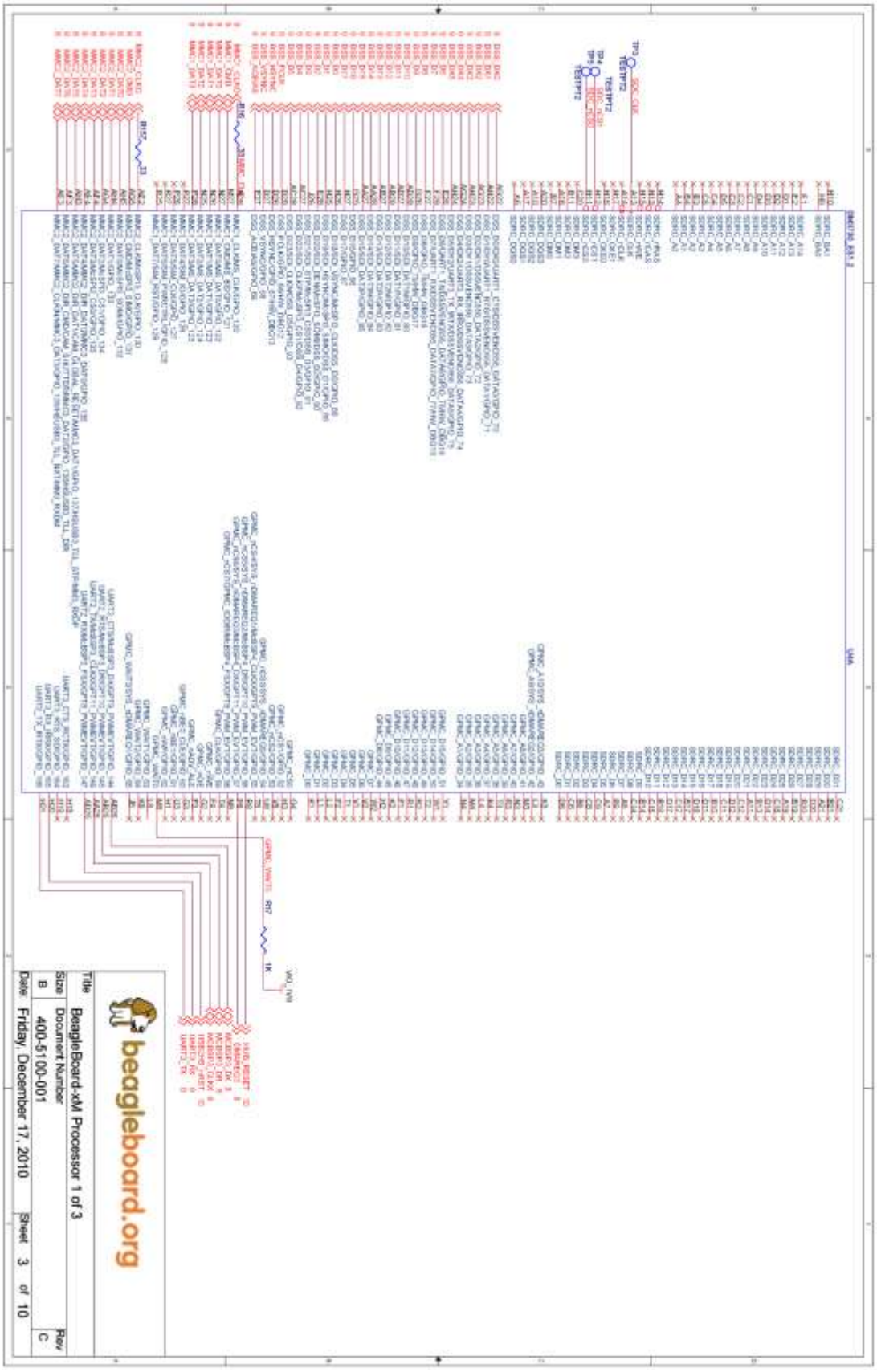
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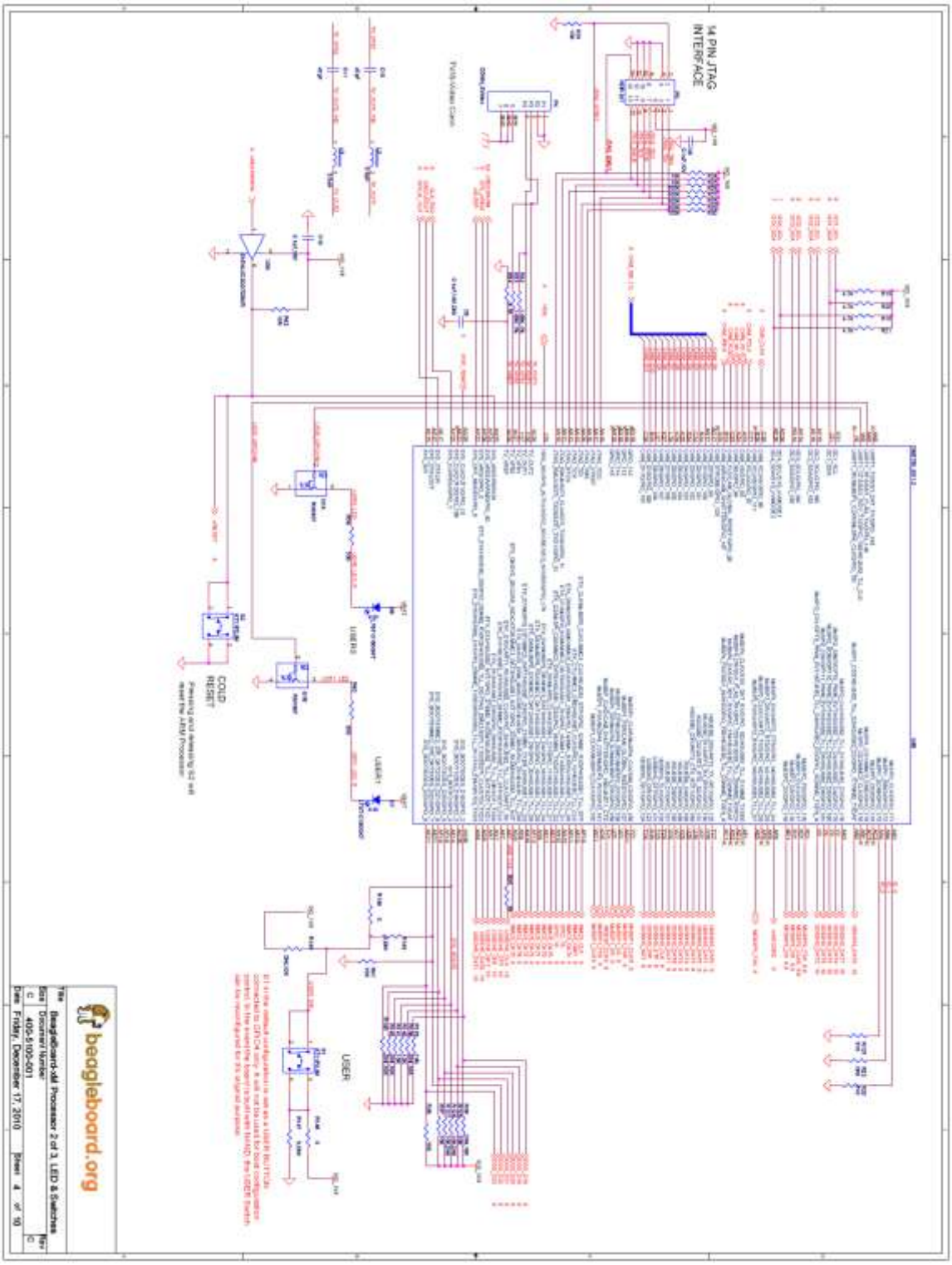
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COLD RESET
USER
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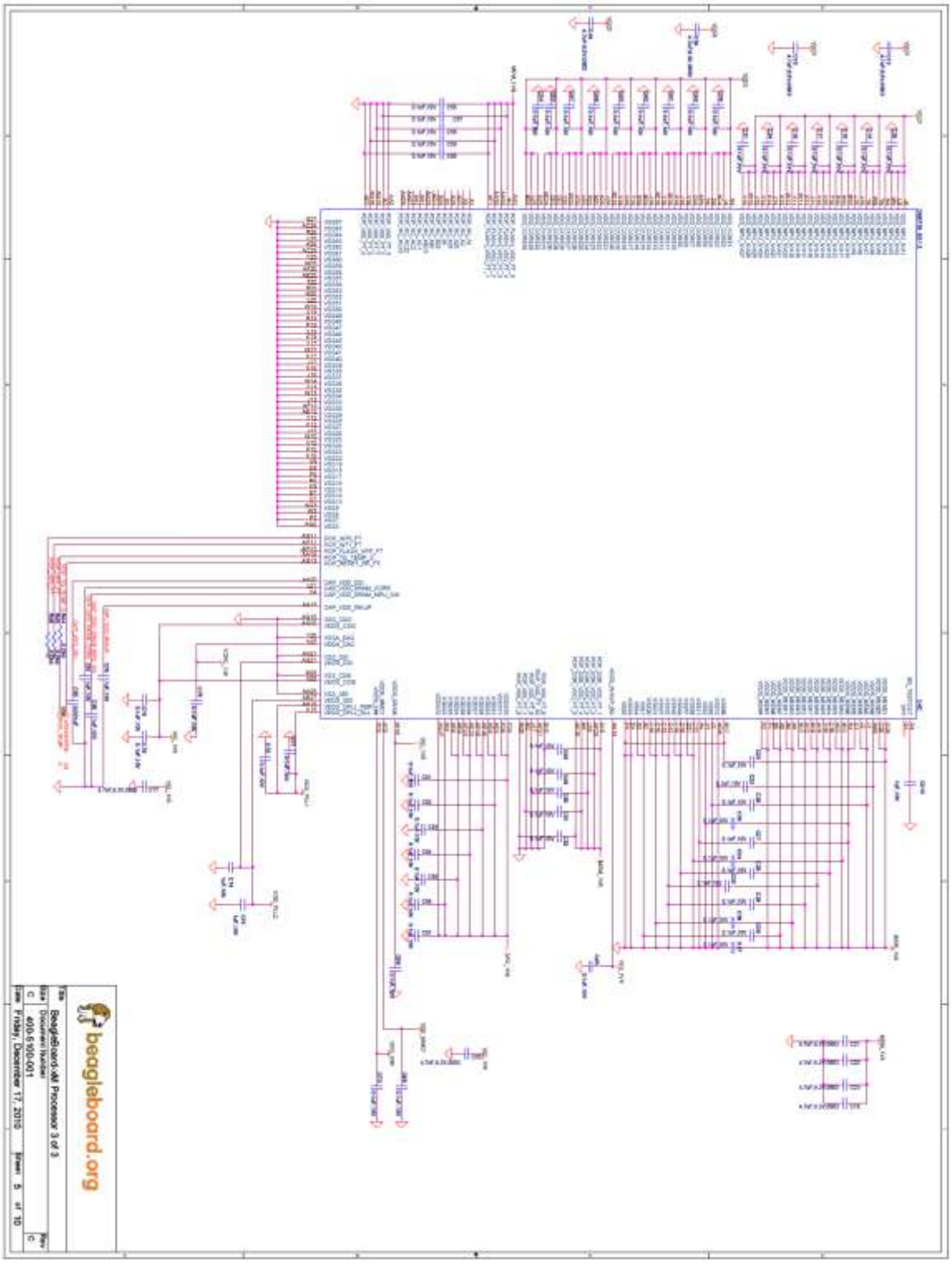
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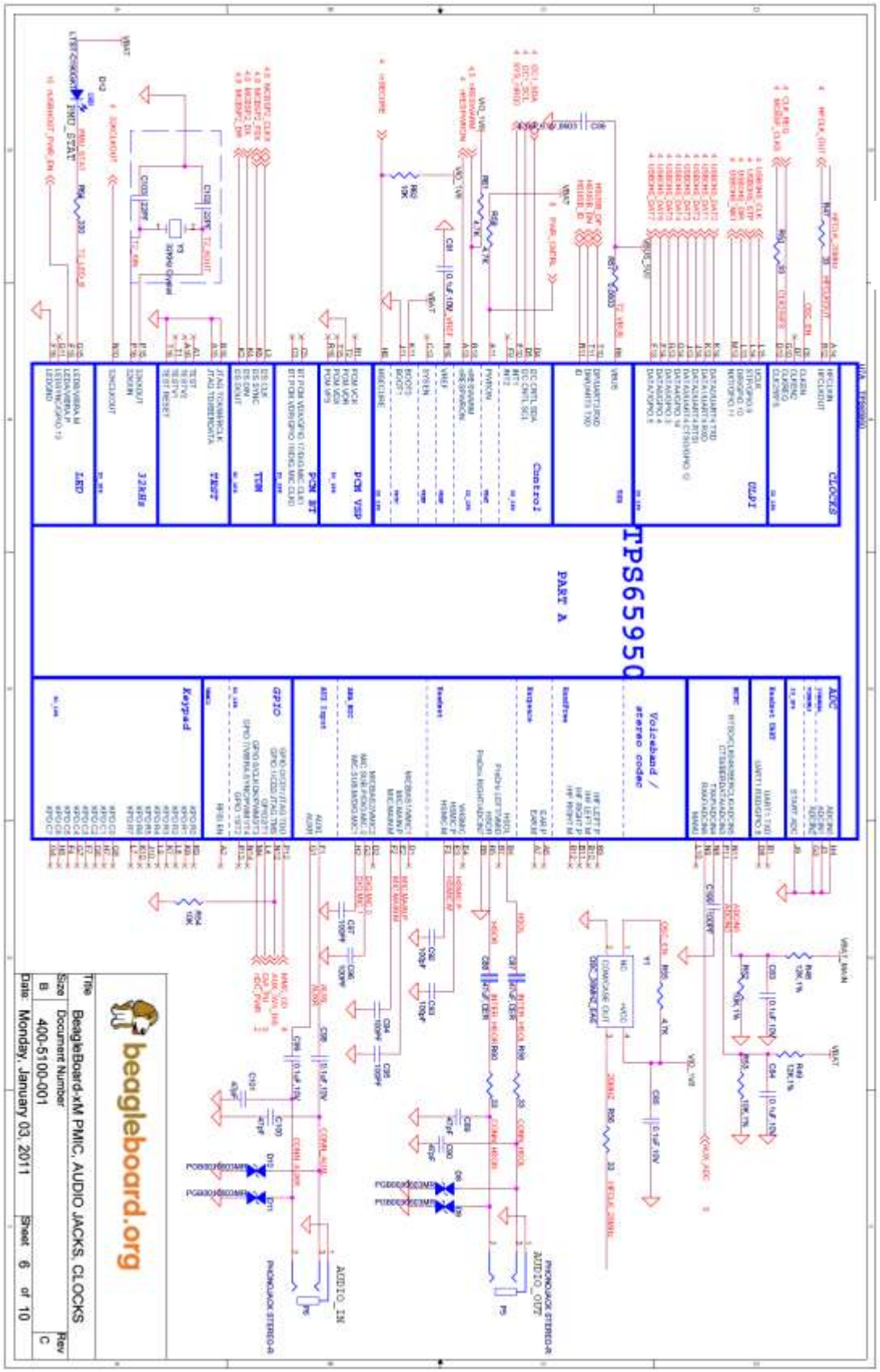
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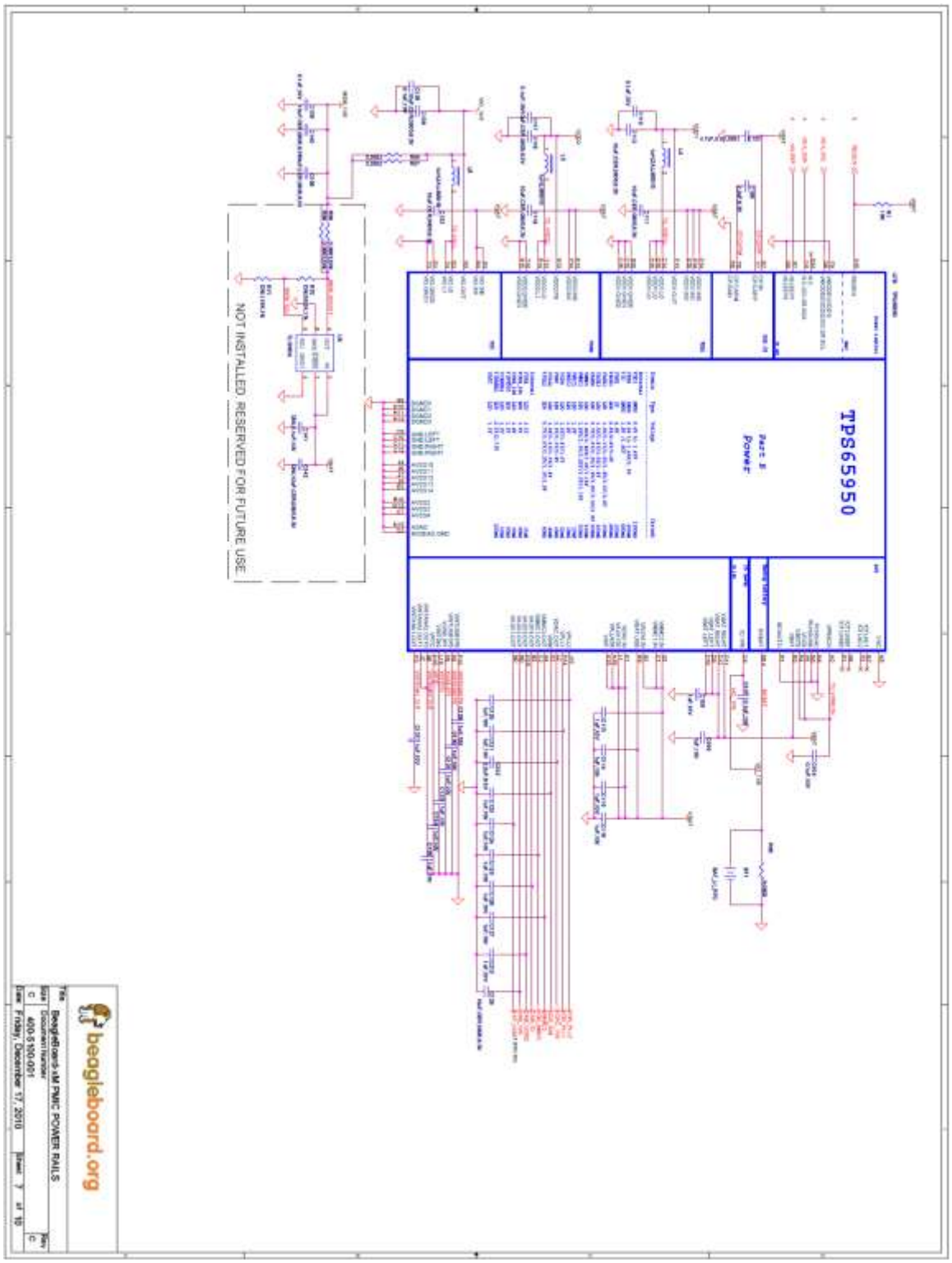
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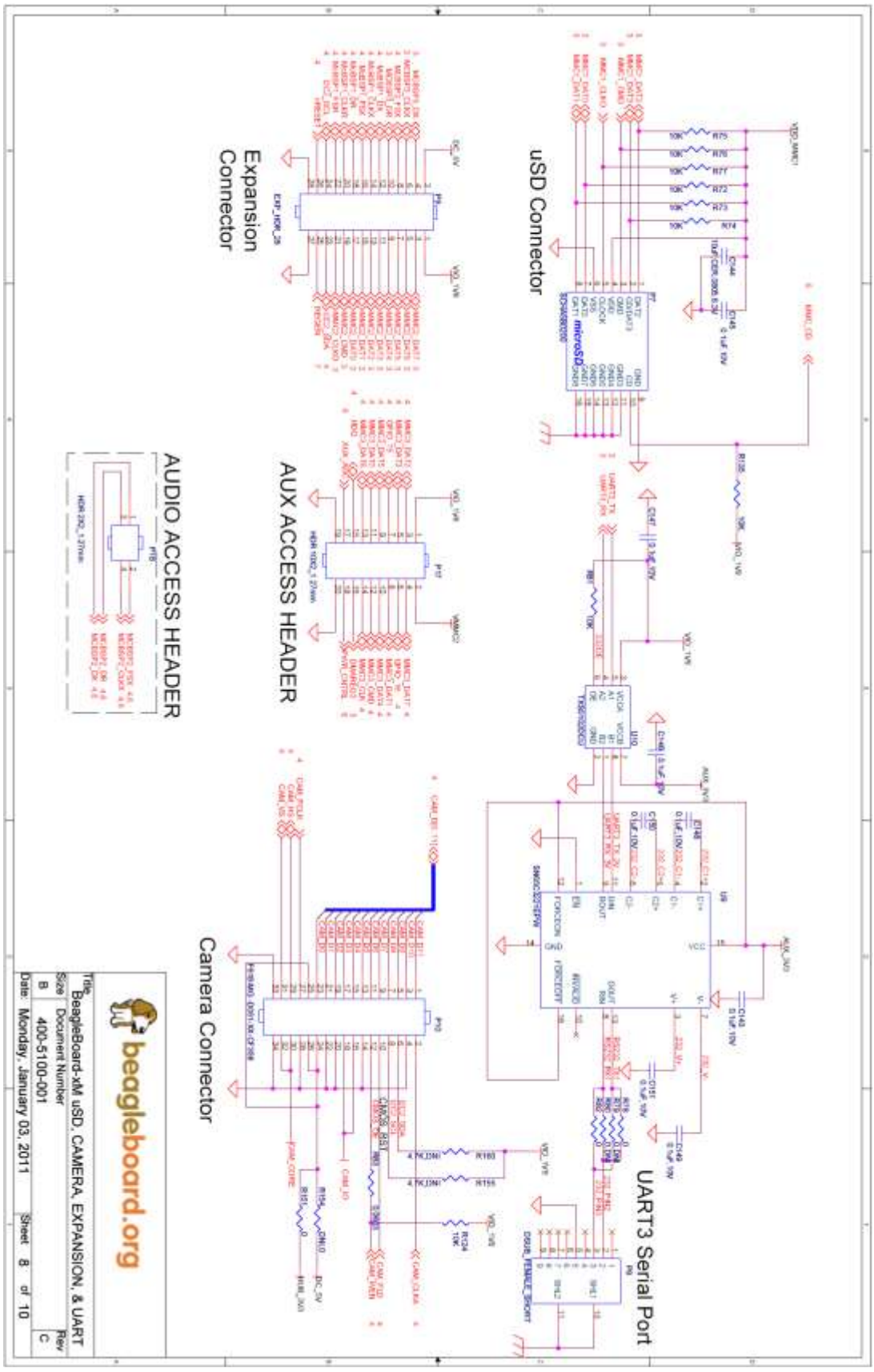
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Expansion Connector
AUX ACCESS HEADER
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Camera Connector
UART3 Serial Port
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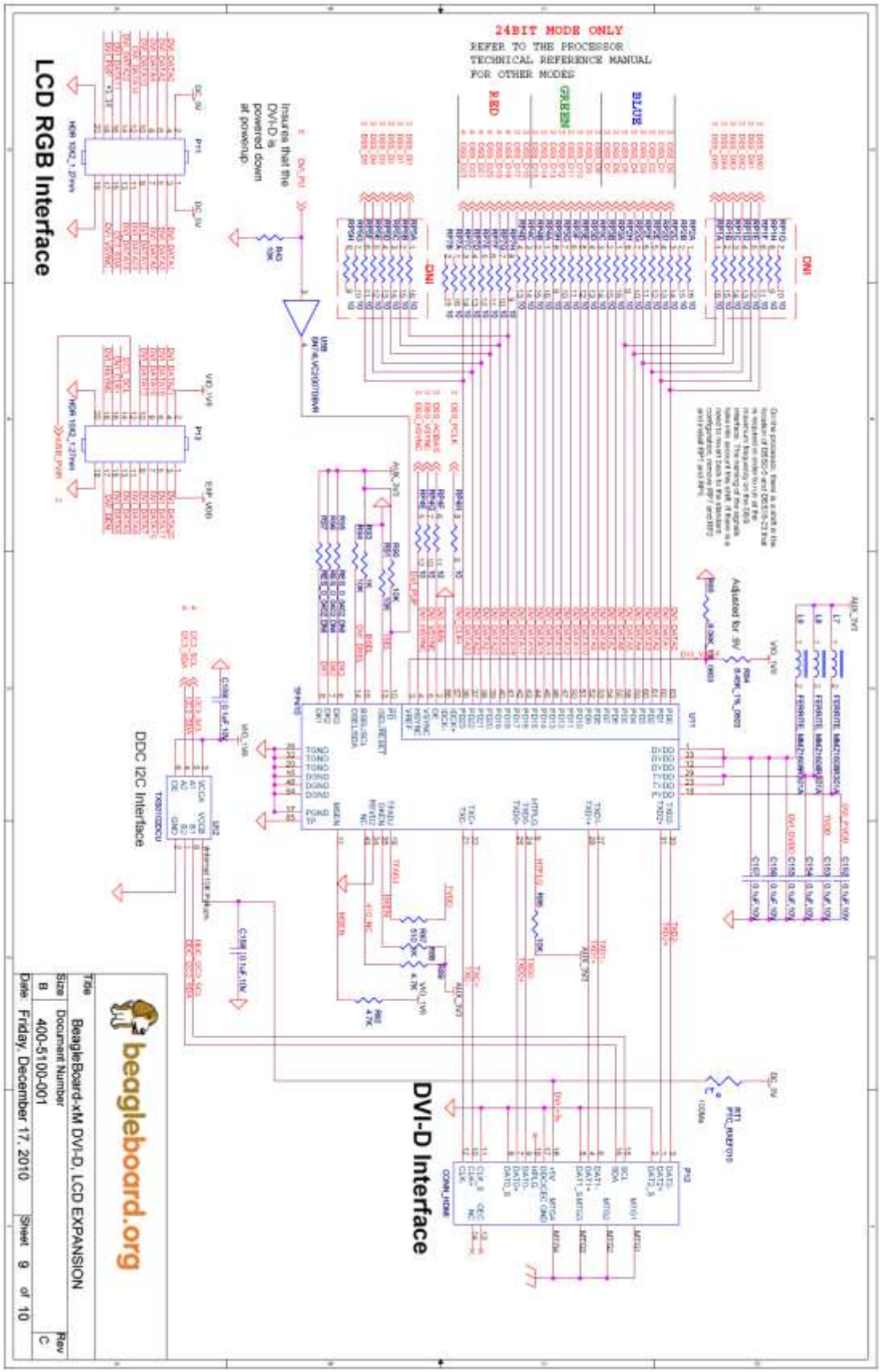
LCD RGB Interface
24BIT MODE ONLY
REFER TO THE PROCESSOR
TECHNICAL REFERENCE MANUAL
FOR OTHER MODES
RED
GREEN
BLUE
DNI
Ensures that the DVI-D is powered down at powerup.
DDC I2C Interface
DVI-D Interface
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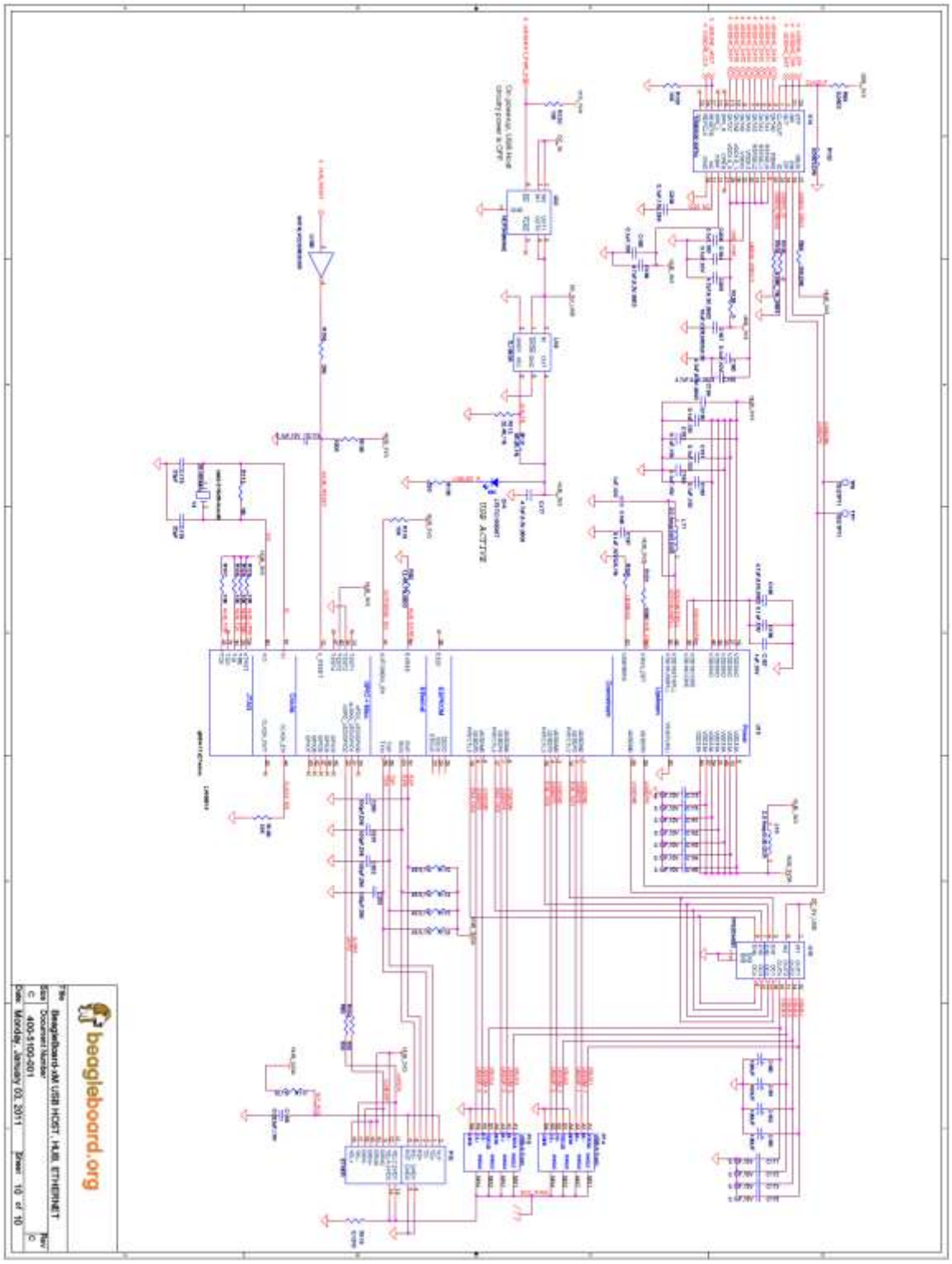
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## 15.0 Bills of Material

The Bill of Material for the Beagle Board is provided at BeagleBoard.org at the following location:

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## 16.0 PCB Information

The following pages contain the PDF PCB layers for the BeagleBoard. Gerber files and Allegro source files are available on BeagleBoard.org at the following address.

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