Nokia Siemens Networks

DX 200

BSC3153
Nokia GSM/EDGE BSS, Rel. BSS13, BSC and TCSM, Rel. S13, Product Documentation, v.1

TCSM2

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Contents

List of tables

List of figures

Summary of changes

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made to previous issues.

Changes for Issue 2-1 and 2-2

Information on TCSM2A-C has been removed.

Changes for Issue 2-0 and 2-1

Editorial changes made.

Changes between issues 1-0 and 2-0

Plug-in unit variants ET2E-T, ET2E-TC, and ET2A-T added. Changes to document structure and headings.

TC1C cartridge power supply

Section *Structure of the power supply* clarified.

Changes for Issue 1-0

TCSM2 replaces separate Functional Unit Descriptions earlier provided for both the TCSM2E and the TCSM2A. Online modifications.

1 TCSM2 overview

Purpose of TCSM2E

The second generation Transcoder and Submultiplexer (TCSM2E) is used in the GSM900/GSM1800/GSM1900 digital cellular network to provide transcoding function for traffic channels. This function is located in the Base Station Subsystem (BSS). The TCSM2E is used together with the Nokia DX 200 Base Station Controller (BSC) and Nokia BTS (Base Transceiver Station).

Although the TCSM2E units are functional units of the BSC, they can be physically located on either the BSC or MSC site.

The major telecommunications interfaces of the TCSM2E are the A interface towards the MSC and the Ater interface towards the BSC.

The capacity of a single TCSM2E is up to seven digital (MSC-side) trunks. The number of TCSM2E units serving a particular BSC is selected on the basis of the capacity of the BSC.

One individual block of the TCSM2E (per traffic channel) is called a Transcoding and Rate Adaptation Unit (TRAU). The TRAU function essentially includes converting the 64 kbit/s traffic channels arriving from the MSC into channels of 8 kbit/s, 16 kbit/s, 32 kbit/s, or 64 kbit/s rate and further multiplexing these channels to fit in the timeslots of the trunk towards the BSC. The other direction (BSC to MSC) works according to the same principle (in reverse).

The operation and maintenance functions of the TCSM2E are co-ordinated using the BSC.

The telecommunications functions of the TCSM2E are:

- transcoding and rate adaptation of traffic channels carried between the BTS and the TRAU
- submultiplexing of 8 kbit/s, 16 kbit/s, 32 kbit/s, or 64 kbit/s capacity TRAU frame channels onto 64 kbit/s time slots
- through-connection of selected entire time slots
- providing the interface functions for the T1 lines
- receiving of clock synchronisation from the MSC direction trunks and being part of the synchronisation chain extending down to the BTSs

Purpose of TCSM2A

The Nokia DX 200 Second Generation Transcoder and Submultiplexer (TCSM2A) is used in the GSM900/GSM1800/GSM1900 digital cellular network to provide transcoding of traffic channels. This function is located in the Base Station Subsystem (BSS). The TCSM2A is used together with the Nokia DX 200 BSC and the Nokia Base Transceiver Station (BTS).

A configuration is also possible, in which a TCSM2A (with a T1 interface) is used in a GSM 1800 network (which is a European system).

The TCSM2A units are functional units of the BSC, but they can be physically located at either the BSC or the MSC site.

The major telecommunication interfaces of the TCSM2A are the A interface towards the MSC and the Ater interface towards the BSC.

The capacity of a single TCSM2A is up to seven T1 (MSC-side) trunks. The number of TCSM2A units serving a particular BSC will depend on the capacity of the BSC.

An individual block of the TCSM2A (per traffic channel) is called a Transcoding and Rate Adaptation Unit (TRAU). The TRAU converts the 64 kbit/s traffic channels arriving from the MSC into channels with a 16 kbit/s or 8 kbit/s rate. It also multiplexes these channels to fit in the time slots of the trunk, towards the BSC. The other direction (BSC to MSC) works according to the same principle (in reverse).

The operation and maintenance functions of the TCSM2A are co-ordinated with the BSC.

Telecommunication functions of the TCSM2A are listed below:

- transcoding and rate adaptation of traffic channels carried between the BTS and the TRAU
- submultiplexing of 8 kbit/s, 16 kbit/s, 32 kbit/s, or 64 kbit/s capacity TRAU frame channels onto 64 kbit/s time slots
- through-connection of selected entire time slots
- providing the interface functions for the T1 lines
- receiving of clock synchronisation from the MSC direction trunks and being part of the synchronisation chain extending down to the BTSs

Operating environment of TCSM2 (ETSI)

The TCSM2E is connected with 2048 kbit/s trunks to the MSC (A interface) as well as the BSC (Ater interface). The LAPD O&M connection with the BSC uses part of the BSC-side trunk capacity.

The figure below shows the operating environment of the TCSM2E.

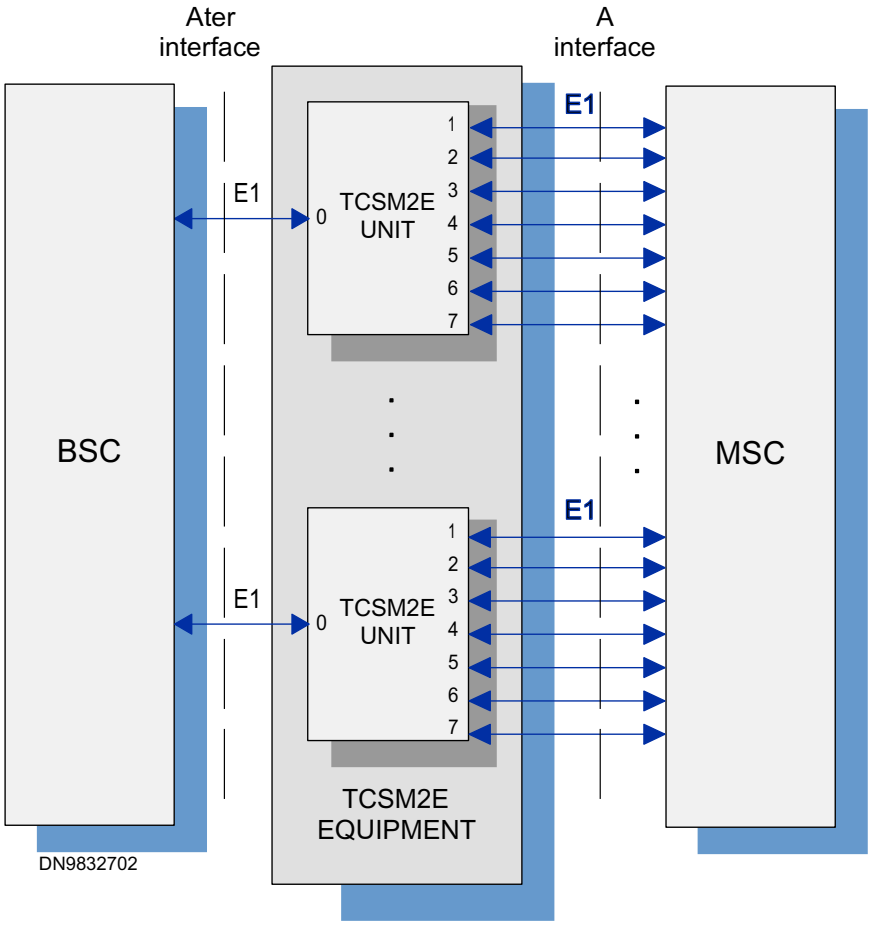

Figure 1. The operating environment of the TCSM2E

Interface to the MSC

The interface to the MSC consists of one or more digital 2048 kbit/s trunks. The synchronisation for the TCSM2E is extracted from a trunk signal from the MSC. The gross bit rate of the traffic channel is 64 kbit/s. The PCM coding follows A-law. Signalling related to call-handling is provided by Common Channel Signalling (CCS) at a bit rate of 64 kbit/s.

Interface to the BSC

The interface to the BSC is a digital 2048 kbit/s trunk. The bit rate of a traffic channel is either 8, 16, 32, or 64 kbit/s. A number of 16 kbit/s streams is, however, reserved for HSCSD connections.

Timeslot Allocations

The routing of signals between the BSC-side and MSC-side trunk interfaces is controlled by the chosen timeslot allocation. Different allocations can be programmed and loaded into the TCSM2E. The selected allocation type must also be supported by the BSC. Different TCSM2Es of the same BSS may use different allocations.

Each Ater trunk may carry different channels. Each of the A interface PCMs can be individually programmed to the appropriate circuit type. The maximum number of A interface PCMs supported by a TCSM2E is dependent on the circuit types.

For Full Rate (FR) traffic use, the TCSM2E uses an allocation with 16 kbit/s traffic channels. Half Rate (HR) traffic uses either an allocation with 16 kbit/s or an allocation with 8 kbit/s traffic channels. High Speed Circuit Switched Data (HSCSD) connections consist of one to four 16 kbit/s streams over the Ater interface.

The TCSM2E is capable of using mixed allocations, with the BSC-side trunk capacity divided into separate 16 kbit/s and 8 kbit/s portions of channels.

A number of 64 kbit/s timeslots can be configured to be through-connected transparently (Common Channel Signalling, O&M connection, and so on) between one of the MSC-side lines and the BSC-side line.

For examples of all the allocations, see the *Product Description for TCSM2A and TCSM2E*.

TRAU interface

A single TCSM2E can operate in different transcoding function modes, depending on the DSP program variant. The basic program performs full rate (FR) transcoding (13 kbit/s speech channel / 16 kbit/s TRAU frame) and half rate (HR) transcoding (5.6 kbit/s speech channel / 8 kbit/s TRAU frame). Different transcoding programs can coexist in the DSP memory, and depending on the transcoding type they are invoked either by command or automatically based on the received TRAU frame type.

Operating environment of TCSM2 (ANSI)

The TCSM2A is connected with 1544 kbit/s trunks to the MSC (A interface) as well as the BSC (Ater interface). The LAPD O&M connection with the BSC uses part of the BSC-side T1 line capacity.

The figure below shows the operating environment of the TCSM2A.

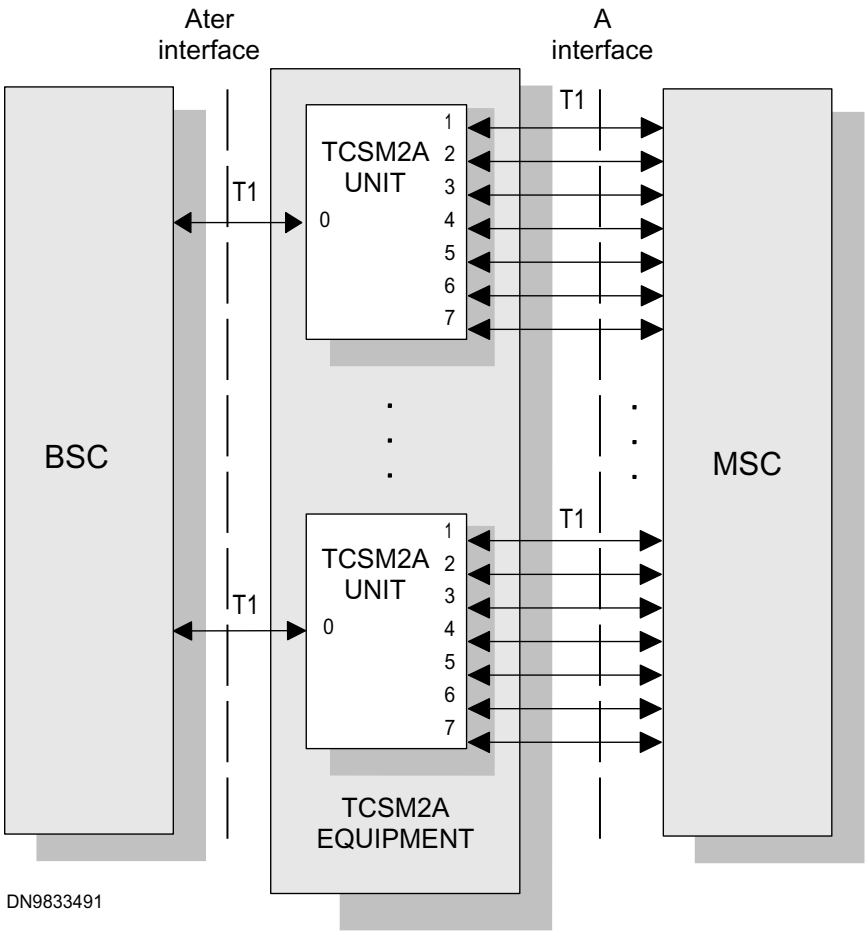

Figure 2. The operating environment of the TCSM2A

Interface to the MSC

The interface to the MSC consists of one or more T1 lines (Digital signal level 1, DS1). The synchronisation for the TCSM2A is extracted from a T1 signal from the MSC. The gross bit rate of the traffic channel is 64 kbit/s. For PCM coding, either A-law or µ-law can be selected. Call-handling-related signalling is provided by Common Channel Signalling (CCS) at a 64 kbit/s or 56 kbit/s rate.

Interface to the BSC

The interface to the BSC is a DS1 signal. The bit rate of one traffic channel is either 8, 16, 32, or 64 kbit/s. A number of 16 kbit/s streams is, however, reserved for High Speed Circuit Switched Data (HSCSD) connections.

Time slot allocations

The routing of signals between the BSC-side and MSC-side trunk interfaces is controlled by the chosen time slot allocation. Different allocations can be programmed and loaded into the TCSM2A. The selected allocation type must also be supported by the BSC. Different TCSM2As of the same BSS may use different allocations.

Each Ater trunk may carry different channels. Each of the A interface PCMs can be individually programmed to the appropriate circuit type. The maximum amount of A interface PCMs supported by a TCSM2E is dependent on the circuit types.

For Full Rate (FR) traffic use, the TCSM2A uses an allocation with 16 kbit/s traffic channels. HSCSD connections consist of one to four 16 kbit/s streams over the Ater interface.

The TCSM2A is capable of using mixed allocations, with the BSC-side T1 line capacity divided into separate 16 kbit/s and 8 kbit/s portions of channels.

A number of 64 kbit/s time slots can be configured to be through-connected transparently between an MSC-side line and a BSC-side line (Common Channel Signalling, O&M connection, and so on).

For examples of all the allocations, see the *Product Description for TCSM2A and TCSM2E*.

TRAU interface

A single TCSM2A can operate in different transcoding function modes, depending on the DSP program variant. The basic program performs Full Rate (FR) transcoding (13 kbit/s speech channel / 16 kbit/s TRAU frame) and Half Rate (HR) transcoding (5.6 kbit/s speech channel / 8 kbit/s TRAU frame). Different transcoding programs can coexist in the memory of the transcoder and, depending on the transcoding type, they are invoked either by command or automatically - based on the received TRAU frame type.

For more information, see:

TC1C cartridge power supply

TC1C and ET1TC cartridge intermediate cabling

Logical structure of TCSM2

Mechanical structure of TCSM2

Plug-in units of TCSM2

Operation of TCSM2

Power consumption of TCSM2

2 Logical structure of TCSM2

Block structure (ETSI)

Each TCSM2E unit of a particular BSC is independent of the others, even if located in the same rack. The figure below shows the block diagram of the TCSM2E unit. The unit consists of four main blocks:

- the Transcoder Controller plug-in unit (TRCO)
- a number (maximum 14) of Transcoder plug-in units (TR16-S)
- the Power Supply Converter plug-in unit (PSC1/PSC1-S) that supplies the +5 V and -5 V operating voltages to the TRCO and TR16-Ss
- the Exchange Terminal plug-in units, ET2E(-S/-T)

The TRCO incorporates a microcomputer that controls and supervises the operation of the TCSM2E.

The TRAU functions (16 channels) are performed by 16 DSPs in the TR16-S unit.

The TCSM2E has up to seven trunk interfaces towards the MSC and one trunk interface towards the BSC. The functions related to the line interfaces are handled in the ET2E(-S/-T) plug-in unit (two trunk interfaces per unit).

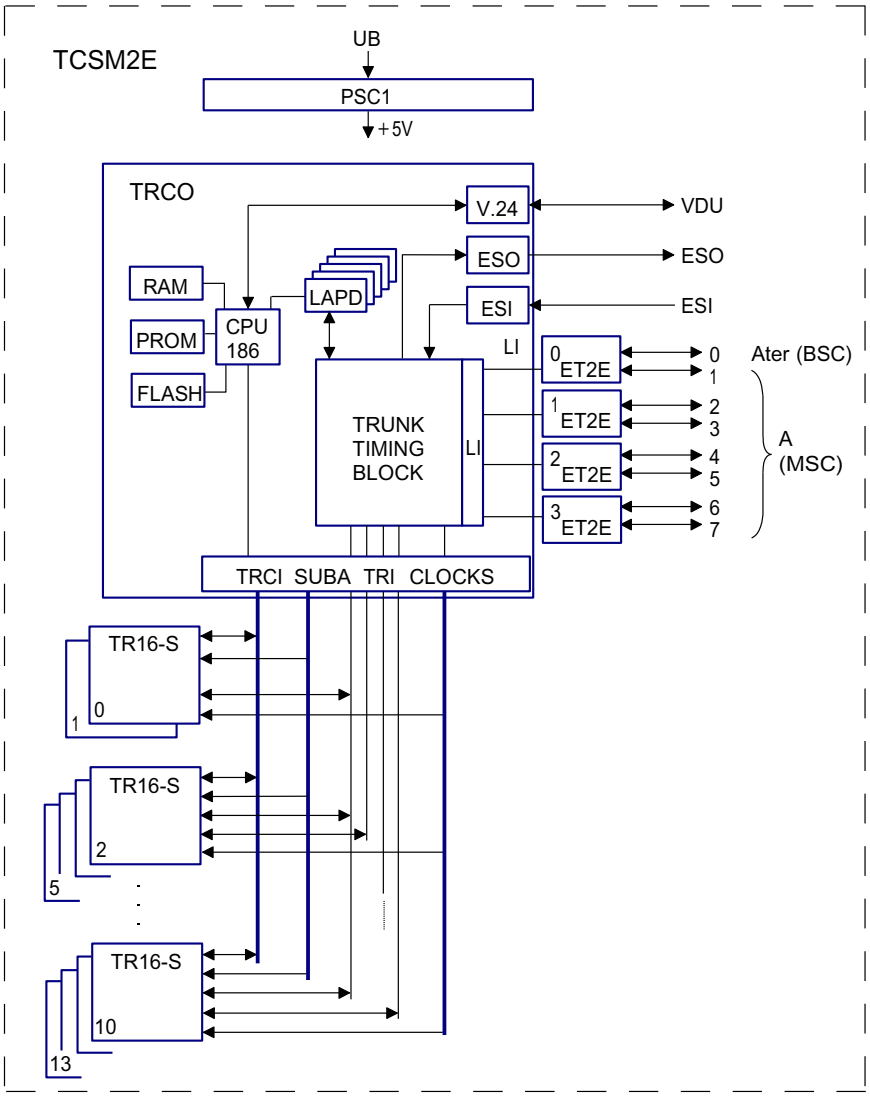

Figure 3. TCSM2E block diagram

Block structure (ANSI)

Each TCSM2A unit of a particular BSC is independent of the others, even if located in the same rack. The figure below shows a block diagram of the TCSM2A unit. The unit consists of four main blocks:

- the Transcoder Controller plug-in unit (TRCO)
- up to 14 Transcoder plug-in units (TR12-T)
- the Power Supply Converter plug-in unit (PSC1/PSC1-S) that supplies the +5 V and -5 V operating voltages to the TRCO and TR12-Ts
- Exchange Terminal plug-in units ET2A(-T)
- ET2E(-S/-T) plug-in units

The TRCO incorporates a microcomputer that controls and supervises the operation of the TCSM2A.

The TRAU functions (12 channels) are performed by 12 DSPs in the TR12-T units.

The TCSM2A has up to seven DS1 ports towards the MSC and one DS1 port interface towards the BSC. The functions related to the line interfaces are handled in the ET2A(-T) plug-in unit (two DS1 ports per unit). Functions related to the E1 line interfaces are handled by the ET2E(-S/-T) unit.

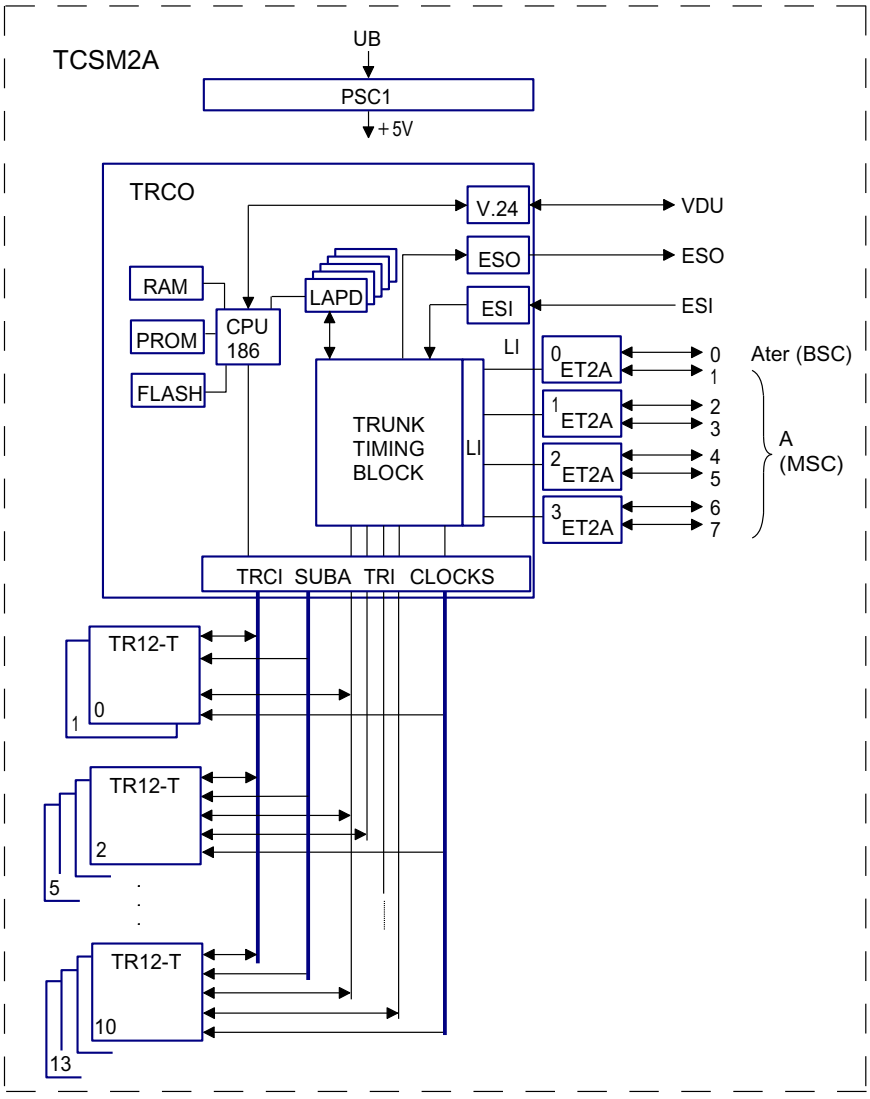

Figure 4. TCSM2A block diagram

3 Mechanical structure of TCSM2

Plug-in units

The plug-in units follow the hardware model of the DX 200 system.

The plug-in unit sizes (H × W × D) are:

- TRCO, TR12-T, TR16-S: 233.4 mm × 4 TE × 220 mm (9.2 in. × 0.8 in. × 8.7 in.)
- PSC1: 233.4 mm × 5 TE × 220 mm (9.2 in. × 1.0 in. × 8.7 in.)
- ET2A(-T), ET2E(-S/-T): 100 mm × 4 TE × 220 mm (3.9 in. × 0.8 in. × 8.7 in.)

TC1C cartridge (ETSI)

The dimensions of the TC1C cartridge are (H × W × D):

- 262 mm × 360 mm × 300 mm

The cartridge is equipped with the PSC1, the TRCO, and up to 14 TR16-S plug-in units. The figure below shows the equipping principle of the cartridge.

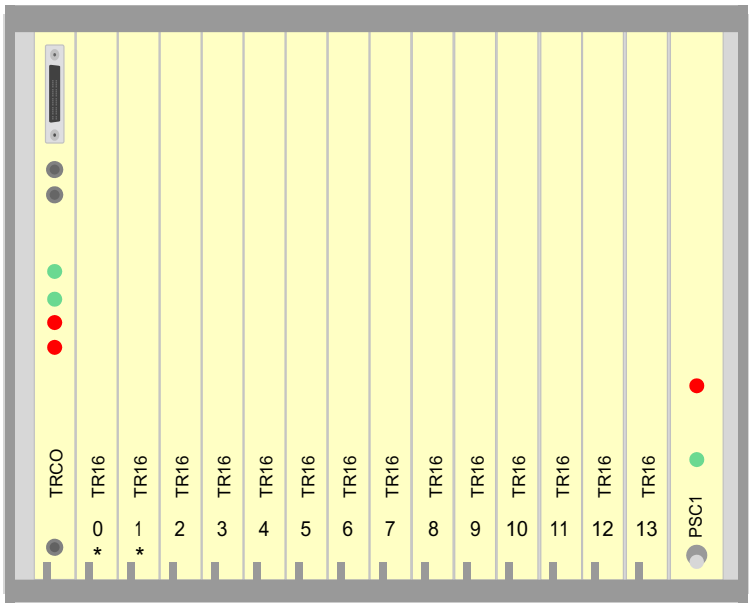

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Figure 5. TC1C cartridge (maximum configuration)

ET1TC cartridge (ETSI)

The dimensions of the ET1TC cartridge are (H × W × D):

- 262 mm × 120 mm × 300 mm

The cartridge houses eight ET2E(-S/-T) plug-in units equipped onto two layers, four in each layer. See the figure below.

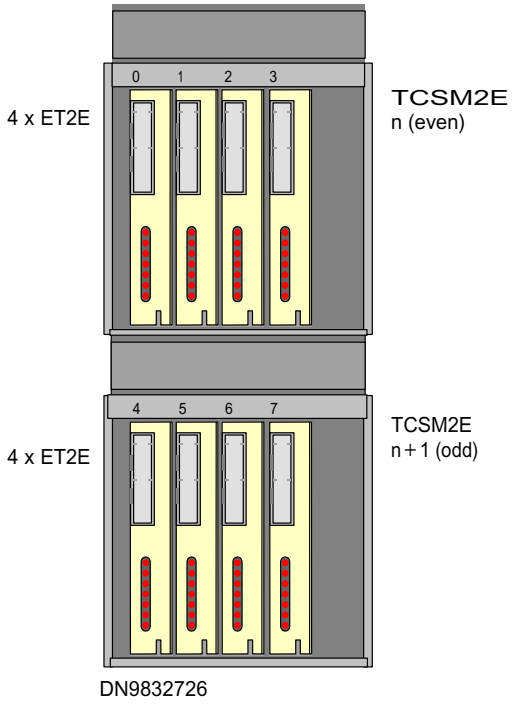

Figure 6. Equipping of the ET1TC (maximum configuration)

TC1C cartridge (ANSI)

The dimensions of the TC1C cartridge are (H × W × D): 262 mm × 360 mm × 300 mm (10.3 in. × 14.2 in. × 11.8 in.).

The cartridge is equipped with a PSC1, a TRCO, and up to 14 TR12-T plug-in units. The figure below shows the equipping principle of the cartridge.

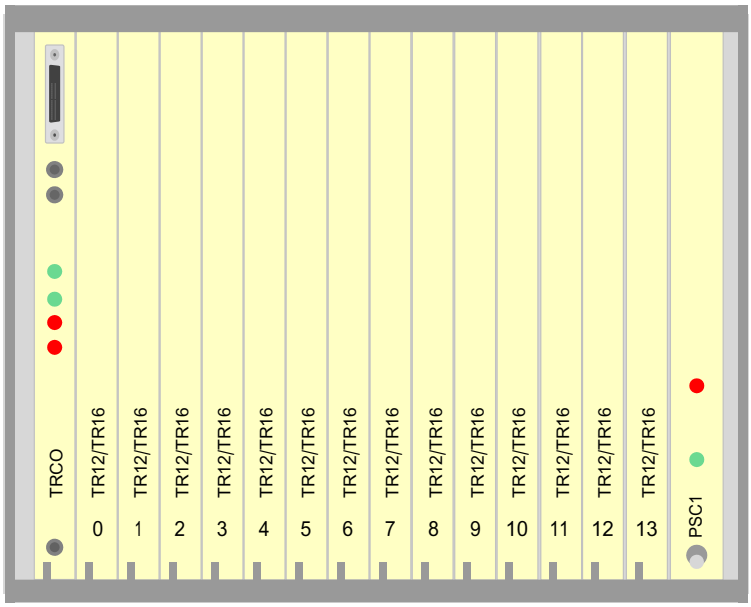

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Figure 7. TC1C cartridge maximum configuration

ET1TC cartridge (ANSI)

Dimensions of the ET1TC cartridge are (H × W × D): 262 mm × 120 mm × 300 mm (10.3 in × 4.7 in × 11.8 in). The cartridge houses eight ET2A(-T) plug-in units equipped onto two layers, four in each. See the figure below.

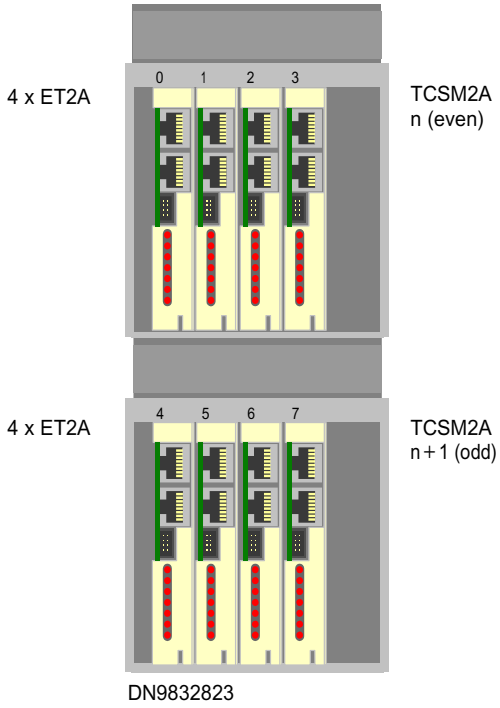

Figure 8. Equipping of the ET1TC (maximum configuration)

Dimensioning (ETSI)

The table below shows how the TCSM2E capacity depends on the number of equipped plug-in units. Capacity is increased by adding TCSM2E units.

Table 1. TCSM2E capacity

Plug-in unit	Capacity unit on Ater: 16 kbit/s (Circuit types A, C)	Capacity unit on Ater: 8 kbit/s (Circuit type B)	Capacity unit on Ater: 2 x 16 kbit/s (Circuit type D)	Capacity unit on Ater: 4 x 16 kbit/s (Circuit type E)
TR16-S	*)	2...14	2...4	2
	2...6			
	2...8			
ET2E(-S/-T)	*)	1...4	1...2	1
	1...2			
	1...3			

Table 1. TCSM2E capacity (cont.)

Plug-in unit	Capacity unit on Ater: 16 kbit/s (Circuit types A, C)	Capacity unit on Ater: 8 kbit/s (Circuit type B)	Capacity unit on Ater: 2 x 16 kbit/s (Circuit type D)	Capacity unit on Ater: 4 x 16 kbit/s (Circuit type E)
TCH	*) 29...90 or 29...120	29...210	29...60	30

*)
If BSC-side submultiplexing is carried out by the SMUX unit and three PCMs are multiplexed onto Ater.

In the table above, TCH stands for traffic channel. For the meaning of the circuit types A, B, C, D, E, and F, please refer to the *Product Description for TCSM2E*. In calculating the minimum traffic channel capacities, it is assumed that each CCS signalling and X.25 O&M channel reserves one time-slot per Ater-line. However, in calculating the maximum capacities, no allowance is made for CCS or X.25.

Dimensioning (ANSI)

The table below shows how the TCSM2A capacity depends on the number of equipped plug-in units. The capacity can be increased by adding more TCSM2A units.

Table 2. TCSM2A capacity

Plug-in unit	Capacity unit on Ater: 16 kbit/s (Circuit types A, C)	Capacity unit on Ater: 8 kbit/s (Circuit type B)	Capacity unit on Ater: 2 x 16 kbit/s (Circuit type D)	Capacity unit on Ater: 4 x 16 kbit/s (Circuit type E)
TR12-T	2 to 8	2 to 14	2 to 4	2
ET2A(-T)	1 to 3	1 to 4	1 to 2	1
TCH	23 to 95	22 to 166	24 to 47	23

In the above table, TCH stands for traffic channels. The circuit types A, B, C, D, and E are explained in the *Product Description for TCSM2A*. In calculating the minimum traffic channel capacities, it is assumed that each CCS signalling and X.25 O&M channel reserves one time slot per Ater line. In calculating the maximum capacities, however, no allowance is made for CCS or X.25.

4 Plug-in units of TCSM2

For more information on the individual plug-in units, see the following Plug-in Unit Descriptions or Sections:

Transcoder Controller plug-in unit (TRCO)

TRCO

Exchange Terminal plug-in unit, ET2A/ET2A-T (ANSI)

ET2E-T, ET2E-TC, ET2A-T, ECE2, ECE2-C, ECE2-A

Exchange terminal plug-in unit, ET2E/ET2E-S/ET2E-T (ETSI)

ET2E-T, ET2E-TC, ET2A-T, ECE2, ECE2-C, ECE2-A

Exchange Terminal plug-in unit, ET2E/ET2E-S/ET2E-T (ANSI)

ET2E-T, ET2E-TC, ET2A-T, ECE2, ECE2-C, ECE2-A

Transcoder plug-in unit, TR16-S (ETSI)

TR12-S, TR12-T, TR16, TR16-S

Transcoder plug-in unit, TR12-T (ANSI)

TR12-S, TR12-T, TR16, TR16-S

Power supply plug-in unit (PSC1)

PSC1

5 Operation of TCSM2

For more information on the operation of the individual plug-in units of the TCSM2, see the following Plug-in Unit Descriptions or Sections:

Jumper settings

Note

No settings are needed for the TC1C or ET1TC cartridges.

Jumper settings of TRCO C08773

Jumper settings of ET2A-T, ECE2-A

Jumper settings of ET2E-T, ECE2

Jumper settings of ET2E-TC, ECE2-C

Jumper settings of TR12-S, TR12-T, TR16, TR16-S

Front panel swithes and LED indicators of the plug-in units

Operation of TRCO

Operation of ET2E-T, ET2E-TC, ET2A-T, ECE2, ECE2-C, ECE2-A

Operation of TR12-S, TR12-T, TR16, TR16-S

Operation of PSC1

See also:

Intermediate cabling of cartridges TC1C and ET1TC

TC1C and ET1TC intermediate cabling

Power supply

TC1C cartridge power supply

6 Internal interfaces

Transcoder interface (TRI)

Four TRI (Transcoder interface) serial interface buses transfer the signals of the traffic channels and through-connected time slots at a bit rate of 4096 kbit/s between the TRCO and the TR12-Ts. The TRI signals are composed of two 2048 kbit/s signals. The table below shows the mapping of the TRI signals to the Line Interface (LI) signals (see Line interface (LI) and to the DS1 ports. For more information, see *6.1 Line interface (LI)*.

The interfaces are synchronised to the master 8192 kHz and 8 kHz clock signals of the TRCO. The TRI signals thus have equal phasing with respect to one another. The figure *9 Timing diagram of the TRI-interface* shows which DSP of which TR12-T unit handles a particular time slot of the TRI.

Table 3. Mapping of the TRI interface time-slots to the LI interfaces, to the ET2A(-T) units and to the Ater and A interfaces

TRI number	LI number	ET2A(-T) number and trunk I/F within ET2A(-T)	Interface number
TRI-0	LI-0	0	Ater I/F
Even time slots	Even time slots	0	
TRI-0	LI-0	0	A I/F 1
Odd time slots	Odd time slots	1	
TRI-1	LI-1	1	A I/F 2
Even time slots	Even time slots	0	
TRI-1	LI-1	1	A I/F 3
Odd time slots	Odd time slots	1	
TRI-2	LI-2	2	A I/F 4
Even time slots	Even time slots	0	

Table 3. Mapping of the TRI interface time-slots to the LI interfaces, to the ET2A(-T) units and to the Ater and A interfaces (cont.)

TRI number	LI number	ET2A(-T) number and trunk I/F within ET2A(-T)	Interface number
TRI-2	LI-2	2	A I/F 5
Odd time slots	Odd time slots	1	
TRI-3	LI-3	3	A I/F 6
Even time slots	Even time slots	0	
TRI-3	LI-3	3	A I/F 7
Odd time slots	Odd time slots	1	

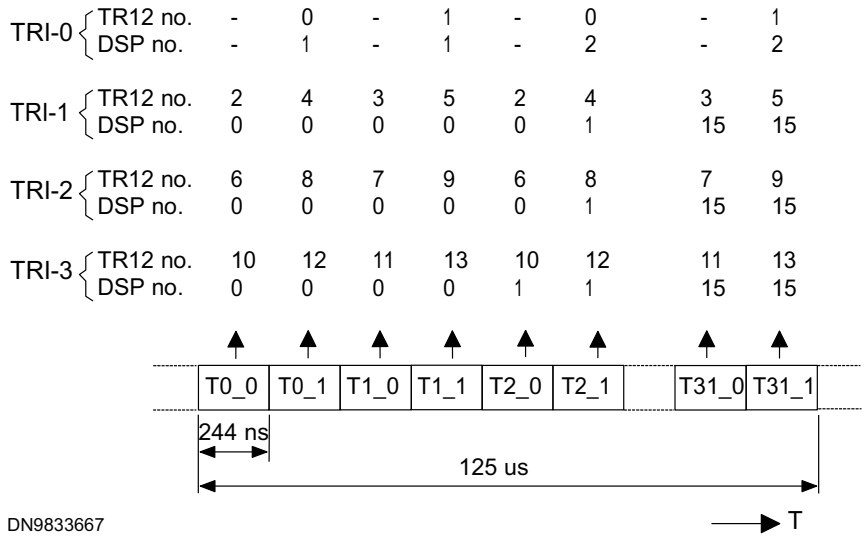

Figure 9. Timing diagram of the TRI-interface

In the figure above, *Tx_y* means time-slot *x* of sub-signal *y*. For example, *T1_0* is time-slot *1* of sub-signal *0*. The buses are driven by asymmetrical driver circuits. See the following figure. It shows the principle of the electrical connection of the signals of the TRI-interface. The connection of 8MHz and 8kHz clocks is presented, but they also provide timing to the SUBA bus.

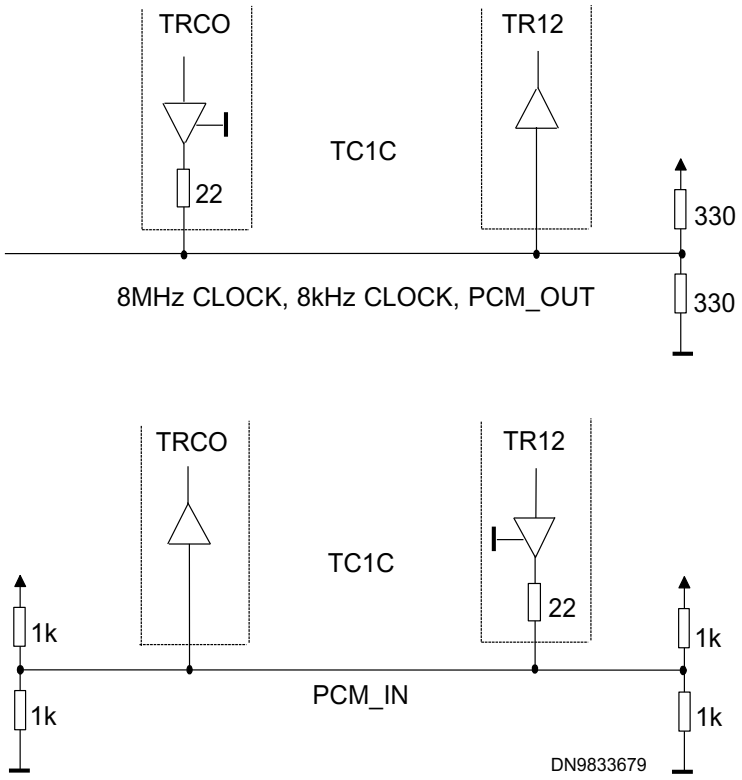

Figure 10. Electrical connection principle of TRI-interface signals

TRCI-bus

The TRCI (Transcoder Control Interface) is a bi-directional internal bus. The bus transfers the control (operating mode settings, for example) and supervision messages (alarms and indications) between the TRCO and the TR12-T plug-in units as well as the program code of the TR12-T units.

The TRCI consists of an address part, an 8-bit data part and a control part. The TRCO is the master, and all the TR12-Ts are slaves on the bus. The bus signals are driven by asymmetric driver circuits. The figure below shows the electrical connection.

Via this bus, the TRCO can supervise that the TR12-T obeys the data switching function, as commanded via the SUBA bus. The functioning of the SUBA-bus and TRCI-bus can thus be supervised.

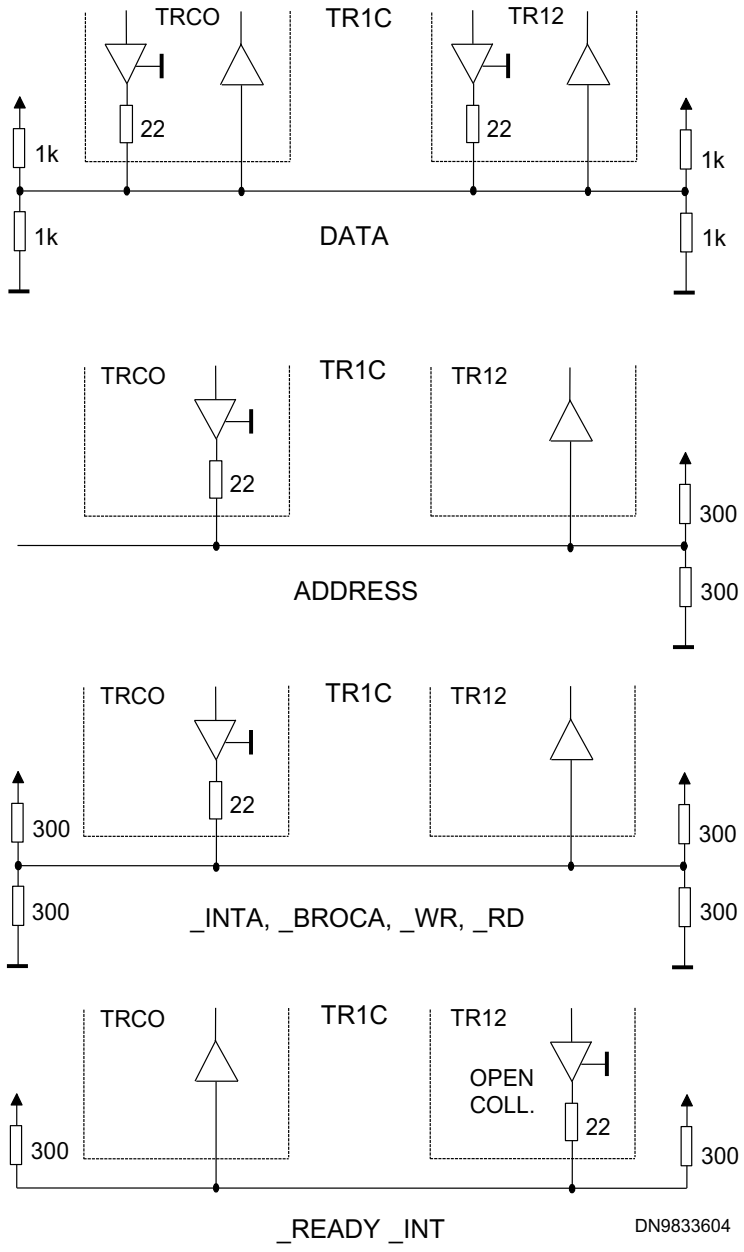

Figure 11. Principle of the electrical connection of the TRCI bus signals

Submultiplexing Address Bus (SUBA)

The SUBA-bus is a uni-directional 8-bit parallel bus. It controls the data switching function of each DSP in each TR12-T plug-in unit, in real time. The DSPs transmit their data signals to the different bit positions of the BSC-side internal trunk, based on the control information received over the SUBA bus. The interface is synchronised to the master 8192 kHz and 8 kHz clock signals of the TRCO, so that the data is written to the bus at instants when each time slot position starts. The figure below shows the timing diagram of the bus.

The bus signals are driven by asymmetric driver circuits. See the figures below.

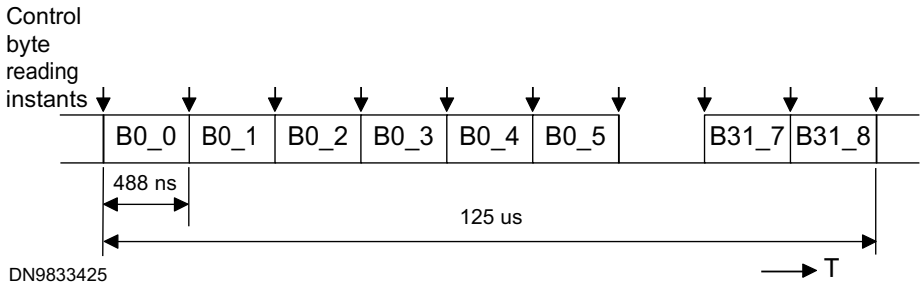

Figure 12. Timing diagram of the SUBA-bus (Bx_y means bit y of time slot x)

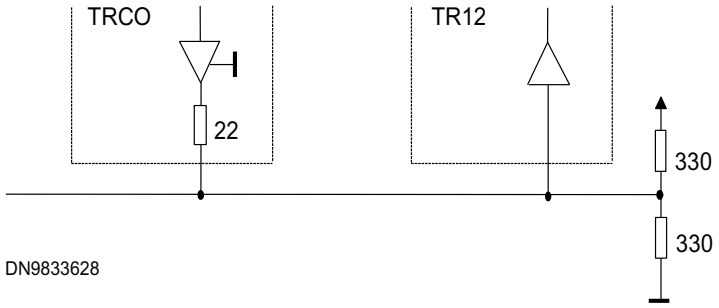

Figure 13. Principle of the electrical connection of the SUBA-bus

Line interface (LI)

Traffic and clock signals between the TRCO and ET2A(-T)/ET2E(-S/-T) are carried over the Line Interface (LI). In addition, the O&M link for the ET2A(-T)s uses time slot 0 of the 2048 kbit/s signal *0* (the first 2048 kbit/s signal of ET2A or ET2A-T). The program code is also loaded over this time slot. The figure below shows the timing diagram.

The LI signals are connected with a cable between the TC1C and ET1TC cartridges. The signals of the LI are driven by symmetric driver circuits. See the figure below.

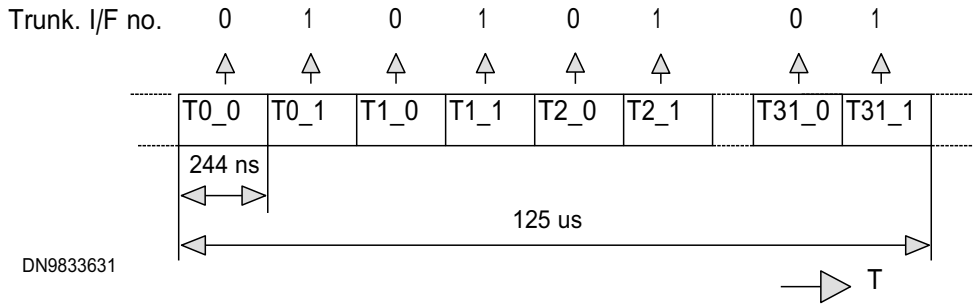

Figure 14. Timing diagram of the LI (Tx_y denotes time slot x of sub-signal y (0 or 1). The arrows show which time slots are routed through a particular trunk interface)

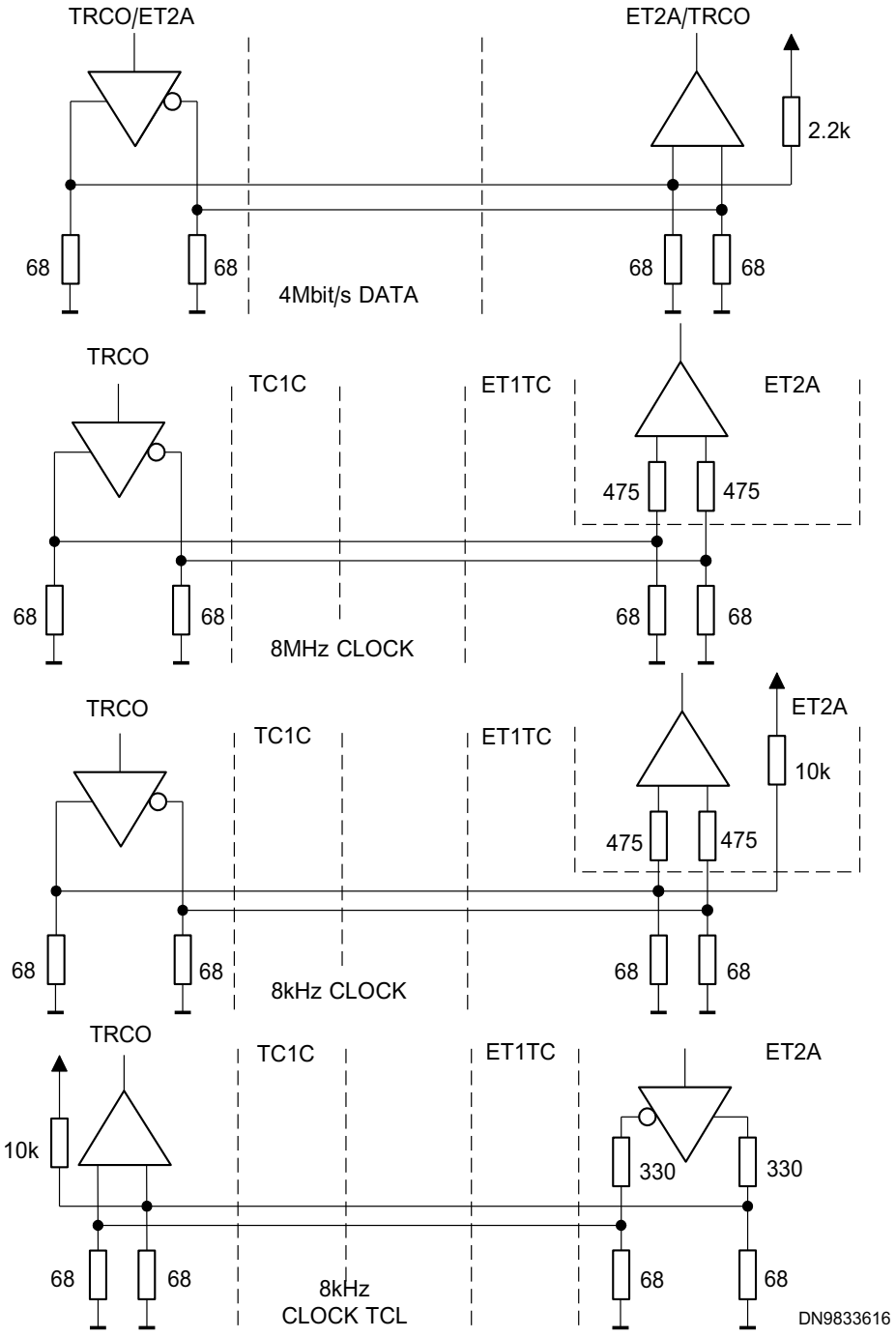

Figure 15. Principle of the electrical connection of the LI

TCSM2 mutual alarm bus

The TRCO can read alarm conditions from four wired alarm inputs of a dedicated alarm bus. The alarm types on the bus are:

- The TRCO processor is in boot state
- O&M connection (LAPD) to the BSC is not working
- The power switch is in the OFF position in the PSC1
- A fuse is blown in the PSC1 or TRCO
- One input is reserved for future use

The figure below shows the principle of this bus.

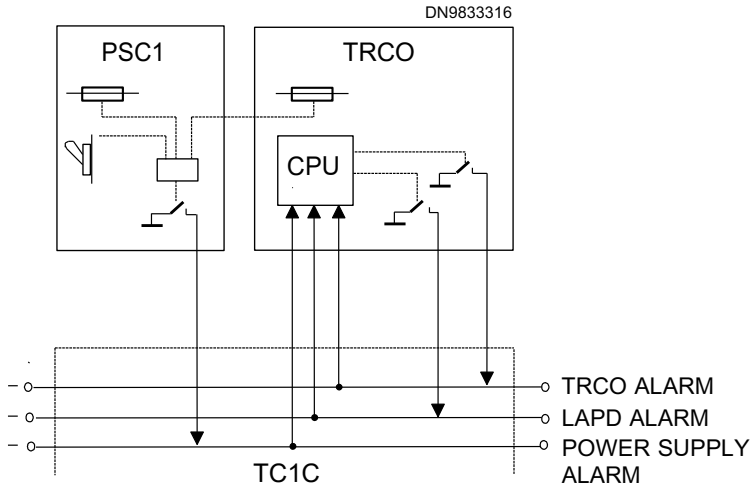

Figure 16. Principle of the mutual alarm bus

7 External interfaces

Trunk interface (ETSI)

The applicable standard for the physical characteristics is G.703 (ITU-T).

The ET2E(-S/-T) plug-in unit has two trunk interfaces. The unit is available in four variants:

- The ET2E(-S/-T) units are provided with a front panel 1/2-width Euroconnector which incorporates the two balanced 120 Ω interfaces, each on their 1/4-Euroconnector modules.
- The ET2E-C, ET2E-SC, and ET2E-TC units are provided with front panel subminiature coaxial connectors interfacing to 75 Ω lines.

DS1 port (ANSI)

The applicable standard for the physical characteristics is ANSI T1.403 Extended Super Frame (ESF) or Super Frame (SF). The LI provides a large dynamic range and overvoltage protection. It does not provide feeding current to the line. The ET2A(-T) incorporates the T1-line Channel Service Unit (CSU) function.

On the ET2A(-T) unit a 2 × 4 pin test connector is provided, where all the DS1 ports are available for a measurement instrument.

External synchronisation interfaces (ESI, ESO)

An External Synchronization Input (ESI, for a frequency of 1544 kHz/ 2048 kHz) and an External Synchronization Output (ESO, 2048 kHz) are provided on the front panel of the TRCO. The connectors are SMB (sub-miniature type-B coaxial) connectors. Since the synchronisation of the TCSM2 is extracted from the T1/E1 lines, these interfaces are meant for test purposes only.

Wired alarms interface

An interface for a number of wired alarms (four inputs) is available on the rear panel of the TC1C cartridge. The alarms are handled by the TRCO unit. An alarm condition is indicated by a low-logic voltage level.

FPGA programming interface

An RJ45 type modular jack, on the TC1C back plane, can be used as a programming interface for FPGA circuits of the TRCO and the TR12-T. The cable from the FPGA programmer device is attached to the JL1 connector, and the plug-in unit to be programmed is pushed to the slot of the last TR12-T. Programming can be done only with a cartridge with no live traffic.

8 User interface

A standard terminal (VT 52 or VT 100) is used as the MMI terminal. The terminal interface is located on the front panel of the TRCO. It is an asynchronous V.24/V.28 serial interface. The electrical characteristics conform to recommendation V.28 (ITU-T). The physical connector is a 25-pin D-connector conforming to ISO standards.

9 Loop tests

Loop test 0

In this test, provided for each TRAU individually, the TRAU is forced to start transcoding, even if the received uplink TRAU frames are not of the correct type. The loop for the time slot can be made, for example, in the ET2E(-S/-T)/ET2A(-T). This test is useful mainly for vendor-internal verification.

Loop test 1

Traffic channel loop tests are activated by a command. The coverage of the loop test can be selected to be one of the following:

- One (MSC-side) DS1/trunk signal, one time slot
- One (MSC-side) DS1/trunk signal, all the time slots
- All trunk interface signals, all the time slots

The automatic diagnostic procedure, when activated, causes all the time slots of all the lines to be tested.

In test state one, the TCSM2 unit is tested by transmitting a signal generated from a defined base set of PCM samples to the 64 kbit/s direction. The PCM samples are looped back from the ET unit and encoded with HR speech coding. The resulting HR TRAU frames are sent in the Ater direction, so that in the case of circuit type *B*, the frames are located (as usual) in the 8 kbit/s sub-channel. In the case of other circuit types, the HR frames are duplicated to the other sub-channels, so that the whole available part of the time-slot is tested. These TRAU frames are looped back from the ET unit and decoded with HR speech coding.

LAPD loop

This test is provided for each of the LAPD interfaces of the TRCO. The LAPD controller makes a loop back of the transmitted signal. A comparison is then made between the transmitted test sequence and the returned signal.

10 Test loops

The purpose of loops is to make routine testing and fault locating easier.

In the TCSM2A unit, loops can be activated either per DS1 signal or per traffic channel (see the following figure). Some of the loops are meant for miscellaneous test purposes, while others can also be used for test functions of a functioning BSS system.

ET equipment loop

The entire signal sent to the DS port/trunk interface (towards the BSC or MSC) is looped back at the ET2E(-S/-T)/ET2A(-T) line interface.

ET time slot loop – ANSI only

A selected time slot of the signal towards the BSC or MSC is looped back at the ET2A(-T).

TRAU loop 1

A selected 8, 16, 32, or 64 kbit/s channel from the BSC-side is looped back at the TRAU before decoding and encoding.

TRAU loop 2

A selected 8, 16, 32, or 64 kbit/s channel from the BSC-side is looped back at the TRAU after decoding and encoding. Transcoding starts if the received TRAU frame is valid.

TRAU loop 3

A selected time slot from the MSC-side is looped back at the TRAU after encoding. Transcoding is forced into an active state.

TRAU loop 4

A selected time slot from the MSC-side is looped back at the TRAU before encoding.

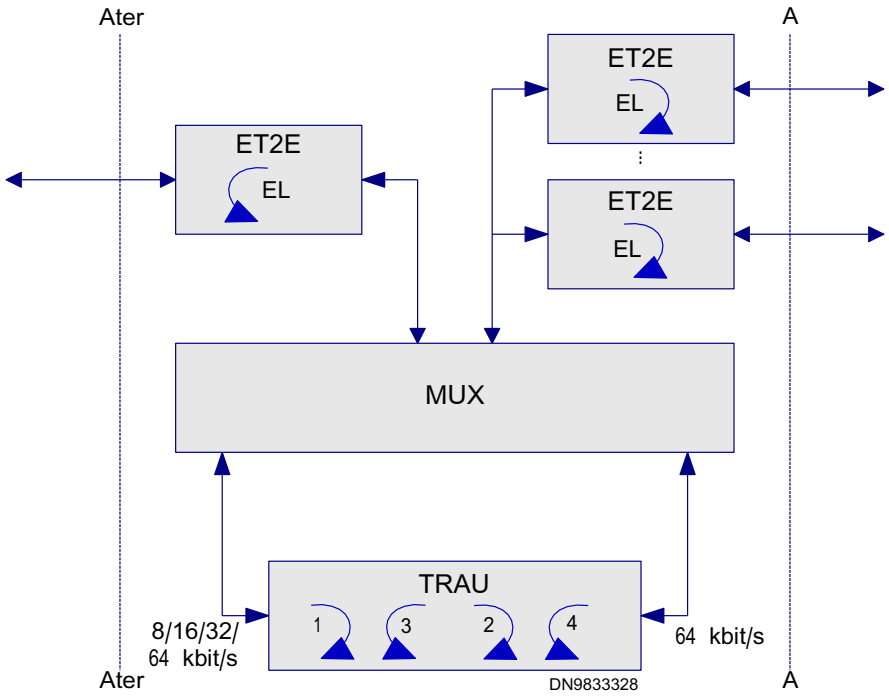

Figure 17. Test loops in the TCSM2E (EL stands for Equipment loop)

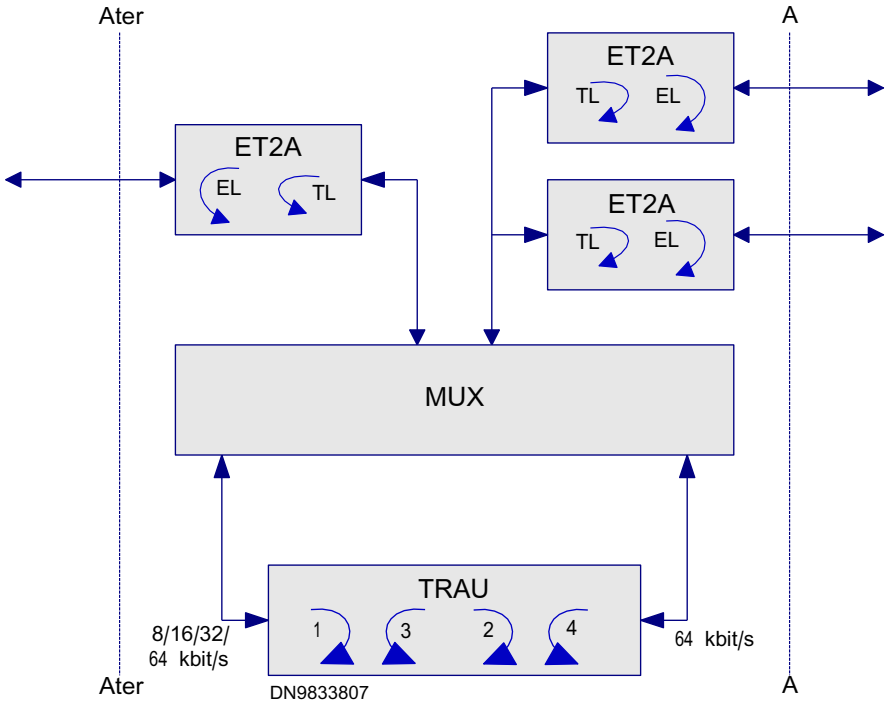

Figure 18. Test loops in the TCSM2A (EL stands for Equipment loop, TL for Time slot loop)

11 TC1C cartridge power supply

Power supply plug-in unit (PSC1)

The PSC1 is the power supply unit of the TC1C cartridge. Its power feeding capacity is +5 V / 24 A and -5 V / 7.5 A. Another power supply variant is the PSC-1, which can deliver +5 V / 40 A and -5 V / 7.5 A. Possible use of this variant is subject to future product enhancements.

Structure of the power supply

All the required voltages for the TCSM2A are generated from DC voltage by high frequency transformers using a chopper technique.

The input voltage range is -40.5 V to -72 V. Because of this wide range, the main battery voltage can be -48 V or -60 V.

The Power Supply PSC1 generates the +5 V and -5 V voltages to the units in the TC1C. The 3.3 V voltage that is used in some parts of the TR12-T is generated on-board from the +5 V voltage.

The ET2 plug-in units have an on-board DC/DC converter, which uses the rack power supply as input.

12 TC1C and ET1TC cartridge intermediate cabling

A standard rack configuration with pre-installed shelves and cartridges allows simple interconnection cabling.

The following two figures show the rear sides of cartridges TC1C and ET1TC with connector identifications.

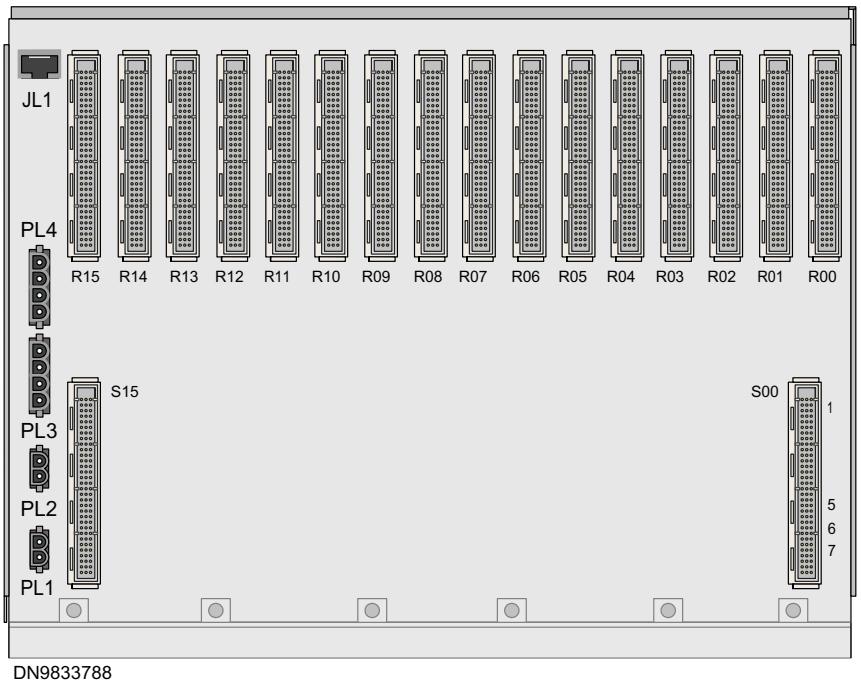

Figure 19. Rear view of the TC1C with connector locations for interconnection cabling

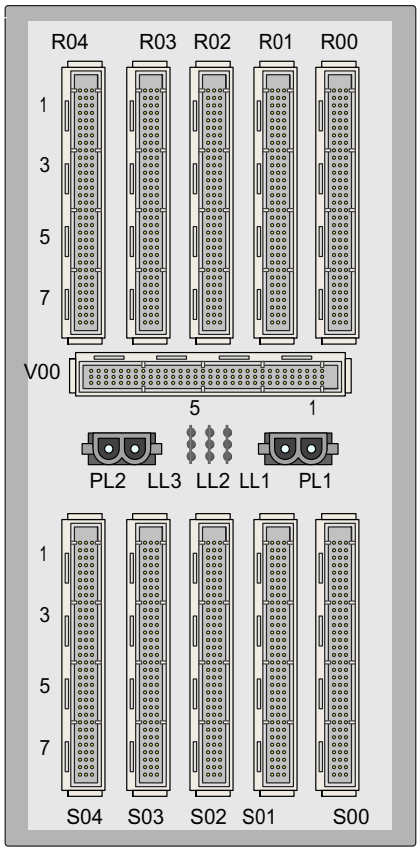

Figure 20. Rear view of the ET1TC with connector positions for interconnection cabling

Interconnection of the TC1C and the ET1TC

An interconnection cable connects the data, clock, and alarm signals between the TC1C and ET1TC cartridges. Even numbers of the TCSM2A use the upper part of the ET1TC, and odd numbers the lower part. The table below presents the connections in detail. The connectors are 1/2-Euroconnectors.

Table 4. Connections for the TC1C - ET1TC interconnection cable

TCSM2A no.	TC1C no.	TC1C connector position	ET1TC connector position
0 (and other even numbers)	0 (and other even numbers)	S00-1	V00-5
1 (and other odd numbers)	1 (and other odd numbers)	S00-1	V00-1

Alarm bus

The alarm bus between the TCSM2As consists of a chain of cables. TC1C connector S00-6 of one TC1C is connected to the TC1C connector S00-5 of the next TC1C. The first TC1C of the chain has S00-5 empty, and the last TC1C has S00-6 empty. The connector of the cable is a 1/8-Euroconnector.

Alarm inputs

A connector is reserved for future use, to connect external wired alarms (a maximum of 3) to the TRCO through the TC1C back plane. It is a 1/8-Euroconnector in position S00-7.

Power supply cables for the TC1C

The cables for the duplicated power supply are connected to TC1C connectors PL1 and PL2, from the rack fuses.

Connectors PL3 and PL4 can be used to provide a parallel feeding of +5 V and -5 V voltages to and from the other cartridges. (Their use is an option for the future).

Power supply and grounding cables for the ET1TC

The table below shows the connections of the power supply cable at the ET1TC side. The other end is connected to the rack fuse outputs. The connector at the ET1TC side is a 1/4-Euroconnector.

Table 5. Connections of the power supply to the ET1TC

Part of ET1TC supplied	Connector
Upper	PL1
Lower	PL2

The overvoltage-protection return-current of the DS1-port is led by a cable from terminal LL2 to the rack ground busbar. It is also possible to connect the cables of different ET1TCs as a daisy chain, by using terminals LL2 and LL3.

13 Power consumption of TCSM2

Power consumption of TCSM2 (ETSI)

The power consumption can be calculated for a group of channels by the formula:

$P(Watts) = N_f \times 0.38 + N_e \times 0.38 + N_h \times 0.36 + N_d \times 0.38 + A \times (Ns \times 0.02 + N_e \times 0.18 + N_h \times 0.17 + N_d \times 0.27)$,

where

N_f = number of (traditional ETSI) FR TCHs

N_e = number of EFR TCHs

N_h = number of HR TCHs

N_d = number of HSCSD (2 × 16 kbit/s or 4 × 16 kbit/s) channels

A = traffic (0 to 1 Erl/TCH)

As far as FR, EFR, and HR channels are concerned, the formula primarily applies for voice traffic. Data traffic results in consumption values which are considerably lower.

If HR is implemented with the circuit type C principle, the formula cannot be directly applied. Instead of using the Nf, Ne, and Nh values as such, the traffic portions of ERF or FR mode and HR mode must be estimated. Based on these estimates, the values of Nf, Ne, and Nh should be modified prior to making the calculation. Cartridge maximum consumptions are shown in the table below.

Table 6. Maximum consumptions

Cartridge	Consumption
TC1C Full rate only	40 W
TC1C Half rate only	105 W
TC1C Enhanced full rate only	65 W
ET1TC Full rate only	18 W
ET1TC Half rate only	25 W
ET1TC Enhanced full rate only	18 W

Power consumption (ANSI)

The power consumption of a group of channels can be calculated using the following formula:

$P(Watts) = N_f \times 0.38 + N_e \times 0.38 + N_h \times 0.36 + N_d \times 0.38 + A \times (N_f \times 0.02 + N_e \times 0.18 + N_h \times 0.17 + N_d \times 0.27)$,

where

N_f = number of (ETSI) full rate TCHs

N_e = number of EFR TCHs

N_h = number of HR TCHs

N_d = number of HSCSD (2 × 16 kbit/s or 4 × 16 kbit/s) channels

A = traffic (0 to 1 Erl/TCH)

As regards FR, EFR, and HR channels, the formula primarily applies for voice traffic. For data traffic, the power consumption values are considerably lower.

Note

If HR is implemented with the circuit type C principle, the formula cannot be directly applied. Instead of using the N, N and N values as such, the traffic portions of Enhanced Full Rate (EFR) or Full Rate (FR) mode and Half rate (HR) mode must be estimated. Based on these estimates, the values of N, N and N should be modified prior to making the calculation.

The maximum consumptions of the cartridges are shown in the following three tables.

Table 7. Maximum consumptions for a normal TCSM2A application

Cartridge	Consumption
TC1C Full rate only	30 W
TC1C Half rate only	80 W
TC1C Enhanced full rate only	50 W
ET1TC Full rate only	18 W
ET1TC Enhanced full rate only	18 W
ET1TC Half rate only	25 W

Appendix A Connector diagrams

The following pages present the figures and pin diagrams of the connectors.

TRCO

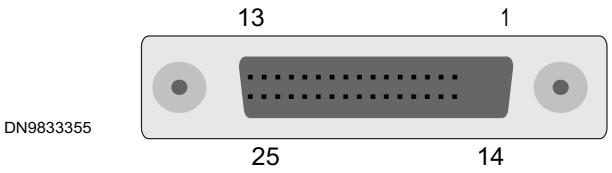

Figure 21. VDU connector, as seen from the front of the TRCO

Table 8. Signals of the VDU connector

Name	Pin	Explanation
GND	1	Frame ground
RXD	2	Receive data (to the TRCO)
TXD	3	Transmit data (from the TRCO)
D0V	7	Signal ground

Table 9. Signals of the VDU connector

Name	Pin	Explanation
GND	1	Frame ground
RXD	2	Receive data (to TRCO)
TXD	3	Transmit data (from TRCO)
D0V	7	Signal ground

ET2E

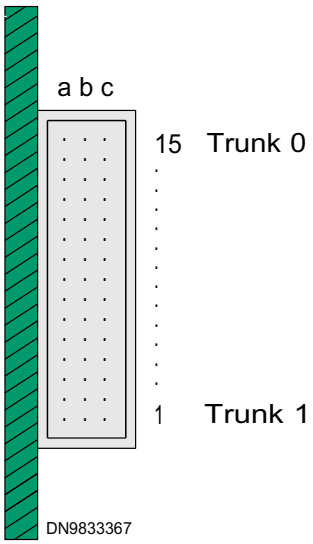

Figure 22. Balanced trunk interface connector, front view of the ET2E and ET2E-S plug-in unit

Table 10. Pin diagram of the balanced trunk interface connector on the ET2E and ET2E-S

Pin row	c	b	a
16			
15			
14	TSG0	TIS0A	TSG0
13	TSG0	TIS0B	TIS0B
12	TSG0	TIS0A	TSG0
11	SG0	RIS0A	TSG0
10	RSG0	RIS0B	RIS0B
9	RSG0	RIS0A	RSG0
8	RSG0		RSG0
7			
6	TSG1	TIS1A	TSG1
5	TSG1	TIS1B	TIS1B
4	TSG1	TIS1A	TSG1

Table 10. Pin diagram of the balanced trunk interface connector on the ET2E and ET2E-S (cont.)

Pin row	c	b	a
3	SG1	RIS1A	TSG1
2	RSG1	RIS1B	RIS1B
1	RSG1	RIS1A	RSG1

Table 11. Signals of the balanced trunk interface connector on the ET2E and ET2E-S

Name	Explanation
TISxy	Trunk interface transmit
	x (= 0 or 1) indicates number of interface
	y (= A or B) indicates polarity of wire
TSG0	Signal ground, used for grounding of transmit pair
	x (= A or B) indicates polarity of wire
RISxy	Trunk interface receive
	x (= A or B) number of interface
	y (= A or B) indicates polarity of wire
RSGx	Ground (Not used)
SGx	Signal ground, used for grounding of receive pair

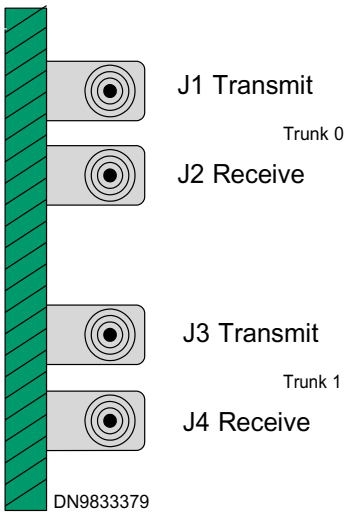

Figure 23. Coaxial trunk interface connectors, front view of the ET2E-C and ET2E-SC plug-in units

Table 12. Signals of the coaxial trunk interface connectors ET2E-C and ET2E-SC

Name	Pin	Explanation
RISxA, TISxA	Centre	Receive, Transmit
Ground	Shield	Ground

ET2A

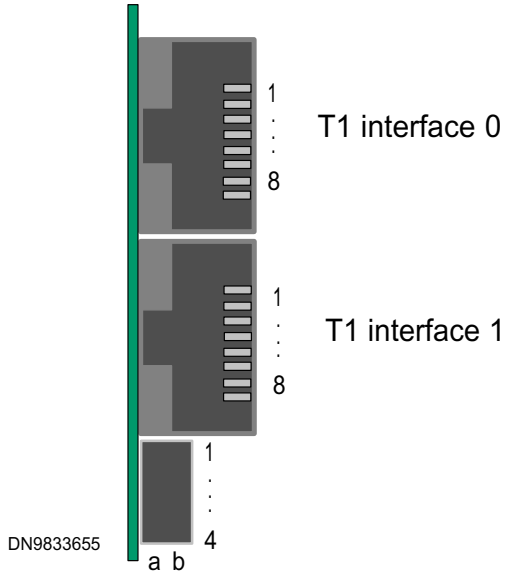

Figure 24. DS1 (T1) port connectors and test interface connector, front view of the ET2A plug-in unit

Table 13. Signals of DS1 (T1) port connectors

Name	Pin	Explanation
R1	1	DS1 port receive to ET2A, wire 1
T1	2	DS1 port receive to ET2A, wire 2
-	3	-
R	4	DS1 port transmit from ET2A, wire 1
T	5	DS1 port transmit from ET2A, wire 2
-	6	-
-	7	-
-	8	-

Table 14. Signals of the DS1 test port connector

Name	Pin	Explanation
R1-0T	1a	DS1 port receive to ET2A, wire 1 / Interface 0
R-0T	2a	DS1 port receive to ET2A, wire 2 / Interface 0
T1-0T	1b	DS1 port transmit from ET2A, wire 1 / Interface 0
T-0T	2b	DS1 port transmit from ET2A, wire 2 / Interface 0
R1-1T	3a	DS1 port receive to ET2A, wire 1 / Interface 1
R-1T	4a	DS1 port receive to ET2A, wire 2 / Interface 1
T1-1T	3b	DS1 port transmit from ET2A, wire 1 / Interface 1
T-1T	4b	DS1 port transmit from ET2A, wire 2 / Interface 1

TC1C

Table 15. Pin diagram of connectors R00 to R14 of the TC1C (signals marked with an asterisk are only included on connector R14)

Pin row	c	b	a
1	+5V	+5V	+5V
2	GND	GND	GND
3	-5V	-5V	-5V
4	GND	GND	GND
5	8M	GND	8K
6	GND	GND	GND
7	+5V_OUT	GND	GND
8			
9		_ispEN *	SDI *
10	MODE *	SDO *	SCLK *
11	SUBA0	SUBA1	SUBA2
12	SUBA3	SUBA4	SUBA5
13	SUBA6	SUBA7	
14	GND	GND	GND
15	PCM0_OUT	PCM1_OUT	PCM2_OUT
16	PCM3_OUT	PCM0_IN	PCM1_IN
17	PCM2_IN	PCM3_IN	GND

Table 15. Pin diagram of connectors R00 to R14 of the TC1C (signals marked with an asterisk are only included on connector R14) (cont.)

Pin row	c	b	a
18			
19	_broca	_ready	_int
20	_inta	_rd	_wr
21	GND	GND	GND
22	add0	add1	add2
23	add3	add4	add5
24	add6	add7	add8
25	add9	add10	
26	GND	GND	GND
27	d0	d1	d2
28	d3	d4	d5
29	d6	d7	GND
30	GND	GND	GND
31			
32	GND	GND	GND

Table 16. Signals of connectors R00 to R14 of the TC1C

Name	Explanation
8M	8192 kHz clock (8M) for TRI and SUBA
8K	8 kHz clock (8K) for TRI and SUBA
+5V	+5 V voltage
-5V	-5 V voltage
GND	Ground for low voltage circuitry
+5V_OUT	+5 V voltage output
SUBA0	Data signals of SUBA
SUBA7	
_ispEN	FPGA programming interface (Only connector R14)
SDI	FPGA programming interface (Only connector R14)
SDO	FPGA programming interface (Only connector R14)
MODE	FPGA programming interface (Only connector R14)

Table 16. Signals of connectors R00 to R14 of the TC1C (cont.)

Name	Explanation
SCLK	FPGA programming interface (Only connector R14)
PCM_0_OUT	4096 kbit/s data signals of TRI (4M), direction TRCO -> TR
PCM_3_OUT	
PCM_0_IN	4096 kbit/s data signals of TRI (4M), direction TR -> TRCO
PCM_3_IN	
_broca	Control signal of TRCI
_ready	Control signal of TRCI
_int	Control signal of TRCI
_inta	Control signal of TRCI
_wr	Control signal of TRCI
_rd	Control signal of TRCI
_add0	Address signals of TRCI
_add10	
d0 to d7	Data signals of TRCI

Table 17. Pin diagram of connector S00 of the TC1C (the signals in brackets appear at duplicated pins on the motherboard)

Pin row	c	b	a
1	D0V	D0V	D0V
2	LIDR_3B	LIDR_3A	LIDT_3A
3	TCL_7B	TCL_7A	LIDT_3B
4	TCL_6B	TCL_6A	D0V
5	8K0_B	8K0_A	_TAL
6	LIDR_2B	LIDR_2A	LIDT_2A
7	TCL_5B	TCL_5A	LIDT_2B
8	TCL_4B	TCL_4A	D0V
9	D0V	D0V	D0V
10	LIDR_1B	LIDR_1A	LIDT_1A
11	TCL_3B	TCL_3A	LIDT_1B
12	TCL_2B	TCL_2A	D0V
13	TCL_1B	TCL_1A	ALTST

Table 17. Pin diagram of connector S00 of the TC1C (the signals in brackets appear at duplicated pins on the motherboard) (cont.)

Pin row	c	b	a
14	LIDR_0B	LIDR_0A	LIDT_0A
15	8M0_B	8M0_A	LIDT_0B
16	TCL_0B	TCL_0A	D0V
17	_ALO_0	_ALO_2	_ALO_1
18	(_ALI_0)	(_ALI_3)	
19	(_ALI_1)		
20	(_ALI_2)		D0V
21	D0V	D0V	D0V
22	_ALI_0	_ALI_3	
23	_ALI_1		
24	_ALI_2		D0V
25	D0V	D0V	D0V
26	_ALI_4	_ALI_7	
27	_ALI_5		
28	_ALI_6		D0V
29	D0V	D0V	D0V
30			
31	+5V	+5V	+5V
32	D0V	D0V	D0V

Table 18. Signals of connector S00 on the TC1C

Name	Explanation
LIDT_0x	4096 kbit/s data of LI interface from TRCO to ET2A x (= A or B) indicates polarity of wire
LIDT_7x	
LIDR_0x	4096 kbit/s data of LI interface from ET2A to TRCO x (= A or B) indicates polarity of wire
LIDR_7x	
TCL_0x	8 kHz clock from ET2A to TRCO x (= A or B) indicates polarity of wire

Table 18. Signals of connector S00 on the TC1C (cont.)

Name	Explanation
TCL_7x	
8K0_x	8 kHz clock from TRCO timing block to ET2A x (= A or B) indicates polarity of wire
8M0_x	8192 kHz clock from TRCO timing block to ET2A x (= A or B) indicates polarity of wire
_TAL_0	Alarm from ET2A/upper row
_TAL_1	Alarm from ET2A/lower row
ALTST_0	Alarm test activation to ET2A/upper row
ALTST_1	Alarm test activation to ET2A/lower row
_ALO_0 ...	Programmable alarm output from TRCO
_ALO_2	
_ALI_0	Programmable alarm input to TRCO, for mutual alarm bus signals
_ALI_3	
_ALI_4	Programmable alarm input to TRCO
_ALI_7	
+5V	+5 V voltage
D0V	Ground for low voltage circuitry

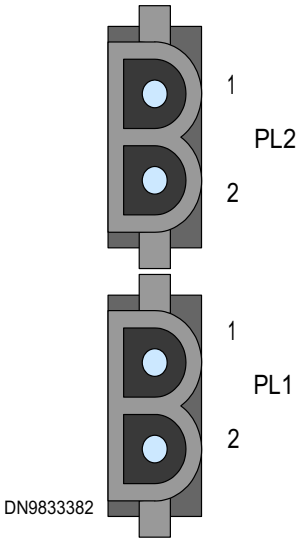

Figure 25. Pins of connectors PL1 and PL2, as seen from the rear of the TC1C

Table 19. Signals of PL1 and PL2 connectors of the TC1C

Name	Pin	Explanation
-UB	1	Negative feeding voltage
B0V	2	Positive lead of feeding voltage

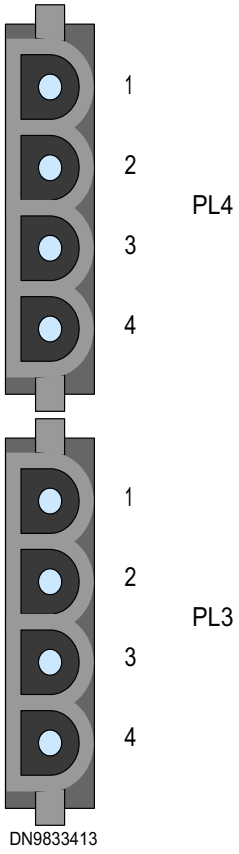

Figure 26. Pins of connectors PL3 and PL4, as seen from the rear of the TC1C

Table 20. Signals of PL3 and PL4 connectors of the TC1C

Name	Pin	Explanation
+5V	1	+5 V voltage
+5V	2	+5 V voltage
+5V	3	+5 V voltage
-5V	4	-5 V voltage

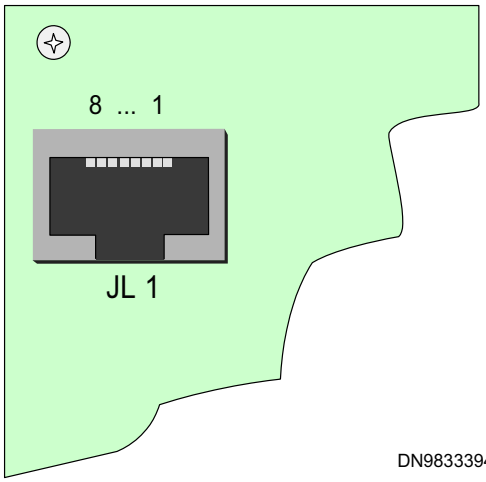

Figure 27. JL1 connector for FPGA programming, rear view of the TC1C

Table 21. Signals of connector JL1 on the TC1C

Name	Pin	Explanation
SCLK	1	Serial clock
GRND	2	Ground
MODE	3	Programming control
-	4	-
_ispEN	5	Programming control
SDI	6	Serial data input
SDO	7	Serial data output
Supply	8	+5 V supply from the TC1C

ET1TC

Table 22. Pin diagram of connectors R00 to R03 and S00 to S03 on the ET1TC

Pin row	c	b	a
1	-UB	-UB	-UB
2			

Table 22. Pin diagram of connectors R00 to R03 and S00 to S03 on the ET1TC (cont.)

Pin row	c	b	a
3			
4			D0V
5	B0V	B0V	B0V
6			
7			
8			D0V
9	CMD	NTIM	0VG
10			
11			
12		_TAL	D0V
13		ALTST	
14			
15			
16			D0V
17	+5VA	CSB	CSA
18			TCL0A
19			TCL0B
20			D0V
21			
22			TCL1A
23			TCL1B
24			D0V
25	-5VA	8M0B	8M0A
26	RCTP0		
27	TCTP	8KB	8KA
28	D0V		
29		T0B	T0A
30	RCTP1	T1B	T1A
31		R0B	R0A
32	D0V	R1B	R1A

Table 23. Signals of connectors R00 to R03 and S00 to S03 of the ET1TC

Name	Explanation
T0x	4096 kbit/s data (LI) from ET2A / Interface 0
	x (= A or B) indicates polarity of wire
T1x	4096 kbit/s data (LI) from ET2A / Interface 1
	x (= A or B) indicates polarity of wire
R0x	4096 kbit/s data (LI) to ET2A / Interface 0
	x (= A or B) indicates polarity of wire
R1x	4096 kbit/s data (LI) to ET2A / Interface 1
	x (= A or B) indicates polarity of wire
8Mx	8192 kHz clock signal to ET2A
	x (= A or B) indicates polarity of wire
8Kx	8 kHz clock signal to ET2A
	x (= A or B) indicates polarity of wire
TCL0x	8 kHz clock signal from ET2A / Interface 0
	x (= A or B) indicates polarity of wire
TCL1x	8 kHz clock signal from ET2A / Interface 1
	x (= A or B) indicates polarity of wire
CMD	Control bit for command connection (Not used)
NTIM	Nominal timing (Not used)
_TAL	Alarm from ET2A
ALTST	Alarm test activation to ET2A
CSA	Control of changeover (Not used)
CSB	Control of changeover (Not used)
TCTP	Measurement point for transmit clock (2048 kHz)
RCTP0	Measurement point for receive clock (2048 kHz) / Interface 0
RCTP1	Measurement point for receive clock (2048 kHz) / Interface 1
+5VA	+5 V voltage
-5VA	-5 V voltage
D0V	Ground of low voltage digital circuitry
V0G	Ground for overvoltage protection
B0V	Ground of power supply input
-UB	Negative power supply input

Table 24. Pin diagram of connector V00 of the ET1TC

Pin row	c	b	a
1			
2	LIDT_7B	LIDT_7A	LIDR_7A
3	TCL_15B	TCL_15A	LIDR_7B
4	TCL_14B	TCL_14A	D0V
5	8K0_B	8K0_A	_TAL_1
6	LIDT_6B	LIDT_6A	LIDR_6A
7	TCL_13B	TCL_13A	LIDR_6B
8	TCL_12B	TCL_12A	D0V
9			
10	LIDT_5B	LIDT_5A	LIDR_5A
11	TCL_11B	TCL_11A	LIDR_5B
12	TCL_10B	TCL_10A	D0V
13	TCL_9B	TCL_9A	ALTST_1
14	LIDT_4B	LIDT_4A	LIDR_4A
15	8M0_B	8M0_A	LIDR_4B
16	TCL_8B	TCL_8A	D0V
17			
18	LIDT_3B	LIDT_3A	LIDR_3A
19	TCL_7B	TCL_7A	LIDR_3B
20	TCL_6B	TCL_6A	D0V
21	8K0_B	8K0_A	_TAL_0
22	LIDT_2B	LIDT_2A	LIDR_2A
23	TCL_5B	TCL_5A	LIDR_2B
24	TCL_4B	TCL_4A	D0V
25			
26	LIDT_1B	LIDT_1A	LIDR_1A
27	TCL_3B	TCL_3A	LIDR_1B
28	TCL_2B	TCL_2A	D0V
29	TCL_1B	TCL_1A	ALTST_0
30	LIDT_0B	LIDT_0A	LIDR_0A
31	8M0_B	8M0_A	LIDR_0B
32	TCL_0B	TCL_0A	D0V

Table 25. Signals of connector V00 on the ET1TC

Name	Explanation
LIDT_0x	4096 kbit/s data (LI) from ET2A/upper row to TRCO
LIDT_3x	x (= A or B) indicates polarity of wire
LIDT_4x	4096 kbit/s data (LI) from ET2A/lower row to TRCO
LIDT_7x	x (= A or B) indicates polarity of wire
LIDR_0x	4096 kbit/s data (LI) from TRCO to ET2A/upper row
LIDR_3x	x (= A or B) indicates polarity of wire
LIDR_4x	4096 kbit/s data (LI) from TRCO to ET2A/lower row
LIDR_7x	x (= A or B) indicates polarity of wire
TCL_0x	8 kHz clock from ET2A/upper row to TRCO
TCL_7x	x (= A or B) indicates polarity of wire
TCL_8x	8 kHz clock from ET2A/lower row to TRCO
TCL_15x	x (= A or B) indicates polarity of wire
8K0_x	8 kHz clock from TRCO timing block to ET2A
	x (= A or B) indicates polarity of wire
8M0_x	8192 kHz clock from TRCO timing block to ET2A
	x (= A or B) indicates polarity of wire
_TAL_0	Alarm from ET2A/upper row
_TAL_1	Alarm from ET2A/lower row
ALTST_0	Alarm test activation to ET2A/upper row
ALTST_1	Alarm test activation to ET2A/lower row
D0V	Ground for low voltage circuitry

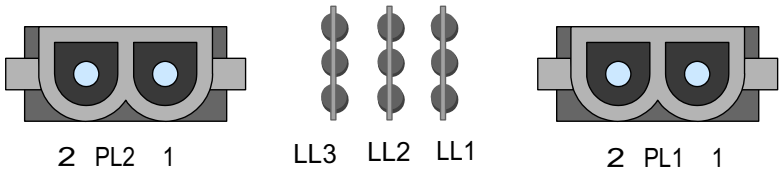

Figure 28. Pins of connectors PL1, PL2, LL1, LL2, and LL3, as seen from the rear of the ET1TC

Table 26. Signals of PL1, PL2, LL1, LL2, and LL3 connectors of the ET1TC

Name	Pin	Explanation
PL1 / -UB	1	Negative feeding voltage
PL1 / B0V	2	Positive lead of feeding voltage
PL2 / -UB	1	Negative feeding voltage
PL2 / B0V	2	Positive lead of feeding voltage
LL1 / D0V	-	Ground of low-voltage digital circuitry
LL2 / 0VG	-	Ground for overvoltage protection
LL3 / 0VG	-	Ground for overvoltage protection

Table 27. Connector and pin arrangement for the power supply alarm concentration on the ET1TC

Signal function	Input conn. pos.	Pin no. (in 1/1-Euroconn.	Output conn. pos.	Pin no. (in 1/1-Euroconn.)
Alarm	R04-1	7b, 7c, 8b, 8c	S04-7	26c
Alarm	R04-2	15b, 15c, 16b, 16c	S04-7	26b
Alarm	R04-3	23b, 23c, 24b, 24c	S04-7	26a
Alarm	R04-4	31b, 31c, 32b, 32c	S04-7	27c
Alarm	S04-1	7b, 7c, 8b, 8c	S04-7	27b
Alarm	S04-2	15b, 15c, 16b, 16c	S04-7	27a
Alarm	S04-3	23b, 23c, 24b, 24c	S04-7	28c
Alarm test	R04-x	7a, 15a, 23a, 31a	S04-7	28b
	S04-x	7a, 15a, 23a	S04-7	28b
Ground	0 V from cartridge	-	S04-7	32a