TECHNICAL BULLETIN
Differences Between the GT-64240-B-0 and the GT-64240A

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The following table summarizes the differences between the GT-64240-B-0 and the GT-64240A.

Table 1: Differences of Existing Features Between the GT-64240-B-0 and the GT-64240A

Feature/Errata	GT-64240-B-0	GT-64240A
Features Changes		
Revision ID	The Revision ID in the PCI Configuration register for the GT-64240-B-0 is 0x1.	The Revision ID in the PCI Configuration register for the GT-64240A is 0x10.
Clock Frequency	The GT-64240-B-0 maximum TClk frequency is 100MHz.	The GT-64240A maximum TClk frequency is 133MHz.
Baude Rate Generators	The GT-64240-B-0 contains three baude rate generators.	The GT-64240A only contains two baude rate generators. BRG2 was removed.
PCI Arbiter	The GT-64240-B-0 PCI arbiter is a weighted round robin arbiter.	The GT-64240A implements a fixed round robin arbiter (priorities are no longer supported).
Access To I2O Registers	The GT-64240-B-0 I2O registers can be mapped for PCI accesses in the first 4Kbyte of SCS[0] BAR space or as part of the GT-64240-B-0 Internal Registers space. It depends on the setting of the PCI Address Decode Control register's MsgAcc bit.	The GT-64240A I2O registers can only be mapped for PCI accesses in the first 4Kbyte of SCS[0] BAR space.
Reset Strapping	The GT-64240-B-0 has some reset strapping over the 32-bit device bus (AD[31:0]).	The GT-64240A AD[27:19] reset strapping has been changed, as follows: • AD[23:19]: Must pull down. • AD[24]: Internal space address window default value. 0 - GT-64240-B-0 compatible (0x1400.0000) 1 - New value (0xF100.0000) • AD[27:25]: Must pull low. All PCI features that were configured via AD[27:19] reset strapping (VPD, MSI, BIST, CPCI Hot Swap, PMG) are now enabled.

Table 2: New Features in the GT-64240A That do not Exist in the GT-64240-B-0

Feature/Errata	GT-64240-B-0	GT-64240A
PMC R7000C Simple Cache	The GT-64240-B-0 does not support PMC R7000C Simple Cache mode.	The GT-64240A supports PMC R7000C Simple Cache mode. This mode eliminates the need for Tag RAMs and L3 cache is built of standard Sync Burst SRAMs. **NOTE:** The GT-64240A Simple Cache mode support is limited to early write L3 SRAM type.
Simple UART	The GT-64240-B-0 MPSC requires the CPU to handle descriptors chain(s) in memory.	When configured to UART, the GT-64240A MPSC can work on a register read/write basis, without handling descriptor chain(s) in memory.
ISL	The GT-64240-B-0 only supports ISL on the Ethernet ports in MII mode.	The GT-64240A supports ISL on the Ethernet ports in MII and RMII modes
Sync Burst SRAM	When interfacing a Sync Burst SRAM on the GT-64240-B-0 device bus, data can be read every third cycle.	The GT-64240A device controller supports a new timing parameter - AddrSkew. This new parameter enables toggling of the burst address two cycles prior to the read data sample window. This results in the ability to read bursts from a Sync Burst SRAM with no wait states between the burst data beats.
GPP Interrupts	The GT-64240-B-0 MPPs, when configured as GPP input pins, can be used to collect external interrupts. However, in this configuration, they act as edge trigger interrupts. If after the interrupt handler cleared the interrupt bit in the GPP Interrupt Cause register, the external interrupt generator still keeps the GPP input asserted, this interrupt is not registered.	The GT-64240A also supports level sensitive GPP interrupts. If the new GPP_mode bit in the Comm Unit Arbiter Control register is set to ‘1’, the GPP inputs act as level interrupts. The interrupt is an OR of all non masked GPP inputs. In this mode, the GPP Interrupt Cause register is not used and the interrupt handler clears the interrupt directly in the external interrupt generator.
Internal Space Address Window Default Value	The GT-64240-B-0 Internal space address window default value is 0x1400.0000	The GT-64240A supports an alternative default value of 0xF100.0000. The default value is determined via AD[24] strapping option.

Table 3: Erratas in the GT-64240-B-0 Corrected in the GT-64240A

Feature/Errata	GT-64240-B-0	GT-64240A
FErr#1, FErr#2, FErr#3, FErr#4, FErr#5, FErr#6, FErr#7, FErr#8, FErr#9, FErr#10, FErr#11, FErr#12, FErr#13, FErr#16, FErr#17, FErr#18, FErr#19, FErr#20, FErr#22, FErr#23, FErr#24, FErr#25, FErr#26, FErr#27, FErr#28, FErr#29, FErr#30, FErr#31, FErr#32, FErr#34, FErr#35, FErr#36, FErr#37, FErr#38, FErr#40, FErr#41, FErr#42, FErr#44, FErr#45, FErr#46, FErr#48, FErr#50, FErr#51, FErr#52	See GT-64240-B-0 Errata document for full details.	All of these erratas are fixed in the GT-64240A.
FErr#39	The GT-64240-B-0 always accesses a 32-bit wide device with an even number of word accesses, starting at a 64-bit aligned address. External logic can identify redundant write accesses via the Wr*[3:0] signal. There is no way to identify the redundant read accesses.	The errata still exists in the GT-64240A. However, bit[2] of the transaction address is now driven on AD[2] during the address phase of the device access. This can be used by external logic, to identify the redundant read accesses.
R#3, R#6, R#9, R#10	See GT-64240-B-0 Restriction document for full details.	These restrictions no longer exist in the GT-64240A.