IBM PowerPC® 750FX RISC Microprocessor

Application Note

Differences Between the IBM PowerPC® 750FX, PowerPC 750™, and the PowerPC 750CX™/ PowerPC 750CXe™ RISC Microprocessors

Version: 1.0

Preliminary

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The information in this document is based on PowerPC 750™ Microprocessor Implementation Definition Book IV. Updates and improvements specific to the 750FX processor supersedes information from the previous specifications. Where information has not been updated specific to the 750FX processor, the older information is presumed to be correct.

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1. Abstract

This application note describes the programming model, performance, package, and power differences between the PowerPC 750FX™, the PowerPC 750™, and the PowerPC 750CXe™ processors.

Implementation Note: This note pertains to DD2.x revisions. Earlier revisions may deviate from descriptions in this application note. Please contact your sales support for information pertaining to earlier revisions.

2. Overview

The PowerPC 750FX is a 32-bit implementation of the PowerPC Architecture™ in a 0.13 micron CSOI technology with 6 levels of copper interconnect plus one level of local interconnect. 750FX is designed for high performance while minimizing power consumption. The PowerPC 750FX processor is derived from the 750 and 750CXe designs. It is a technology remap of the 750CXe and includes a complete 60x bus interface.The 750FX increases the size of the internal L2 cache to 512 KB. It also provides a miss-under-miss L1 data cache[1] and dual PLLs to allow dynamic adjustments of clock frequency for reduced power consumption. In addition to these major differences, the 750FX varies from the 750CXe and the 750 in a number of other ways, which are defined in the following sections.

- 3.0. Programming Model
- 4.0. Performance
- 5.0. Power, Voltage, Frequency
- 6.0 Timings
- 7.0. Package
- 8.0. Start-up Functions
- 9.0. Summary of 750FX Version Differences

3. Programming Model

3.1 Processor Version Register (PVR)

The 750FX processor version number (PVR) is 0x7000. This differs from the processor version number for both the 750 and the 750CXe, which is 0x0008.

Table 3-1. Design Revision Levels and Processor Version Registers (PVR)

Design Revision Level	PVR
DD2.0	0x700002r0
DD2.1	0x700002r1
Note: r = reserved bit	

1. Not supported on revision DD1.X of the 750FX.

3.2 Additional Block Address Translation (BAT) registers

The 750FX processor has increased the BAT registers to a quantity of 8 pairs for both the D-BAT and I-BAT. This differs from the number of BATs for both the 750 and the 750CXe, which have 4 pairs of D-BAT and I-BATs. *Table 3.2.1 750FX New BAT Registers Assignment* on page 10 has the special purpose register definitions (SPRs) for the added BATs. SPR assignments for the lower I and D BATs remained identical to the other 750 family designs.

3.2.1 750FX New BAT Registers Assignment

Table 3-2. New BAT Registers Assignment

SPR Decimal	r/w	Privileged	Register Name	Function
560	r/w	Yes	IBAT4U	BAT
561	r/w	Yes	IBAT4L	BAT
562	r/w	Yes	IBAT5U	BAT
563	r/w	Yes	IBAT5L	BAT
564	r/w	Yes	IBAT6U	BAT
565	r/w	Yes	IBAT6L	BAT
566	r/w	Yes	IBAT7U	BAT
567	r/w	Yes	IBAT7L	BAT
568	r/w	Yes	DBAT4U	BAT
569	r/w	Yes	DBAT4L	BAT
570	r/w	Yes	DBAT5U	BAT
571	r/w	Yes	DBAT5L	BAT
572	r/w	Yes	DBAT6U	BAT
573	r/w	Yes	DBAT6L	BAT
574	r/w	Yes	DBAT7U	BAT
575	r/w	Yes	DBAT7L	BAT

3.3 Configuration

The 750 has an on-chip L2 cache controller with a tag array that can support external L2 cache sizes of 256KB, 512KB, or 1MB, while the 750CXe has integrated a 256KB L2 cache array onto the chip. The 750FX also has an internal L2 cache array, but has **doubled that capacity to 512KB.**

The 750 off-chip cache is accessed over an external bus that is generally run at up to 1/2 the speed of the processor. The 750CXe and the 750FX internal caches run at the same speed as the processor core; this results in system performance for the 750CXe and the 750FX that is comparable to a 750 configuration with a larger external cache.

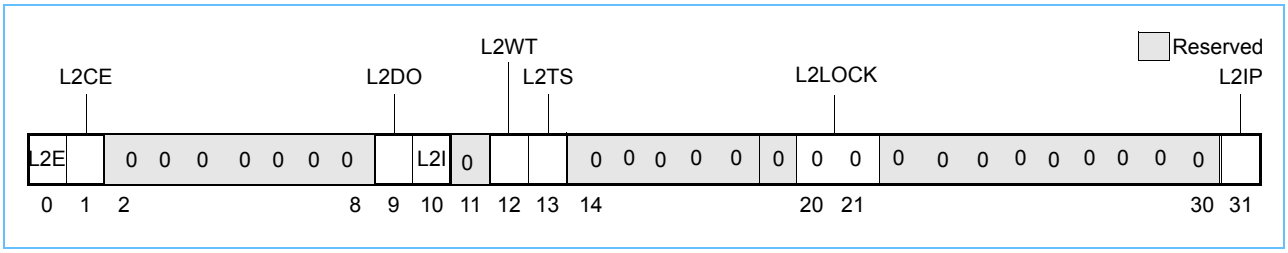
The 750CXe internal L2 cache uses ECC for error detection and correction. Like the 750CXe, the 750FX L2 cache has an 8-bit ECC for every 64-bit double-word in memory. The 750FX also supports L1 tag parity on the tag address and status bits[1].The parity feature is enabled in the HID2 register by setting bit 31.

Unlike the 750CXe, which transfers data from the L2 to the L1 cache in four double-word (64-bit) transfers, the 750FX transfers an entire four double-word (256-bit) cache line in a single cycle. The 750FX L2 cache is two-way set associative, each way containing 4096 blocks, each block consisting of two 32-byte sectors.

L2 Cache Locking[1]: The L2 cache can be configured to be unlocked, have one-half of the array locked or have the entire array locked. When configured to be unlocked, the L2 cache is 2-way set associative, with 32 bytes per sector, two sectors per block. With one way locked, the locked side is a 256 KB, direct-mapped on-chip memory (OCM) that is explicitly managed by software, while the unlocked side is a 256 KB direct-mapped cache managed by hardware. With both ways locked, the L2 cache is a 512 KB OCM, that is explicitly managed by software. The locked cache is considered to be local memory, and so is not kept coherent with main memory.

As the 750CXe and the 750FX processors no longer have an external L2 cache, some of the bits in the L2 Cache Register (L2CR) present on the 750 are unused on the 750CXe and the 750FX. The bit definitions for the L2CR for the 750FX are shown in *Figure 3-1*.

Figure 3-1. L2CR for the 750FX



3.4 Dual PLL Support

In the 750CXe and earlier processors, the hardware implementation-dependent 1 (HID1) register is used to provide software access to read the state of the PLL_CFG[0:3] signals. In the 750FX, the HID1 functionality has been enhanced to control the dual PLLs and address all five PLL_CFG signals ([0:4]) described in a later section. The 750FX HID1 bits are described in *Table 3-3*.

Table 3-3. HID1 Bit Functions for the 750FX

Bit(s)	Name	Description
0-4	PCE	PLL external configuration bits (read-only)
5-6	PRE	PLL external range bits (read-only)
7-13	—	Reserved
14	PI0	PLL 0 internal configuration select 0 Select external configuration and range bits to control PLL 0 1 Select internal fields in HID1 to control PLL0
15	PS	PLL select 0 Select PLL 0 as source for processor clock 1 Select PLL 1 as source for processor clock
16-20	PC0	PLL 0 configuration bits
21-22	PR0	PLL 0 range select bits

1. Not supported on revision DD1.X of the 750FX.

Table 3-3. HID1 Bit Functions for the 750FX (cont.)

Bit(s)	Name	Description
23	—	Reserved
24-28	PC1	PLL 1 configuration bits
29-30	PR1	PLL 1 range bits
31	—	Reserved

3.5 The 750FX Cache Parity

The 750FX has also implemented a HID2 register in DD2.X, which provides control and status of special cache related parity functions.

Table 3-4. HID2 Bit Functions for the 750FX

Bit(s)	Name	Description
0-24	—	Reserved
25	ips	icache parity status bit (read only)
26	dps	dcache parity status bit (read only)
27	l2ps	L2 tag parity status bit (read only
28	icm	icache parity error mck disable
29	ipe	icache parity enable
30	dpe	dcache parity enable
31	l2pe	L2 tag parity enable

A summary of the programming model differences between the 750, 750CXe and 750FX is provide in *Table 3-5 Summary of Programming Model Differences* on page 12.

Table 3-5. Summary of Programming Model Differences

	750	750CXe	750FX
PVR value	0x0008XXXX	0x00082204 (DD 2.4) 0x00082301 (DD 3.1)	0x7000010X (DD 1.X) 0x7000020X (DD 2.X)
BAT Registers	4 pairs (I-BAT/D-BAT)	4 pairs (I-BAT/D-BAT)	8 pairs (I-BAT/D-BAT)
PLL Config. Bits	4 [0:3]	4 [0:3]	5 [0:4] PLL_CFG and 2 [0:1] PLL_RNG (range bits)
HID1 function	Read-only access to PLL_CFG[0:3]	read-only access to PLL_CFG[0:3]	Read-only access to PLL_CFG[0:4], PLL_RNG[0:1] and software control of PLLs
HID 2 function	N/A	N/A	Parity enable and status
L2CR	Supports external L2	Internal L2 ONLY	Internal L2 ONLY, cache locking

Notes:

1. Not supported on revision DD1.X of the 750FX.
2. See the *IBM PowerPC 750FX RISC Microprocessor Datasheet* for latest revision and PVRs.

4. Performance

4.1 Improvements to the 750FX over the 750CXe and 750

In addition to having a larger internal L2 cache, there are several other enhancements to the design that improve the performance of the 750FX over the 750CXe and 750.

- Miss-under-miss L1 data cache[1.]
- L1 cache and tag parity, L2 tag parity[1]
- Wider L1 data cache reload bus (256-bit); same as 750CXe.
- Wider L2 reload path (256-bit)
- L2 support for 2 outstanding misses (1 data and 1 instruction; or 2 data[1])
- Additional FPU reservation station; same as 750CXe.
- Higher precision results from the reciprocal estimate instructions; same as 750CXe.
- Enhanced 60X Bus: pipelines back-to-back reads to a depth of 2.

The 750 and 750CXe L1 data cache supports hit-under-miss access, meaning that with one miss outstanding, the cache can continue to be accessed for accesses that hit. Once a second miss occurs, the corresponding instruction stalls, waiting for the first miss to be serviced. The 750FX L1 data cache has been enhanced to allow a second miss to initiate a transaction in the bus interface unit while the first miss is pending[1].

The data bus width for bus interface unit (BIU) accesses of the L1 data cache array is 64 bits on the 750. To cast out or to reload a 256-bit cache line requires four access cycles. On the 750FX and 750CXe, this bus has been expanded to 256 bits. As a result, cache line data bursts can be read from or written to the cache array in a single cycle, reducing cache contention between the BIU and the load-store unit.

The floating-point execution unit in the 750 has a single reservation station, which caused it to stall whenever the three stages of the FPU execution pipeline are full. A second reservation station has been added to the 750FX and 750CXe FPU which eliminates this stall, resulting in higher throughput for optimized floating-point intensive applications.

On the 750, the floating reciprocal estimate single (fres) instruction provides an estimate of the reciprocal of its input value to a precision of 8 bits and the floating reciprocal square root estimate (frsqrte) instruction provides an estimate of the square root of its input value to a precision of 5 bits. Both of these computations are improved on the 750FX and 750CXe to yield results which contain 12 bits of precision. This reduces, or eliminates the need for iterative refinement of these values in applications which use these functions.

1. Not supported on revision DD1.X of the 750FX.

The 60x bus has decoupled address and data busses, allowing transactions to be pipelined on the bus. That is, the address operation for a second transaction can be initiated before the data operation for a previous transaction is complete. The 750 or 750CXe does not pipeline back-to-back read transactions on the bus. The 750FX BIU has been enhanced to pipeline read transactions to a depth of two.

Table 4-1. Performance Comparison - 750 to 750CXe

	750	750CXe	750FX
L1 cache miss behavior	hit-under-miss	hit-under-miss	miss-under-miss[1]
L1 data bus width	64 bits	256 bits	256 bits
L2 cache size	NA	256 KB	512 KB
L2 reload path	64 bits	64 bits	256 bits
FPU reservation stations	1	2	2
fres precision	8 bits	12 bits	12 bits
frsqrte precision	5 bits	12 bits	12 bits
60X BIU consecutive reads	not pipelined	not pipelined	2 deep pipelined

Note:
[1]Not supported on revision DD1.x of the 750FX.

5. New functions

5.1 750FX Dual PLLs

The 750FX design includes two PLLs, allowing the processor clock frequency to be dynamically changed to match processing requirements. Control of the PLLs is through the HID1 register, which contains fields that specify the frequency range of each PLL, the clock multiplier for each PLL, external or internal control of PLL0, and a bit to choose which PLL is selected, that is, which is the source of the processor clock at any given time.

At power-on reset, the HID1 register contains zeroes for all the non-read-only bits (bits 7 to 31). This configuration corresponds to the selection of PLL0 as the source of the processor clocks, and selects the external configuration and range pins to control PLL0. The external configuration and range pin values are accessible to software via HID1 read-only bits 0-6. PLL1 is always controlled by its internal configuration and range bits. The HID1 setting associated with hard reset corresponds to a PLL1 configuration of clock off, and selection of the medium frequency range.

As stated in the hardware specification, $\overline{\text{HRESET}}$ must be asserted during power up long enough for the PLL(s) to lock, and for the internal hardware to be reset. Once this timing is satisfied, $\overline{\text{HRESET}}$ can be negated. The processor now will proceed to execute instructions, clocked by PLL0 as configured via the external pins. The processor clock frequency can be modified from this initial setting in one of two ways. First, as with earlier designs, $\overline{\text{HRESET}}$ can be asserted, and the external configuration pins can be set to a new value. The machine state is lost in this process, and, as always, $\overline{\text{HRESET}}$ must be held asserted while the PLL relocks, and the internal state is reset. Second, the introduction of another PLL provides an alternative means of changing the processor clock frequency, which does not involve the loss of machine state, nor a delay for PLL relock.

The following sequence can be used to change processor clock frequency. Assume PLL0 is currently the source for the processor clock. The first step is to configure PLL1 to produce the desired clock frequency, by setting HID1[PR1] and HID1[PC1] to the appropriate values. Next, wait for PLL1 to lock. The lock time is the same for both PLLs and is provided in the hardware specification. Finally, set HID1[PS] to a 1 to initiate the transition from PLL0 to PLL1 as the source of the processor clocks. From the time the HID1 register is updated to select the new PLL, the transition to the new clock frequency will complete within 3 bus cycles.

Once both PLLs are running and locked, the processor frequency can be toggled with very low latency. For instance, when it is time to change back to the PLL0 frequency, there is no need to wait for PLL lock. HID1[PS] can be reset to 0, causing the processor clock source to transition from PLL1 back to PLL0. If PLL0 will not be needed for some time, it can be configured to be off while not in use. This is done by resetting the HID1[PC0] field to 0, and setting HID1[PI0] to 1. Turning the non-selected PLL off results in a modest power savings, but introduces added latency when changing frequency. If PLL0 is configured to be off, the procedure for switching to PLL0 as the selected PLL involves changing the configuration and range bits, waiting for lock, and then selecting PLL0, as described in the previous paragraph.

Caution:
The following hazards must be avoided when reconfiguring the PLLs. First, the configuration and range bits in HID1 should only be modified for the non-selected PLL, since it will require time to lock before it can be used as the source for the processor clock. Second, the HID1[PI0] bit should only be modified when PLL0 is not selected. Third, whenever one of the PLLs is reconfigured, it must not be selected as the active PLL until enough time has elapsed for the PLL to lock. Fourth, at all times, the frequency of the processor clock, as determined by the various configuration settings, must be within the specification range for the current operating conditions. In particular, in systems where V_{DD} may be varied to achieve additional power efficiency, a transition from low frequency to high frequency requires that V_{DD} is at a sufficiently high level to support the higher frequency. Finally, never select a PLL that is in the ‘off’ configuration.

***Configuration Restriction*:** The following restriction on frequency transitions. It is considered a programming error to switch from one PLL to the other when both are configured in a ‘half-cycle’ multiplier mode. For example, with PLL0 configured in 9:2 mode (cfg = 01001) and PLL1 configured in 13:2 mode (cfg = 01101), changing the select bit (HID1[PS]) is not allowed. In cases where such a pairing of configurations is desired, an intermediate full-cycle configuration must be used between the two half-cycle modes. For example, with PLL0 at 9:2, PLL1, configured at 6:1 is selected, then PLL0 is reconfigured at 13:2, locked and selected.

The processor to bus clock ratios supported by 750FX are compared with those supported by the 750CXe in *Table 5-1 PLL Comparison - 750CXe to 750FX* on page 15.

Table 5-1. PLL Comparison - 750CXe to 750FX

	750CXe	750FX
Number and type of PLLs	one externally controlled PLL	two programmable PLLs, one with external controls
PLL full cycle ratios	2,3,4,5,6,7,8,9,10	2,3,4,5,6,7,8,*9*,10,*11,12,13,14,15,16,17,18,19,20*
PLL half cycle ratios	2.5,3.5,4.5,5.5,6.5,7.5	2.5,3.5,4.5,5.5,6.5,7.5,*8.5,9.5*

6. Power, Voltage, Frequency

Due to the technology remaps, all three processors differ in power, voltage, and frequency characteristics. These differences are summarized in the following table. In addition, the dynamic power management (DPM) facility that was available on the 750 and 750CXe is planned to be available on 750FX.

Notes:

DPM does not function on revision level DD1.0, but has been fixed for DD1.1, DD1.2, and planned for DD2.0. See the *PowerPC 750FX RISC Microprocessor Errata List*.

DPM was not available on early revisions of 750CX, but is supported on all revisions of 750CXe.

6.1 750FX Low Voltage Operation (at lower frequency)

For further power savings, the 750FX supports transition between a low power and high power mode, where core voltage (V_{DD}) can be lowered to a specified minimum with a corresponding lower operating frequency. The methodology and rating specifications for switching to lower Voltage/Frequency modes will be defined in the *IBM PowerPC 750FX RISC Microprocessor Datasheet*.

6.2 I/O Voltage mode selection

750FX provides selection for I/O voltages in various ranges of operation; 1.X (1.2, 1.5, or 1.8)V, 2.5V and 3.3V[1]. BVSEL and L1_TSTCLK are used to set these modes. Details will be listed in the *IBM PowerPC 750FX RISC Microprocessor Datasheet*.

Table 6-1. Power, Voltage, Frequency Differences

	750	750CXe	750FX
Silicon Technology	0.22 micron	0.18 micron	0.13 micron
Core Voltage	See the respective PowerPC 750 family microprocessor datasheet for specific values.		
Lower Core Voltage Operation[2]	See the respective PowerPC 750 family microprocessor datasheet for specific values.		
I/O Voltage	1.8V, 2.5V, or 3.3V	1.8V or 2.5V	1.X(1.2,1.5,1.8),2.5V,3.3V[1]
Core Speed Range	See the respective PowerPC 750 family microprocessor datasheet for details		
Maximum bus speed	100MHz[3]	133MHz[3]	150MHz - 200MHz[3]
Power dissipation	See the respective PowerPC 750 family microprocessor datasheet for specific values.		

[1]Revision Level Note: Not supported on revision DD1.X of the 750FX
[2] Lower core voltages may be defined to allow slower operation at substantial power savings.
[3] Applications with higher bus speed may be achievable with special design considerations.

1. Not supported on revision DD1.X of the 750FX

7. Timings

Note: Timings are very processor and technology specific. It should not be assumed that timings remain equivalent between any of the PowerPC microprocessor designs. Timings for each of the IBM PowerPC microprocessor family of products are located within their specific electrical specification, referred to as the *datasheet*. Contact your IBM Sales or technical support group to request the appropriate *IBM PowerPC 750FX RISC Microprocessor Datasheet*.

8. Package

8.1 CBGA

The 750FX is designed on a 21 x 21 mm ceramic ball grid array (CBGA) with 1.0 millimeter pitch solder balls. The signal ball footprint is different from the previous 750 and 750CXe designs.

8.2 Signal Descriptions

The 750FX footprint restores a number of signals that were removed from the 750 PID8p pinout to create the 750CXe, as well as adding new signals specific to the 750FX. The 750FX CBGA has a partially depopulated signal footprint.

Table 8-1. Pins Comparison: 750, 750CXe, 750FX

Pins Removed or Changed From 750 Signals	Pin Functionality	
	750CXe	750FX
AP[0:3]; DP[0:7]	Not present.	60x address and data parity signals.
$\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{DBDIS}}$, $\overline{\text{DRTRY}}$	Not present.	Optional 60x address and data bus protocol signals.
$\overline{\text{RSRV}}$, $\overline{\text{TLBISYNC}}$, $\overline{\text{SMI}}$, TBEN	Not present.	Signals for interrupt, MP, and debug support.
CLKOUT	Test pin, shared with $\overline{\text{CKSTP\_OUT}}$.	CLKOUT is no longer shared with $\overline{\text{CKSTP\_OUT}}$.
L2_TSTCLK	Test pin, shared with $\overline{\text{DBWO}}$.	L2_TSTCLK is no longer shared with $\overline{\text{DBWO}}$; used for factory testing only.
L1_TSTCLK	Test pin.	Factory test shared with 3.3v I/O mode.
DBWO	Shared with L2_TSTCLK.	$\overline{\text{DBWO}}$ is separate input.
VOLTDET	Not present.	Not present.

8.2.1 750CXe Signal Configuration

The 750CX for DD1.0, the $\overline{\text{CKSTP\_OUT}}$ is removed and CLKOUT is present. Beginning with DD2.0, $\overline{\text{CKSTP\_OUT}}$ and CLKOUT share a pin. Functionality for both is still available depending on the setting of the HID0[BCLK] and HID0[ECLK] register bits.

Table 8-2. HID0[BCLK] and HID0[ECLK] CKSTP_OUT Configuration

HRESET	HID0[ECLK]	HID0[BCLK]	CKSTP_OUT
Asserted	x	x	Not Applicable
Negated	0	0	CKSTP_OUT
Negated	0	1	SYSCLK/ 2
Negated	1	0	Processor Core
Negated	1	1	SYSCLK

8.2.2 750FX Signal Configuration

Signals introduced in the 750FX design include PLL_CFG[4] and PLL_RNG[0:1]. PLL_CFG[4] provides an additional PLL configuration bit to support additional processor to bus clock frequency ratios. PLL_RNG[0:1] are used to select a frequency range for the processor clock. This allows a wider range of frequencies to be supported by the PLL(s).

Note: PLL configuration settings are not compatible between 750FX and 750CXe/750. See the *IBM PowerPC 750FX RISC Microprocessor Datasheet*for the correct values.

In addition, a second analog voltage pin, $A2V_{DD}$, has been added to power the second PLL. This input requires its own filter circuit, which should duplicate that corresponding to the $A1V_{DD}$ pin.

The resulting signal and pin count for the package is summarized in *Table 8-3 Pin Count Differences* on page 18.

Table 8-3. Pin Count Differences

	750	750CXe	750FX
Package	360 pin CBGA with 1.27mm pitch	256 pin PBGA with 1.27mm pitch	292 pin CBGA with1.0mm pitch
Signal I/Os	258	139	163

8.3 750FX Mechanical Specifications

Figure 8-1 DD1.0 & DD1.1 Package Top View on page 20 shows the top, bottom, and side profiles of the 750FX package including the height from the top of the die to the bottom of the solder balls.

IBM offers a ceramic ball grid array (CBGA) which supports 292 balls for the 750FX package.

Table 8-4 lists several views of the 750FX physical package.

Table 8-4. Figures Describing the 750FX Package – Dimensions and Signals

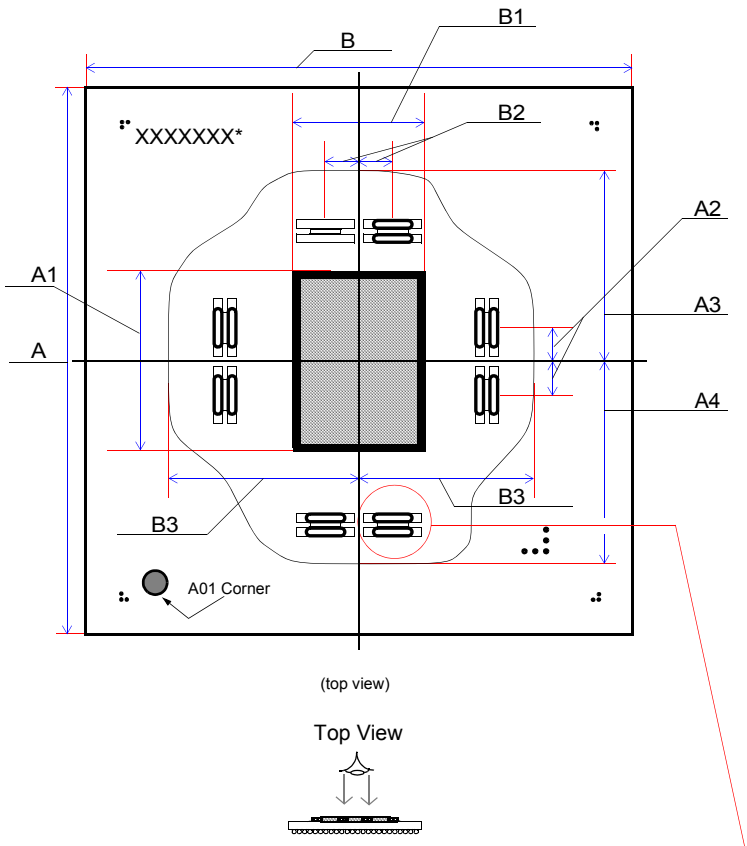
Revision	Figure	Notes
DD1.0 & DD1.1	For a top view of this package, see *Figure 8-1 DD1.0 & DD1.1 Package Top View* on page 20. For a bottom and side view of this package, see *Figure 8-2 DD1.X Package Bottom View (CBGA Package)* on page 21.	1, 2, 3
DD1.2	For a top view of this package, see *Figure 8-3 DD1.2 Package Top View* on page 22. For a bottom and side view of this package, see *Figure 8-2 DD1.X Package Bottom View (CBGA Package)* on page 21.	2, 3
DD2.X	Not shown in this document.	4

Notes:

1. The 750FX DD1.0 and DD1.1 products have an incorrect A01 corner locator marking on the BGA package. A special mark has been added to define the actual A01 pin location. For details see Figure 8-1 on page 20.
2. The side and bottom views are the same for DD1.0, DD1.1, and DD1.2 packages. For a bottom and side views of the 750FX package, see Figure 8-2 on page 21.
3. For details about the 750FX mechanical specifications, ball placement, and signals, see the *IBM PowerPC 750FX RISC Microprocessor Datasheet for DD1.X*.
4. For a details about the 750FX mechanical specifications, ball placement, and signals, see the *IBM PowerPC 750FX RISC Microprocessor Datasheet for DD2.X*.

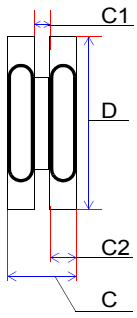
8.3.1 DD1.0 & DD1.1 Package Top View

Figure 8-1. DD1.0 & DD1.1 Package Top View



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. A1 CORNER INCORRECTLY MARKED ON PROCESSOR. CORRECT A1 CORNER IS INDICATED ON THIS DIAGRAM; THERE IS NO BALL MISSING FROM THE ARRAY. ACTUAL A01 CORNER INDICATED BY DOT.
4. PITCH IS 1.0 MM

	MILLIMETERS	
DIM	Minimum	Maximum
A	21	
A1	6.938	
A2	1.5	
A3	7.917	
A4	9.357	
B	21 ± 0.2	
B1	5.327	
B2	1.5	
B3	7.5	
C	1.5	
C1	0.48	
C2	0.51	
D	2.5	

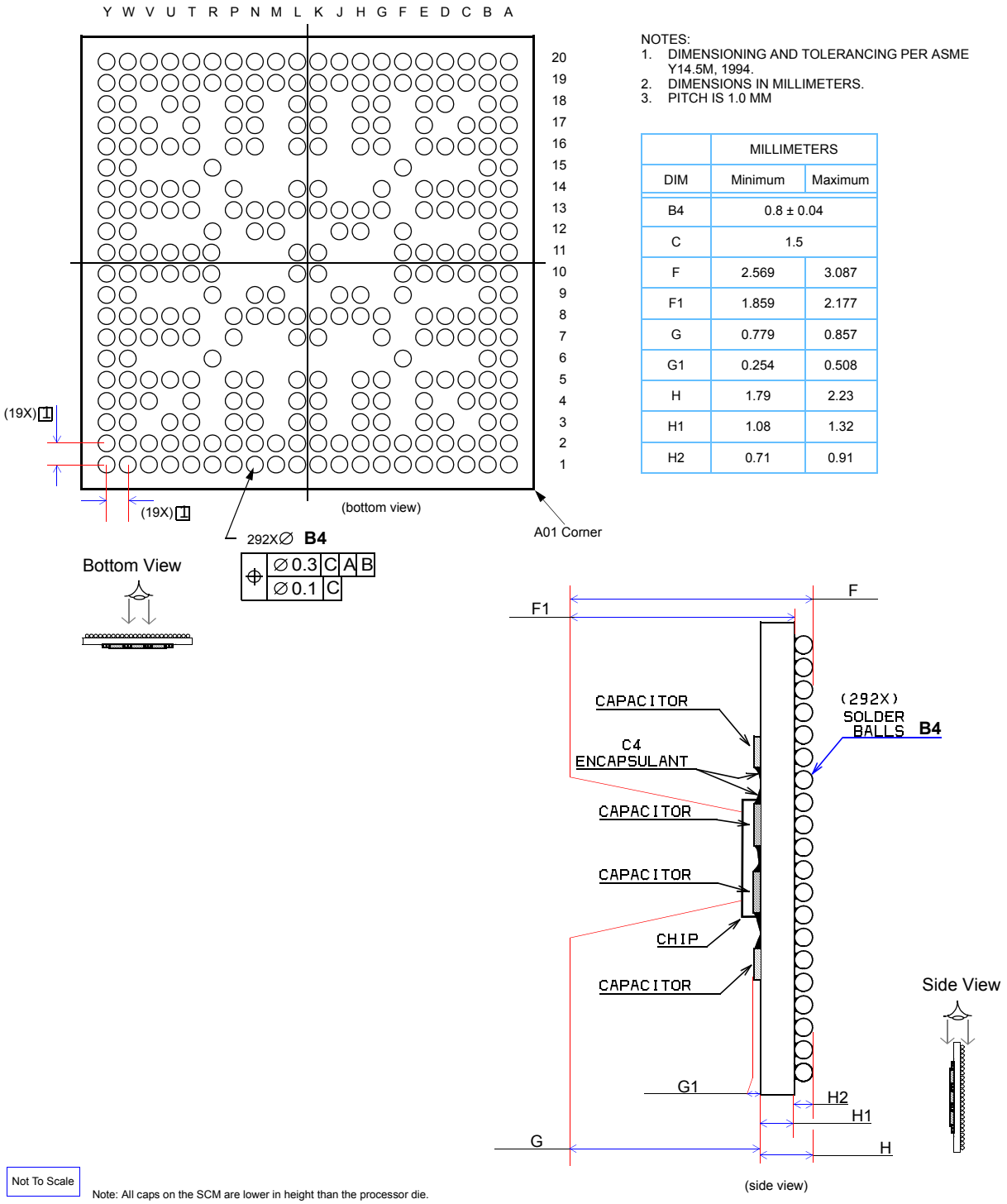


Not To Scale

Note: All caps on the SCM are lower in height than the processor die.

8.3.2 DD1.X Package Bottom View

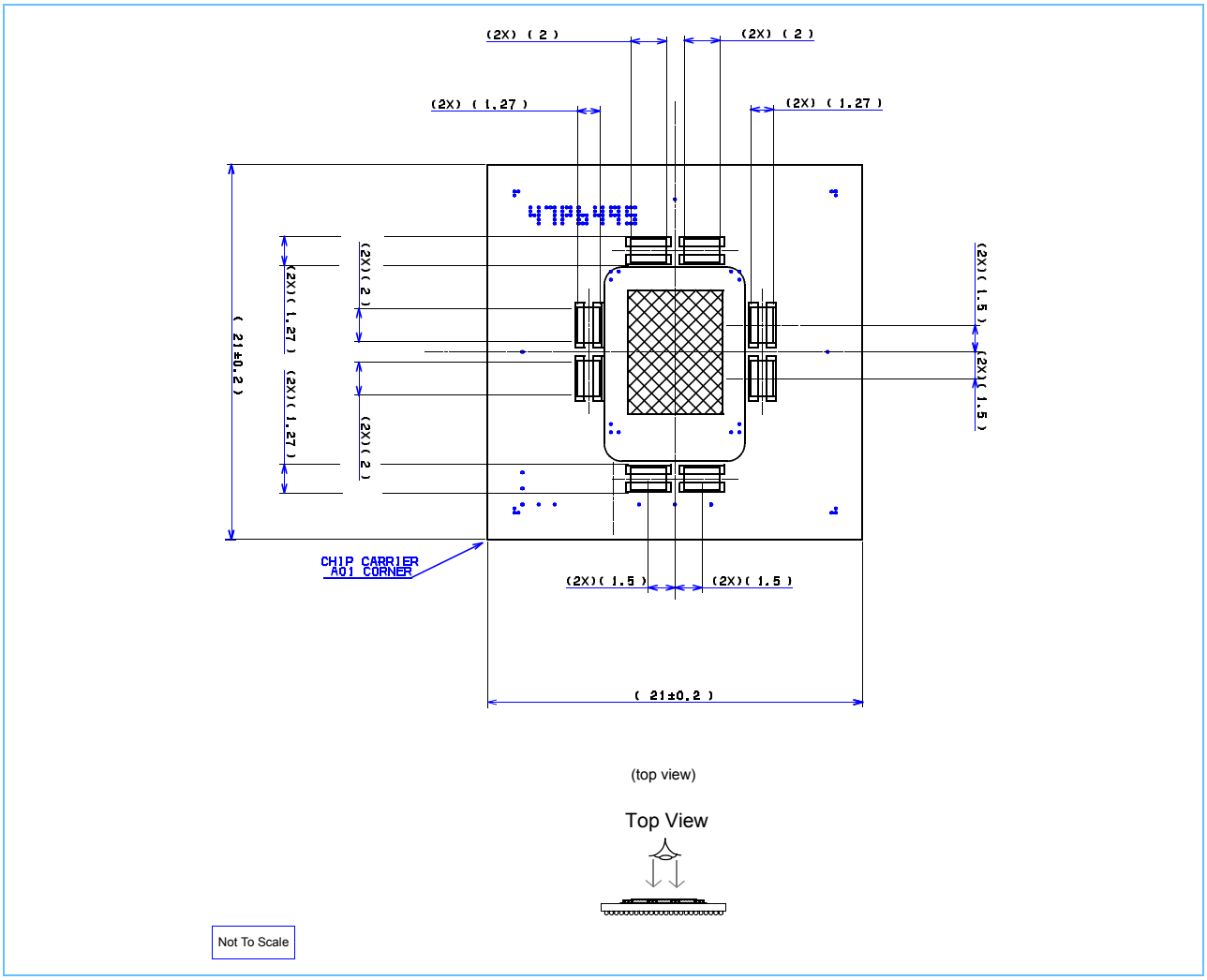
Figure 8-2. DD1.X Package Bottom View (CBGA Package)



	MILLIMETERS	
DIM	Minimum	Maximum
B4	0.8 ± 0.04	
C	1.5	
F	2.569	3.087
F1	1.859	2.177
G	0.779	0.857
G1	0.254	0.508
H	1.79	2.23
H1	1.08	1.32
H2	0.71	0.91

8.3.3 DD1.2 Package Top View

Figure 8-3. DD1.2 Package Top View



8.4 Decoupling Capacitors

The depopulated footprint allows for decoupling capacitors to be placed in a tight group, on the system board, directly behind the 750FX module. The voltage and ground pins are placed in a pattern to facilitate this action. Board designers need to consider layout rules for accommodating the tightly grouped pattern. Recommended capacitor values will be provided, but actual quantity and values will depend on the design. For capacitor information, see to the *IBM PowerPC 750FX RISC Microprocessor Datasheet*.

9. Start-up Functions

The $\overline{\text{DRTRY}}$ signal is optional in the 60x bus protocol. In systems where it is not used, the processor can be configured not to expect it, by selecting 'no-$\overline{\text{DRTRY}}$' mode during start-up. In this mode, the bus interface unit can forward incoming data one bus cycle earlier to the load/store unit, knowing that the data will not be invalidated by a succeeding assertion of $\overline{\text{DRTRY}}$. In the 750CXe, the $\overline{\text{DRTRY}}$ pin is absent, and so cannot be used to post-invalidate received data. Therefore, the 750CXe is always configured in 'no-$\overline{\text{DRTRY}}$' mode.

In the 750 and 750FX, the state of $\overline{\text{DRTRY}}$ is sampled at the negation of the $\overline{\text{HRESET}}$ signal, to determine whether 'no-$\overline{\text{DRTRY}}$' mode is selected. If the DRTRY signal is active-low at start-up, the processor will run in 'no-DRTRY' mode.

Note: The $\overline{\text{DRTRY}}$ signal should NOT be tied low (directly to GND), as this is an invalid condition.

The 750 samples $\overline{\text{TLBISYNC}}$ at negation of $\overline{\text{HRESET}}$ to determine whether the processor will run in '32-bit data bus' mode.[1] In this mode, only four bytes of data are transferred on the data bus at any one time, requiring a two-beat transaction to transfer a double word, and an eight-beat transaction to transfer a cache line. In the 750CXe, the $\overline{\text{TLBISYNC}}$ pin is absent. In this case, the start-up function previously implemented by $\overline{\text{TLBISYNC}}$ is performed by the $\overline{\text{QACK}}$ signal. Although $\overline{\text{TLBISYNC}}$ has been restored to the 750FX, the 750FX DD1.X versions follow the 750CXe model and samples $\overline{\text{QACK}}$ to select 32-bit mode.

The 750FX DD2.0 revision will change from $\overline{\text{QACK}}$ to $\overline{\text{TLBISYNC}}$, as defined for 750: when $\overline{\text{HRESET}}$ is de-asserted, TLBISYNC held high selects 64 bit bus, held low selects 32 bit bus.

9.1 Reduced Pin-Out Mode

To transition from a previous processor model with reduced pin out mode, drive TLBISYNC appropriately, leave the DP(0..7) and AP(0..3) pins floating, and disable parity checking with the HID0 bits. The 750FX, 750CXe, and 750 do not have APE or DPE pins.

1. DD2.0 version of 750FX will change to sample the $\overline{\text{TLBISYNC}}$ pin, like the 750.

9.2 Summary of Start-Up Differences

Table 9-1 provides a summary of the start-up differences between processors.

Table 9-1. Start-Up Differences

	750	750CXe	750FX
no-$\overline{\text{DRTRY}}$ mode	sample $\overline{\text{DRTRY}}$ to select	always in no-$\overline{\text{DRTRY}}$ mode	sample $\overline{\text{DRTRY}}$ to select
32-bit mode	sample $\overline{\text{TLBISYNC}}$ to select	sample $\overline{\text{QACK}}$ to select	DD1.X - sample $\overline{\text{QACK}}$ to select DD2.0 -sample $\overline{\text{TLBISYNC}}$ to select HIGH = 64-bit mode LOW = 32-bit mode

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

Rev	Contents of Modification
May 29, 2002	Initial preliminary release of version 1.0.