1. Introduction

This application note provides a checklist of items to consider when reviewing schematics. This checklist includes common errors and issues faced by customers while working with the Marvell® GT-64260A device. Failure to check these items carefully can lead to expensive debug time and often necessitates a new spin on boards.

This application note does not cover all the possible errors that may occur when checking schematics. It is the designer's responsibility to ensure the accuracy of the design. The GT-64260A datasheet is the authoritative document to use when checking the schematics. If you have any questions or comments, please contact Marvell's technical support.

2. Document Checklist

Make sure that you have the latest version of the following documents:

- ❏ Datasheet
- ❏ Errata
- ❏ Documentation Changes and Updates (DCU)
- ❏ Evaluation board schematics

3. Check Reset Configuration Pull-up and Pull-down

Note

The CPU must not issue any access to the device for at least ten (10) TClks after the reset de-assertion.

- ❏ Double-check the reset configuration pull-up and pull-down resistors against the datasheet.
  - If your system does not support SDRAM UMA (e.g., AD[12] is set to "0" and the SDRAM UMA is disabled), make sure that the UMA Device Type bit is configured to the UMA Master. (AD[13] must set to "0"). See the DCU "GT-64260A System Controller for PowerPC Processors" Rev. B, change #22 for more details.
  - Only pull-down is needed for AD[28-29]. See DCU "GT-64260A System Controller for PowerPC Processors" Rev. B, change #22 for more details.
- ❏ All pins sampled at reset must be pulled to a defined logical state. This includes the pins that are set as is "don't care" in the customer's system.
- ❏ Make sure that there is no other device driving the AD[31:0] bus during power-up. For example, the "Bus Hold" feature found in many buffers and transceivers prevents CMOS inputs from floating during reset configuration, and thereby sustains the bus value.
- ❏ Have a "stuffing" option to support both pull-up and pull-down if you are not sure which way to pull.
- ❏ If a serial ROM is used for the initialization of GT-64260A, the minimum numbers of strapping resistors needed is listed in Table 1.

All of the following pins must be configured to the intended value during Serial ROM initialization.

Table 1: Pin Description

Pin	Description
AD[1]	Serial ROM Byte Offset Width
AD[3:2]	Serial ROM Address
AD[4]	CPU Data Endianess
AD[7:6]	CPU Bus Configuration
AD[8]	Internal 60x bus Arbiter
AD[9]	Multiple GT-64260A Support
AD[11:10]	Multi-GT-64260A Address ID
AD[12]	SDRAM UMA
AD[13]	UMA Device Type
AD[16]	PCI Retry
AD[23]	SDClk select
AD[24]	Internal Space Default Address
AD[28:30]	PLL Settings
AD[31]	CPU Interface Voltage

Note

When using the ROM for initializing the GT-64260A's internal registers, the ROM's data must be in Little Endian mode. This also applies when interfacing with a CPU that is set to Big Endian mode. Refer to GT-64260A-B-0 Errata and Restrictions, FEr #1: I^2C serial ROM in Big Endian mode.

4. PLL

Make sure that you are using the latest revision of the PLL circuit recommended by Marvell. Our filter is a "generic" filter. Each system usually has its own noise that should be filtered.

5. Clock Signal

- ❏ When configuring the CPU interface clock to run on the same clock with SysClk (SysClk = TClk), SysClk must not be floating. TClk will drive all the internal logic.
- ❏ SDClkOut must never be used. Refer to AN-82 "SDRAM clocking schemes in the GT-642xx/A" for more details.
- ❏ The PCI clock frequency must not exceed the TClk frequency.

6. CPU Interface

- ❑ Make sure that all these signals are pulled-up: A[0:31], AP[0:3], TS*, TBST*, TSIZ[0:2], TT[0:4], GBL*, ABB*, DBB*, and ARTRY*. In the case of a CPU that implements a bus holder, such as 750FX, follow the CPU datasheet requirements. Usually TS*, ABB*, DBB* & Artry* must have pull-ups.
- ❑ The following signals also require pull-ups: TA*, AACK* if used in multi-GT mode.
- ❑ The recommended pull-ups in order to avoid unstable states at reset are: BR0*/GT_BG*, BG0*, DBG0*, BR1*/GT_DBG*, DBG1*, BG1*/GT_BR.
- ❑ The DTI[0:2] signals must be configured as follows:
  1. When using the MPC7400/7410, DTI0 is DBWO* in 60x mode, make sure it is pulled high.
  2. When using the same board for MPC75x and MPC7400/7410 in 60x mode, DTI1 is used as DRTRY* for MPC75x and it must be pulled high.
  3. For all other configurations, pull them down.
- ❑ If you have mictors on the CPU interface, make sure that this interface is simulated.
- ❑ If the CPU interface is not in use, the following signals are pulled as listed:
  - Pull-up: A[0:31], AP[0:3], BR0*, BR1*, TS*, TBST*, TSIZ[0:2], TT[0:4], ARTRY*.
  - Pull-down: AD[5] and AD[9:6].
  - Needs pull, must not be floating: SysClk.

7. Memory Interface

- ❑ If you are not using ECC[7:0], a pull-up is required.
- ❑ If you are using UMA mode, make sure there are pull-ups on SCS[3:0]*, DWr*, SRAS*, and SCAS*, Dadr[12:0], BankSel[1:0].
- ❑ If you are not using the memory interface, the following reset pins must be configured as follows:
  - Set AD[12] and AD[13] to ‘0’ to disable UMA support.
  - Set AD[23] to ‘0’ to support SDClkOut.
- ❑ REGE signal on SDRAM DIMM - Some DIMMs have an internal pull on this pin, and some don't. Don't rely on this internal PLL and make sure you drive this pin as desired.
- ❑ Make sure that this interface is simulated.

8. Device Interface

- ❑ If you are not using Ready* pin, tie Ready* pin to GND.
- ❑ The Motorola MPC7450 performs burst reads during boot, even though its caches are disabled. When interfacing with this CPU (and other CPUs in the future), the boot device must be 32-bits wide.
- ❑ Make sure that the address connections correspond to the device width as follow:
  - For an 8-bit device: BAdr[2:0] are used as device address[2:0]. Latched AD[27:2] are used as device address[28:3].
  - For a 16-bit device: BAdr[2:0] are used as device address[2:0]. Latched AD[27:3] are used as device address[27:3].
  - For a 32-bit device: BAdr[2:0] are used as device address[2:0]. Latched AD[27:4] are used as device address[26:3].

Note

Refer to the interfacing with 8/16/32-bit devices section of the datasheet and also the Hardware Design Guide.

- ❏ Make sure that the boot device width is configured correctly at the boot strapping.
- ❏ Make sure that none of the latches or buffers sitting on the device bus have internal bus holds. These can interfere with the correct boot strapping.
- ❏ If you are not using the device interface, pull down the Ready* pin.

9. PCI Interface

- ❏ Make sure that VREF0/1 is connected directly to the 3.3V or 5V power plane.
- ❏ Decide which PCI arbiter to use.
- ❏ If you use the internal PCI arbiter, the pull-up must be set on all GNT* signals.

32-bit PCI bus

- When the PCI is configured as a 32-bit bus, the GT-64260A drives PADx[63:32] and CBEx[7:4], and a pull-up is not required.
- A pull-up is required for PAR64x and REQ64*.

64-bit PCI bus

- When the PCI is configured as a 64-bit bus, the PADx[63:32] and CBEx[7:4] require pull-up as per the PCI specification.

- ❏ If you are not using the PCI interface (to bypass the requirement of putting pull-ups on the following signals: AD[63:0], CBEx[7:0], PARx, PAR64x), then do the following:
  1. Connect the PCI Rst0/1* to the SysRst*.
  2. Pull down the GNT0/1*.
  3. Connect the PCI Clk0/1 to a clock (this can be a very slow clock, requiring only a few cycles).
  4. Pull up DevSel*, Trdy*, Stop*, ACK64*, PERR*, SERR*, HS, P64En*.

10. MPSC Interface

- ❏ If not using port S0, configure the port to MPSC and pull down pins S0[6:0].
- ❏ If not using port S1, configure the port to MPSC and pull down pins S1[1] and S1[6:3].

11. Ethernet Interface

- ❏ If not using port E0, pull down all of its inputs. To minimize the number of pull-downs, configure the port to MII and pull-down pins E0[1] and E0[14:6].
- ❏ If not using port E1, pull down all of its inputs. To minimize the number of pull-downs, configure the port to MII and pull-down pins E1[1] and E1[14:6].

12. MPP Pins

- ❏ If MPP is not used, all signals must be configured as outputs. The recommendation is to pull these signals either up or down so the hardware will be protected from software errors.

13. JTAG Interface

An incorrect pull of the JTAG signals could result in a hang upon reset.

❏ Pull-up required:

- TMS

❏ Pull-down required:

- TCK
- TRST*
- TDI

14. I^2C Interface

❏ If I^2C is not used, then pull-up I2CSCK and I2CSDA.

15. Miscellaneous

❏ Make sure you comply with the Marvell power sequence requirements (see Application Note 67, "Powering Up/Powering Down Galileo Technology Devices with Multiple Power Supplies of Different Voltages").

Marvell
700 First Avenue
Sunnyvale, CA 94089
Phone: (408)222 2500
Sales Fax: (408)752 9029
Email commsales@marvell.com