APPLICATION NOTE

SDRAM Clocking Schemes in the GT-642xx and GT-642xxA/B Devices

AN-82

1. Introduction

The Marvell® GT-642xx and GT-642xxA/B high-end devices are capable of achieving speeds of up to 133 MHz. Operating at these frequencies leaves little room for timing margins and requires careful design for high signal integrity. When interfacing with SDRAM DIMMs, the problem is even more acute as the clock-to-out of an SDRAM DIMM is 5.4 nS while the clock cycle time is 7.5 nS. The GT-642xx and GT-642xxA/B (hereafter referred to as "GT devices") provide clocking options that should enable achieving these high frequencies.

This document provides details on these clocking schemes. An example of physical connection is provided in "Sample Implementation on the EV-642x0A" and a theoretical calculation example is provided in "Example of Trace Length Calculations".

2. Clocking Options

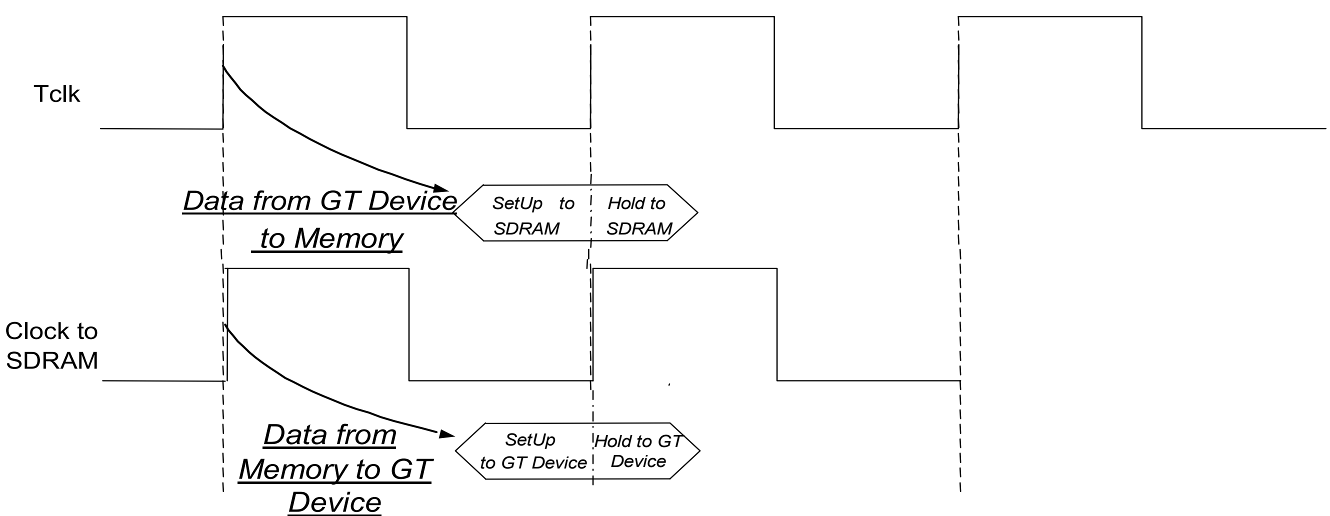
The GT-642xx has two options for connecting the SDRAM interface: Tclk and SDClkOut. The GT-642xxA/B has an additional option: SDClkIn.

2.1 Tclk

This is the basic mode. In this mode, all clocks in the system are "synchronized" i.e., there is no skew between the receiving side or the transmitting side of the GT device and the SDRAM clocks.

The SDClkOut pin of the GT device is left unused.

Figure 1: Clock Relations When Working in Tclk Mode



2.2 SDClkOut

In this mode, the GT device supplies the clock signal to the SDRAM. This way better clock-to-out can be generated by the GT device. In other words, the cycle time for the write path is larger than the clock cycle time.

Note

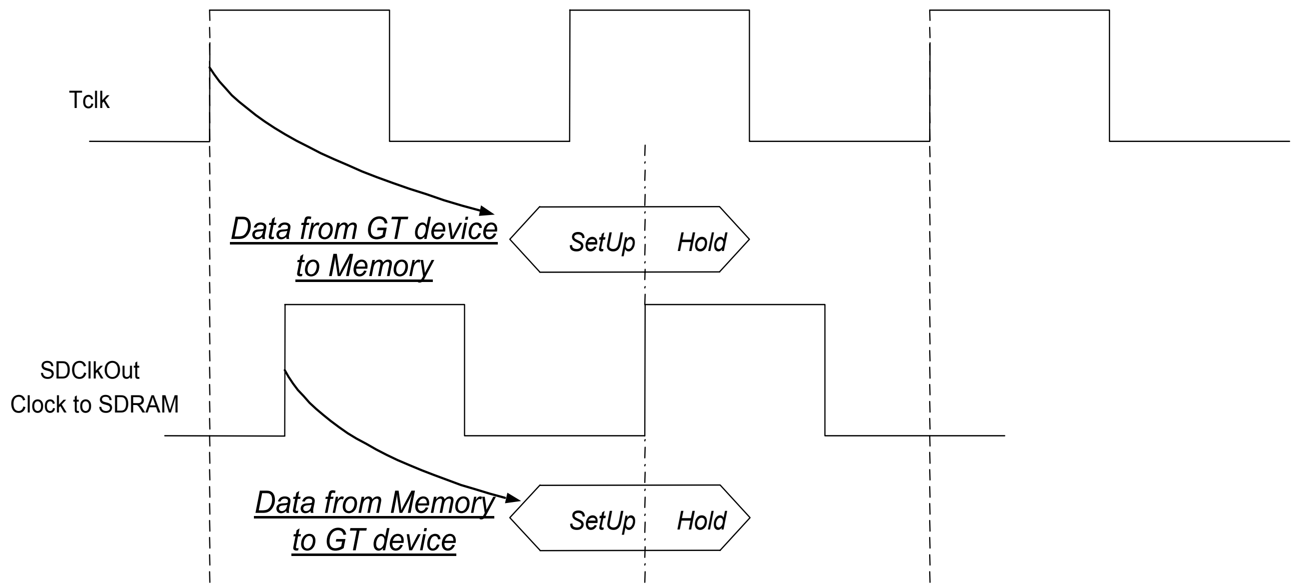
Marvell does not recommend working in this mode. For the GT-642xx, the highest frequency available is 100 MHz. Tclk mode is sufficient and should be selected. For the GT-642xxA/B, SDClkIn should be the preferred method of clocking. See Section 2.3 "SDClkIn" on page 2 for more details.

Working in this mode adds one sampling stage in the read direction thus adding one clock cycle to the latency of a read from the SDRAM.

This resolves issues with driving heavier loads such as control signals (RAS, CAS, DWR, etc.) and address lines.

As shown in Figure 2, this mode does not improve the returning data path. The read path cycle time is equal to the clock cycle time. The data is sampled in the GT device with the SDClkOut signal and is then sampled again with Tclk.

Figure 2: Timing When Using SDClkOut



2.3 SDClkIn

This mode exists only in the GT-642xxA/B. The assumption behind this implementation is that the AC timing of the read path allows for no margin, but the GT device can compensate for the high output delay of the SDRAM inside the chip, i.e., the AC timing of a path inside the chip is much faster than AC timings on the PCB.

The idea is that a skewed clock is supplied externally into the SDClkOut ball of the GT device. The GT device is configured to use this ball as an input by sampling AD23 high at reset.

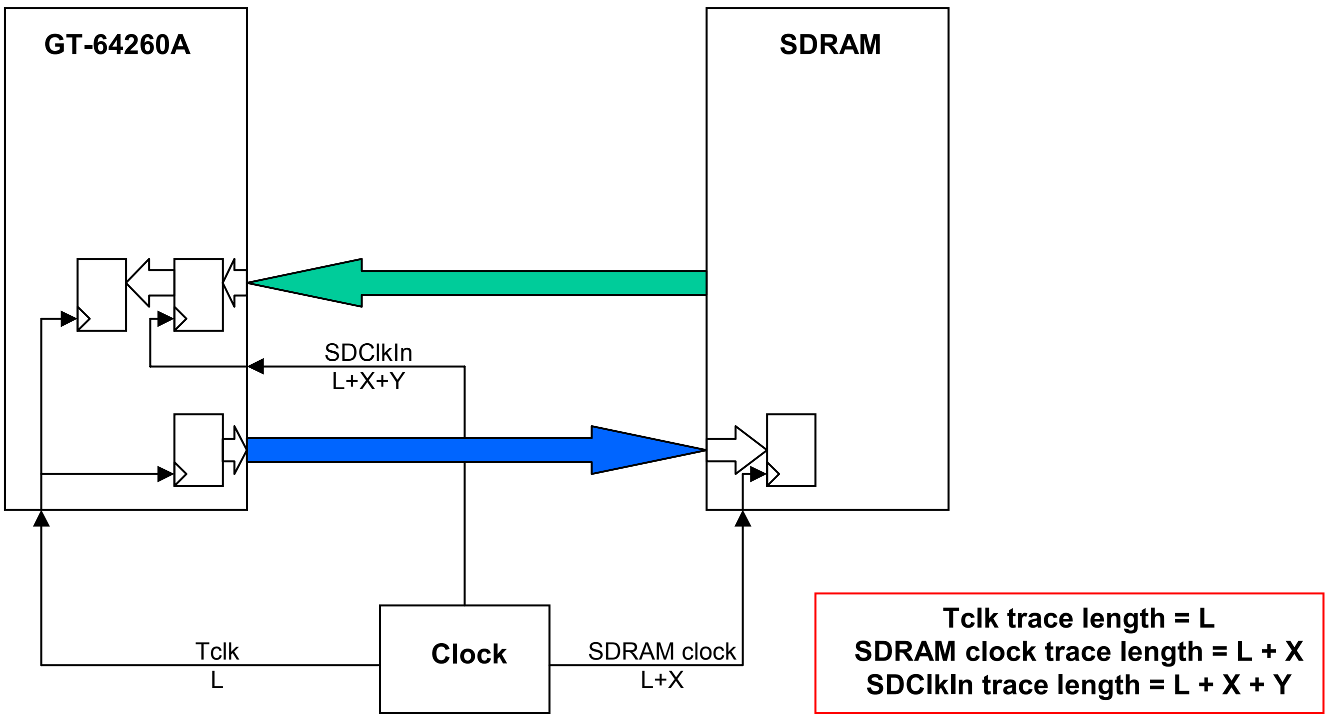
Note

If the GT–642xxA/B SDClkOut/SDClkIn pin is configured as SDClkIn, the Heavy Load mode cannot be used. The SDRAM Configuration register (Offset: 0x448) SDLoad bit [19] must be set to ’0’.

2.3.1 Timing

Figure 3 shows the relationship between the system clocks. In this method, both path directions gain additional margin.

Figure 3: Block Diagram of SDRAM Interface



GT Device to SDRAM

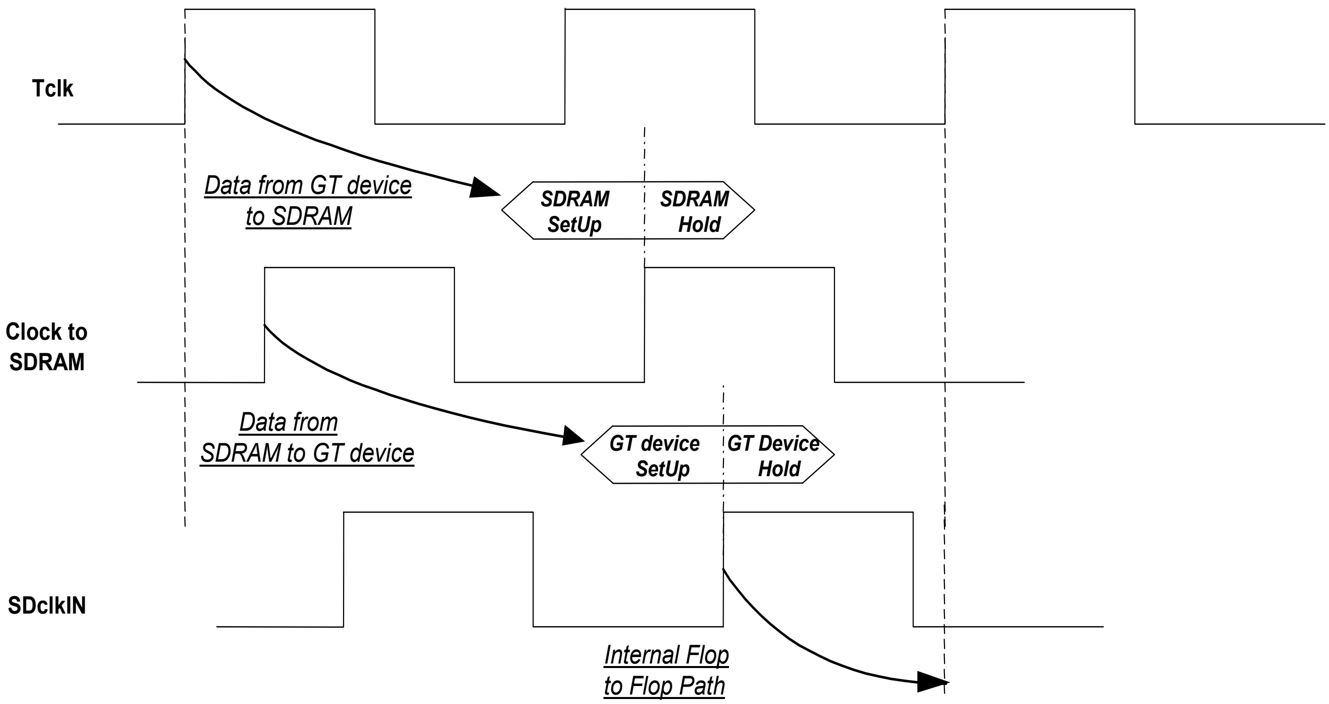
In the case of signals driven by the GT device to the SDRAM, the SDRAM uses the SDRAM clock to sample signals generated by the GT device with Tclk. The SDRAM clock can be skewed from Tclk using a longer trace length. This way, the cycle time of the write path can be longer than the clock cycle time. The maximum skew allowed is limited to the hold time requirements of the SDRAM.

SDRAM to GT Device

In the case of signals driven by the SDRAM to the GT device, signals are generated by the SDRAM with the SDRAM clock and are sampled by the GT device with the SDClkIn clock. The SDClkIn clock can be skewed from the SDRAM clock using a longer trace length. This way, the cycle time of the read path can be longer than the clock cycle time. Again, the maximum skew allowed is limited to the GT device hold time and the internal path timing between the two internal sampling stages.

After the data is sampled with the SDClkIn, it is sampled again with Tclk. This means that there is an additional sampling stage resulting in longer latency. At this point, the data is again synchronized to the GT device's internal clock.

Figure 4: Timing when using SDClkIn



2.3.2 Calculating the Correct Clock Skew

To achieve the desired skew between the clocks in Figure 3, the formulae below should be calculated. See "Example of Trace Length Calculations" for an example of this calculation.

Three formulae define the clock skews (or clock trace lengths) needed:

Internal flop-to-flop path

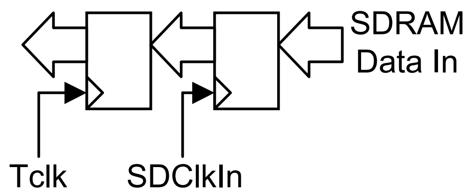
X + Y < Tcycle - 3.85

This formula is derived from the way the incoming signals (data read) from the SDRAM are sampled first with SDClkIn, and then are sampled again (internally) with Tclk. The time allowed from the first sampling stage (that is clocked with SDClkIn) to the second stage (that is clocked with Tclk) is Cycle time minus 3.85 nS (this includes clock-to-out, propagation and setup of this internal path).

X = Additional delay to the clock going to the SDRAM compared to Tclk.

Y = Additional delay to the clock going to the SDClkIn compared to the clock received by the SDRAM.

Figure 5: Sampling Stage with SDClkIn



Path from GT Device to SDRAM

Tcycle > Tco1 + Tfly1 + Tsu1 - X

Tcycle = Cycle time

Tco1 = Clock-to-out of the GT device

Tfly1 = Signal flight time + clock skew + clock jitter

Tsu1 = Setup time of the SDRAM

This formula reflects the requirements for signals going from the GT device to the SDRAM (control, address, write data, ECC, etc.). This calculation needs to be repeated for the different types of signals as they have different timing (depending on AC specification of the device, trace routing, etc.). The greatest sum of Tco1+Tfly1+Tsu1 is the number that should be used.

Path from SDRAM to GT Device

Tcycle > Tco2 + Tfly2 + Tsu2 - Y

Tco2 = Clock-to-out of the SDRAM

Tfly2 = Signal flight time + clock skew + clock jitter

Tsu2 = Setup time of the GT device

This formula reflects the requirements for signals coming from the SDRAM to the GT device (read data).

Verifying Hold Time Requirements

Once the above formulae are calculated and X and Y values are found, the result must be verified against Hold Time requirements and the following formulae need to be calculated:

Thold1 + X < Tco3 + Tfly3

Thold1 = Hold time of the SDRAM

Tco3 = Minimal clock-to-out of the GT device

Tfly3 = Signal flight time - clock skew - clock jitter

Thold2 + Y < Tco4 + Tfly4

Thold2 = Hold time of the GT device

Tco4 = Minimal clock-to-out of the SDRAM

Tfly4 = Signal flight time - clock skew - clock jitter

3. Implementation

Figure 6 illustrates the implementation of the SDRAM clocking schemes in the GT-642xxA/B.

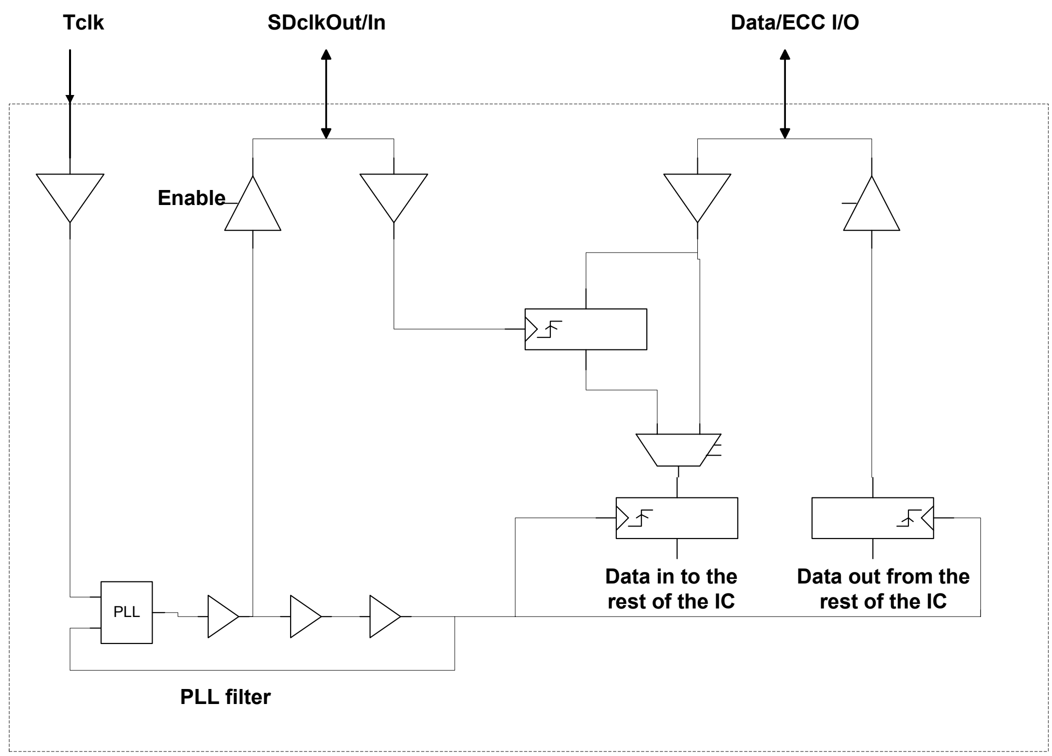
Note the following:

SDClkOut/In	This ball can be configured as output (SDClkOut) or input (SDClkIn). The decision is based on the value sampled at reset on pin AD23. Sampling this pin as logical ’0’ configures the GT device to drive SDClkOut by enabling the output driver. Sampling this ball as logical ’1’ configures the GT to receive the SDClkIn clock.
Added sampling stage	On the incoming path, there is an additional sampling stage. This sampling stage receives its clock from either the SDClkOut or the SDClkIn, depending on the reset configuration as stated above.
Mux after sampling	The mux selects whether or not to use the sampling stage to synchronize the data from the SDClk-Out or SDClkIn domain to the Tclk domain. When working in the Tclk mode, this synchronization is not needed. Determining the selection of the mux is done through the SDRAM timing parameters register at offset 0x4B4. Setting bit 12 of this register to ’1’ selects the synchronization path. Setting it to ’0’ bypasses the sampling stage.

Note

The default value for this bit is '0' and it must be set to '1' in order to work with SDClkIn

Figure 6: Implementation of SDRAM Clocking in the GT-642xxA/B



4. Conclusions and Recommendations

4.1 GT-642xx

The GT-642xx has two SDRAM clocking options: Tclk and SDClkOut.

- As this device's maximum frequency is 100 MHz, working with Tclk should be the preferred method of clocking. This should be based on timing of IBIS simulations to prove that the design allows for this frequency.
- In the GT-642xx, working with SDClkOut will cause a latency increase of 1 clock cycle (one sampling stage added). As noted before, working in this mode is not recommended.
- Working with SDClkOut does not improve results in the read direction; only in the write direction.

4.2 GT-642xxA/B

The GT-642xxA/B has three clocking options: Tclk, SDClkIn, and SDClkOut.

- If the system design permits, the Tclk clocking method is the preferred clocking method.
- For frequencies and designs that do not support Tclk clocking method, the SDClkIn method should be used.
- Avoid using the SDClkOut method when using the GT-642xxA/B.

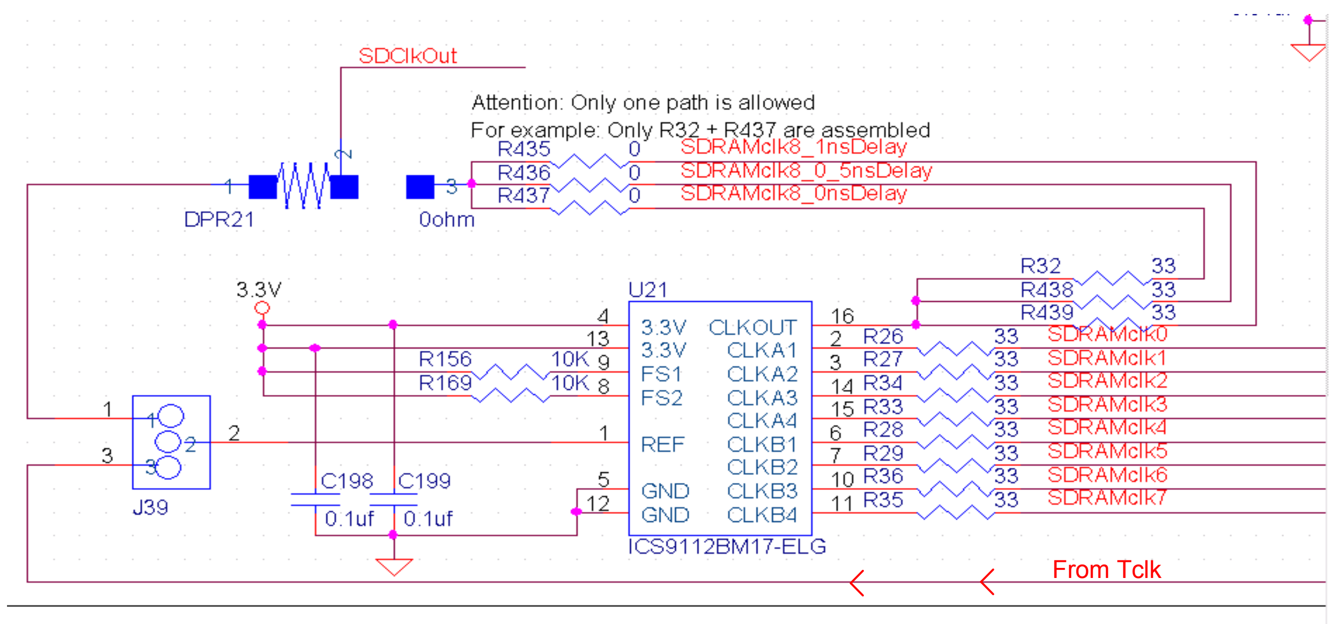
Sample Implementation on the EV-642x0A

The schematic sample shown below is part of the EV-642x0A schematic.

The implementation below allows for one of the three configurations to be selected and used in the system:

Tclk	Connecting J39 between pins 2 and 3 supplies the zero-delay clock buffer with a reference clock from Tclk. The SDRAM clock signals are fed by this buffer.
SDClkOut	Connecting J39 between pins 1 and 2, and assembling the 0 ohm resistor of the DPR21 between 1 and 2 feeds the clock buffer with the SDClkOut signal coming from the GT device. In addition, AD23 of the GT device needs to be sampled low at reset to generate the SDClkOut signal. This delayed clock is then fed to the clock buffer that generates the SDRAM clocks.
SDClkIn	In this case, DPR21 is assembled between pads 2 and 3. J39 is connected between 2 and 3 and feeds the clock buffer with Tclk. SDClkIn is fed back to the GT device through one of the three resistor pairs (R32 and R437, R438 and R436, R439 and R435). Each pair is routed differently on the board resulting in different trace lengths. Assembling one of these three pairs selects one of three possible trace lengths.

Figure 7: SDRAM Clocking Implementation in the EV-642x0A



Example of Trace Length Calculations

The following is an example of how to calculate the trace lengths:

As detailed in Section 2.3.1 "Timing" on page 3, the formulae to be calculated are as follows:

1. X + Y < Tcycle - 3.85
2. Tcycle > Tco1 + Tfly1 + Tsu1 - X
3. Tcycle > Tco2 + Tfly2 + Tsu2 - Y

Where: the parameters in the formulae are defined as follows:

Tcycle = 7.5 nS (@ 133 MHz)

Tco1 = Clock-to-out of the GT device. The GT device's largest number is 4.1 nS for ECC.

Tfly1 = Signal flight time + clock skew + clock jitter. In our example, we'll assume 2 nS.

Tsu1 = Setup time of the SDRAM. "-7" SDRAM DIMMs give a number of 1.5 nS.

Tco2 = Clock-to-out of the SDRAM is usually 5.4 nS.

Tfly2 = Signal flight time + clock skew + clock jitter. The assumption is 2 nS

Tsu2 = Setup time of the GT (0.15 nS)

Results:

From formula 2: 7.5 > 4.1 + 2 + 1.5 - X, the result is: X > 0.1 nS

From formula 3: 7.5 > 5.4 + 2 + 0.15 - Y, the result is: Y > 0.05 nS

For the Hold requirements:

1. Thold1 + X < Tco3 + Tfly3 results in X < 1.3 nS
2. Thold2 + Y < Tco4 + Tfly4 results in Y < 3.1 nS

Where:

Thold1 = Hold time of the SDRAM = 0.8 nS

Tco3 = Minimal clock-to-out of the GT = 1.3 nS

Tfly3 = Signal flight time - clock skew - clock jitter = 0.8 nS

Thold2 = Hold time of the GT = 0.7 nS

Tco4 = Minimal clock-to-out of the SDRAM = 3 nS

Tfly4 = Signal flight time - clock skew - clock jitter = 0.8 nS

We can therefore calculate:

X = 1 nS; Y = 2 nS

assuming that 1" = 180 pS delay,

the result is X = 5.5” and Y = 11"

Revision History

Revision	Date	Comment
A	February 27, 2002	First revision.
B	May 14, 2003	1. Added the GT-642xxB part to the document. 2. Added the following note to Section 2.3 "SDClkIn" on page 2: **NOTE:** If the GT–642xxA/B SDClkOut/SDClkIn pin is configured as SDClkIn, the Heavy Load mode cannot be used. The SDRAM Configuration register (Offset: 0x448) SDLoad bit [19] must be set to ’0’. 3. Revised description for SDClkOut/In in Section 3. "Implementation" on page 6. The new text is as follows: This ball can be configured as output (SDClkOut) or input (SDClkIn). The decision is based on the value sampled at reset on pin AD23. Sampling this pin as logical **‘0’** configures the GT device to drive SDClkOut by enabling the output driver. Sampling this ball as logical **‘1’** configures the GT to receive the SDClkIn clock.

Marvell
700 First Avenue
Sunnyvale, CA 94089
Phone: (408) 222 2500
Sales Fax: (408) 752 9029
Email commsales@marvell.com