APPLICATION NOTE

CPCI® HOTSWAP
GT-642xx and GT-64120A Boards Hardware Compliance

AN-105

Introduction

This application note addresses basic problems associated with the particular requirements for the Hot Swap procedure of Add-In boards containing the Marvell Discovery GT-642xx and GT-64120A ICs in CPCI Bus environments. These guidelines allow the incorporation of the Hot Swap feature into the boards to eventually comply with the specifications as stated in the *CompactPCI® Hot Swap Specification*, **"**Release Notes for PICMG 2.1 Revision 2.0**",** dated January 17, 2000. Refer to this specification document.

It is also assumed here that the board designer will adhere to the connectors' characteristics, pin assignments, and bus driving -loading as defined in the CompactPCI® bus specification.

Specifically, this document applies to the following devices:

- GT-64120A
- GT-64240/1/2A
- GT-64240/1/2B
- GT-64260/1/2A
- GT-64260/1/2B

Note

Within the context of this document, these devices will be referred to as "GT-64xxx".

Board Electrical Requirements

The hardware features of CPCI Add-In boards, as defined in the C*ompactPCI® Hot Swap Specification*, provide the means to comply with the specification in the following issues:

- Precharging
- Bus isolation
- Power usage
- ESD
- Reset
- Mechanical

Power supply issues for the Marvell Discovery ICs are covered in Marvell's AN-67. The precharging, mechanical, reset, and ESD issues are not affected by the on-board IC types. Therefore, this note only covers issues peculiar to the CPCI Bus Interface for GT-64xxx ICs.

Bus Isolation Requirements

When a board is inserted or removed from a bus, it goes through a power up or a power down sequence. If special care is not taken during this process, backplane signal integrity problems or even permanent damage to sensitive IC devices can occur.

Assuming power up and power down sequences are properly taken care of, the board designer is required by the CPCI specification to prevent two potential problems that may affect the rest of the system and the board. During biasing voltages up or down transitions, ICs may not necessarily behave as specified, but rather exhibit erratic behavior. This is an immediate cause of backplane signal integrity problems.

During board insertion or removal, the power up/down sequence does not guarantee I/O pads from the following occurrences:

- Incidentally driving their corresponding bus signals
- Being driven by the bus signal prior to bias build up

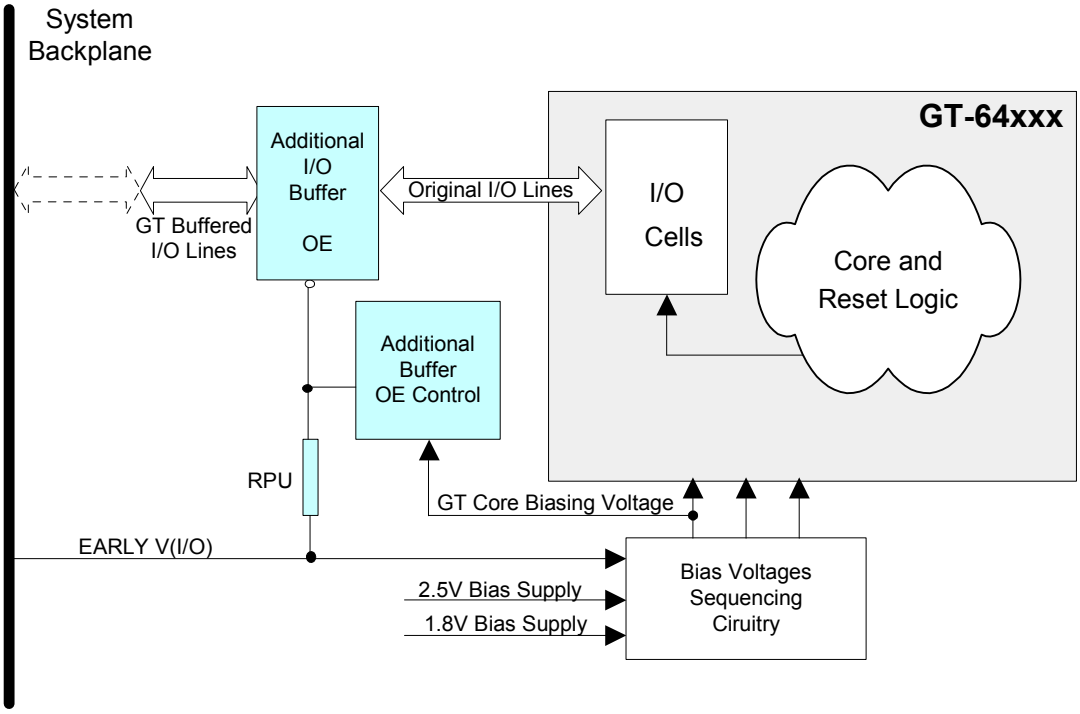
Additional buffering of the original I/O signals is required to prevent the undesired driving from or to the board during the temporary and partial absence of bias voltages. This additional I/O buffering is capable of effectively separating between the board's I/O signal lines during the power up or power down sequences. In the case of insertion, the additional buffering behaves transparently during the normal operation, i.e. after the board has finally completed the insertion process.

The additional buffering requires some kind of Output Enable (OE Control), which can be implemented easily.

The following three new components were added to the original circuit (see Figure 1):

- Additional I/O Buffer
- Additional Buffer OE Control
- Pull up resistor (RPU)

Figure 1: Additional Buffering and OE Control



The additional buffer OE control block and the pull-up resistor (RPU) control the OE pin of the additional I/O buffer. The additional I/O buffer guarantees that the additional buffers remain in the OFF (disconnect) state when their bias voltage and OE pin are kept at the same potential. They go into the ON (connect) state, as specified by their manufacturer, if they are properly biased and their OE pin is asserted as indicated (generally a LOW is required).

The correct driving of the OE pin is achieved by using the core biasing voltage as an indication that the core has reached its final biasing value: indicating that the GT-64xxx IC is "healthy". If the OE control pin is not asserted, the additional buffer is kept in the OFF state. This is guaranteed by the RPU. The backplane is effectively disconnected from the board. When the system reaches the point from which it is guaranteed to behave as specified, the OE pin is asserted to allow the transfer of signals via the I/O lines.

The additional buffer I/O control block may include an extra delay, if necessary. The delay is inserted prior to asserting the additional buffer's OE pin, depending on the specifics of the board in question.

An Example of Bus Isolation Implementation

The implementation of additional circuitry required to prevent the original I/O signals from interfering with the bus is relatively simple. Buffers with several bit widths are readily available from several manufacturers.

The additional I/O buffer functions as a series connected switch. The switch is forced into the OFF state whenever the board is inserted or removed from the system, and is switched into the ON state in the course of normal operation. This is achieved by controlling the buffer's device OE pin with the resistor (RPU), in conjunction with the circuitry contained in the Additional Buffer OE Control block, such as an Open Drain output voltage comparator.

Among the numerous manufacturers who offer competitive buffer parts are IDT and TI:

- IDT offers switches based on its well known technology, in a variety of bit widths and packages, exhibiting typical ON state switch resistances of 5 Ohms and propagation delays under 250ps @ C_L=50pF, with a max. OFF state current of ±1uA.
- TI offers bus switches based on crossbar technology, functionally similar to IDTs, but with different bus widths.

Take the following parameters into consideration when selecting the bus switch device:

- Maximum device operating frequency
- Maximum channel ON state resistance
- Channel ON resistance matching
- Maximum device power dissipation

Based on the Switch device's parameters, the user should check his board's I/O timing design to ensure its proper operation after the introduction of the Bus Switch device. The user should also verify that the device's maximum power dissipation, quiescent and dynamics considered under the worst expected conditions, never exceeds the specified maximum.

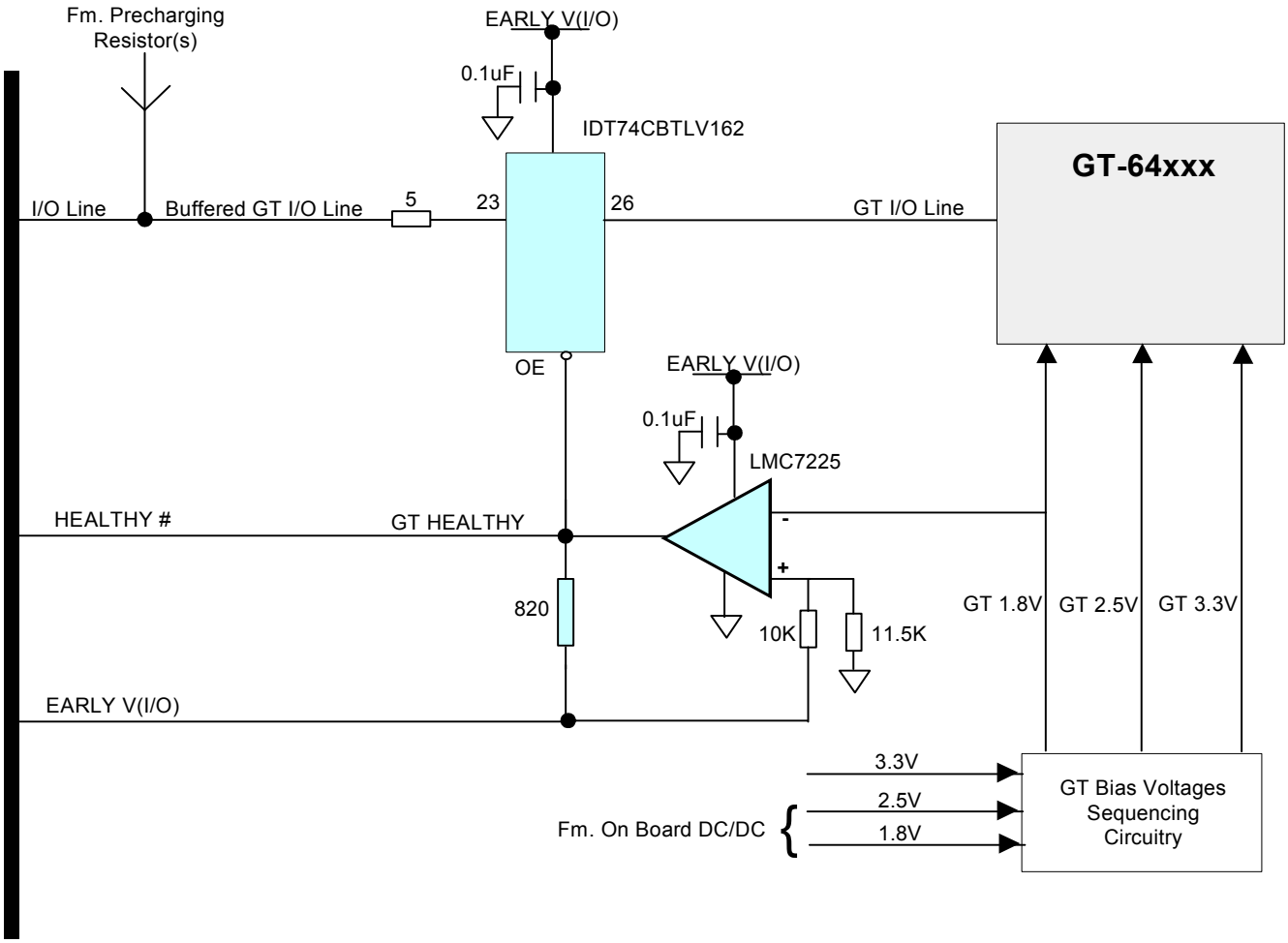
Figure 2 illustrates an example of a possible implementation of the additional I/O buffering, using an IDT 74CBTLV16245 16-bit wide bus switch. The "original" GT-64xxx I/O signal line (only one is brought as an example) is routed through the buffer/switch -via its pins 23 and 26, which correspond to one of the 16 switches contained in the IDT device, and a 5 Ohms additional series resistor, to become the GT Buffered I/O line. This buffered I/O line replaces the original GT I/O line, and connects to its peer in the bus together with its corresponding Precharge connection coming from the Precharge circuitry, as required in the *CPCI Hot Swap Specification*.

The additional 5 Ohms series resistor is inserted to comply with the CPCI Signal Electrical Model requirement to have a 10 Ohms DC "stub resistance". Since the IDT buffer exhibits a typical 5 Ohms resistance at its ON state, the remaining 5 Ohms are complemented by these series resistors.

The OE of the switch is controlled by the output of a voltage comparator (in the example; the NSC low power, tiny SOT23-5 package LMC7225 Open Drain output type is used) and the 820 Ohms pull up resistor. When the board is initially inserted, the first voltage to ramp up, the EARLY V(I/O) which is 3.3V in our example, forces the comparator's output into high impedance, and holds the switch OE pin at its biasing voltage (EARLY V(I/O) via the 820 Ohm pull up resistor. This effectively puts the switches in their disconnect position, and prevents the possibly erratic GT I/O signals from disrupting their corresponding peers in the system's backplane.

The 1.8V core bias follows and ramps up after the 3.3V. It eventually reaches the value established by the 10K and 11.5K 1% precision resistors voltage divider. When this value is reached (~1.8V), the comparator goes into its output low state, and puts the switches into their ON, connect, state. The output of the comparator, GT HEALTHY, can in fact also be used as the enable for the board's HEALTHY# signal as required by the specifcation.

Figure 2: Implementing Hot Swap Using IDT74CBTLV16245 Devices



The switches remain in their ON, connect, state as long as the board maintains its 3.3V and 1.8V biases at their stable values, i.e., as long as the board stays in its inserted position.

When the board removal begins, the first bias voltage to ramp down is the core's 1.8V. This causes the comparator output to revert into its high impedance state, thus deasserting the GT HEALTHY signal. This puts the switches back into their disconnect position, and prevents the possible undesired interference between the GT I/O lines and their corresponding ones in the system's backplane.

Summary

This note is aimed to highlight the basic problems associated with the Hot Swap procedure of boards containing Marvell Integrated Circuits, especially focusing on the issue of preventing the board's I/O signals and their system bus peers from interfering with each other in the absence of adequate bias to the GT device.

The recommended solution is the addition of signal isolation buffers, or "Bus Switches", as they are commonly called in the industry, especially intended to perform in PCI/CPCI Hot Swapping circuitry.

The incorporation of the Bus Switch devices presents some new requirements to the board's designer, but these can be easily met with relatively simple and readily available components.

As a final suggestion, the designer is encouraged to always refer to the *CompactPCI® Hot Swap Specification* in order to verify the validity of the design and/or any later introduced modifications.

Marvell
700 First Avenue
Sunnyvale, CA 94089
Phone: (408) 222 2500
Sales Fax: (408) 752 9029
Email commsales@marvell.com