1. Introduction

Marvell Technology's Discovery devices are high end devices that are capable of achieving up to 133Mhz. Operating at these frequencies leaves little room for timing margins and requires careful design for high signal integrity. When interfacing SDRAM DIMMs the problem is even more acute as the clock to out of an SDRAM DIMM is 5.4nS while the clock cycle time is 7.5nS. The GT-642xx and GT-642xxA (hereafter referred to as "GT") provides clocking options that should enable achieving these high frequencies.

This document provides details on these clocking schemes. An example of physical connection is provided in appendix A and a theoretical calculation example is given in appendix B.

2. Clocking options

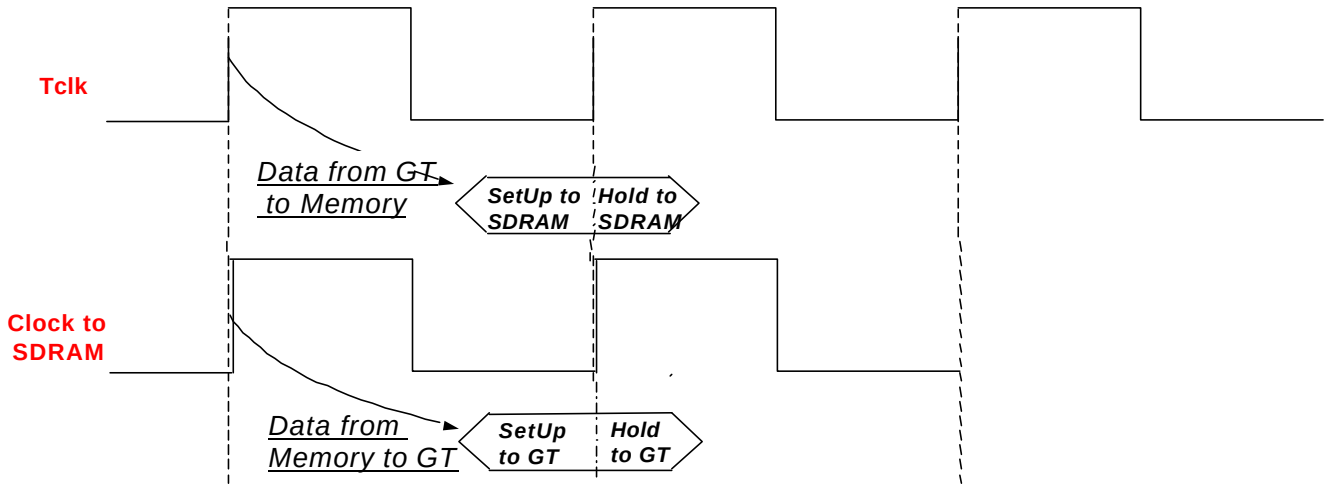
The GT-642xx has two options for connecting the SDRAM interface: Tclk and SDClkOut. The GT-642xxA added another option that is called SDClkIn

2.1 Tclk

This is the basic mode. In this mode all clocks in the system are "synchronized" i.e., no skew between the receiving side or transmitting side of the GT and the SDRAM clocks.

The SDClkOut pin of the GT is left unused.

Figure 1: Clock relations when working in Tclk mode



2.2 SDClkOut

In this mode The GT supplies the clock signal to the SDRAM. This way we can generate better clock to out time from the GT. In other words, one can say that the cycle time for the write path is larger than the clock cycle time.

Note

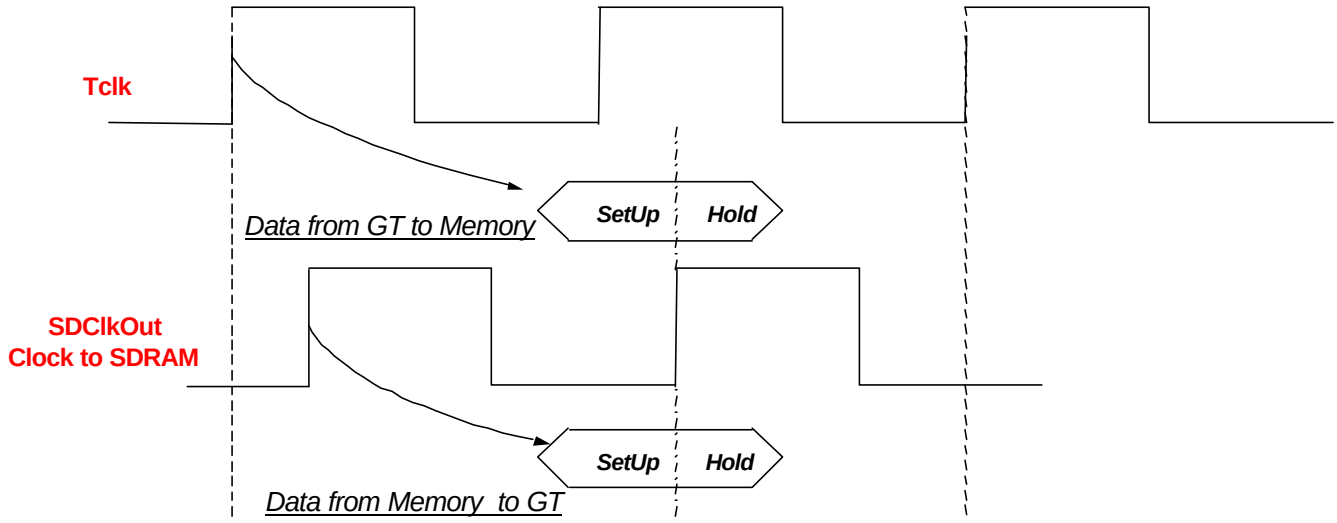
Marvell does NOT recommend working in this mode. For the GT-642xx, The highest frequency available is 100Mhz. Tclk mode is sufficient and should be selected. For the GT-642xxA, SDClkIn should be the preferred method of clocking. See section 2.3 for more details.

Working in this mode adds on sampling stage in the read direction thus adding one clock cycle to the latency of a read from the SDRAM.

This resolves issues with driving the heavier loads such as the control signals (RAS, CAS, DWR, etc.) and address lines.

As shown in the timing waveform below, this mode does not help in the returning data path. The read path cycle time is equal to the Clock cycle time. The data is sampled in the GT with the SDClkOut signal and is then sampled again with Tclk.

Figure 2: Timing when using SDClkOut

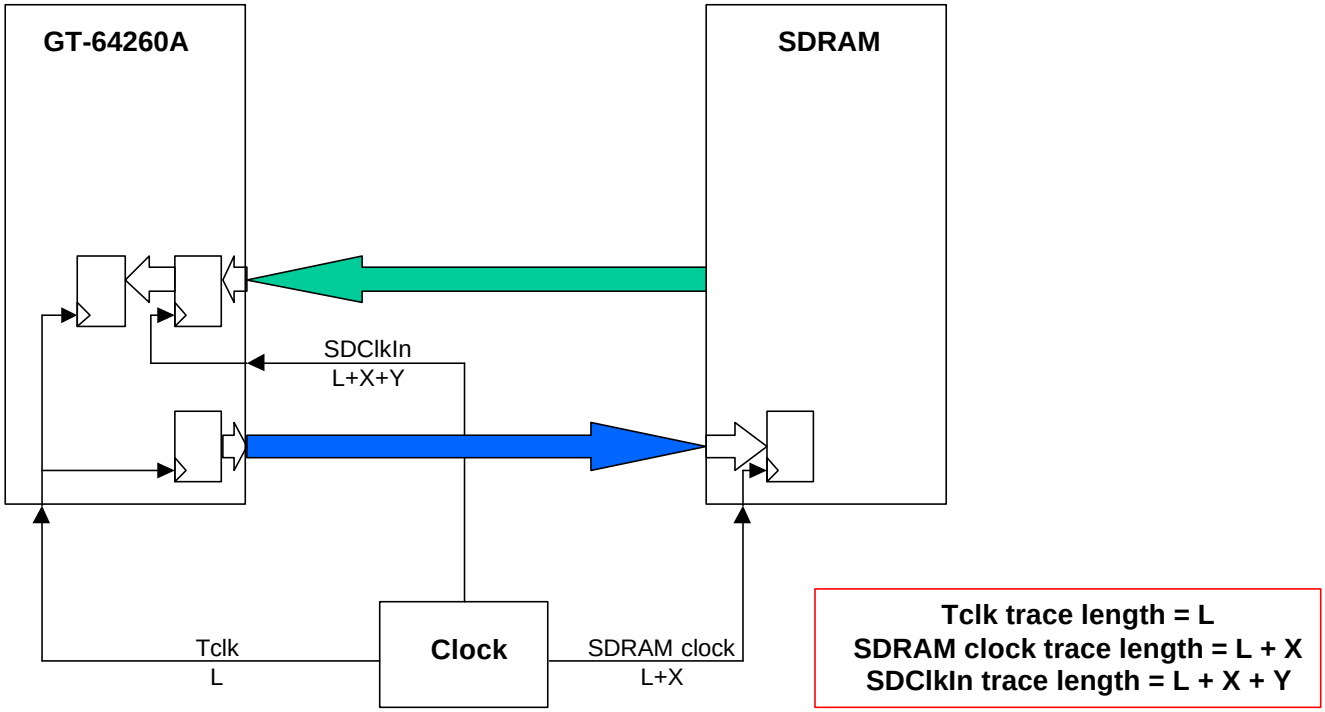


2.3 SDClkIn

This mode exists only in the GT-642xxA. The assumption behind this implementation is that the AC timing of the read path allows for no margin, but the GT can compensate for the high output delay of the SDRAM inside the chip, i.e. the AC timing of a path inside the chip is much faster than AC timings on the PCB.

The idea is that a skewed clock will be supplied externally into the SDClkOut ball of the GT. The GT will be configured to use this ball as an input by sampling AD23 high at reset.

Figure 3: Block diagram of SDRAM interface



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2.3.1 Timing

The following figure shows the relations between the clocks of the system. In this method both path directions can gain some additional margin

2.3.1.1 GT to SDRAM

For the case of signals driven by the GT to the SDRAM, signals are generated from the GT with Tclk and are sampled at the SDRAM with the SDRAM clock. The SDRAM clock can be skewed from Tclk using longer trace length. This way, the cycle time of the write path can be longer than the clock cycle time. The limit for the amount of skew allowed is the hold time requirements of the SDRAM.

2.3.1.2 SDRAM to GT

For the case of signals driven by the SDRAM to the GT, signals are generated from the SDRAM with the SDRAM clock and are sampled at the Gt with the SDClkIn clock. The SDClkIn clock can be skewed from the SDRAM clock using longer trace length. This way, the cycle time of the read path can be longer than the clock cycle time. Again, the limit on the max skew allowed is the GT hold time and

After the data is sampled with the SDClkIn it is sampled again with Tclk. This means that there is an additional sampling stage resulting in longer latency. At this point, the data is again synchronized to the GT's internal clock

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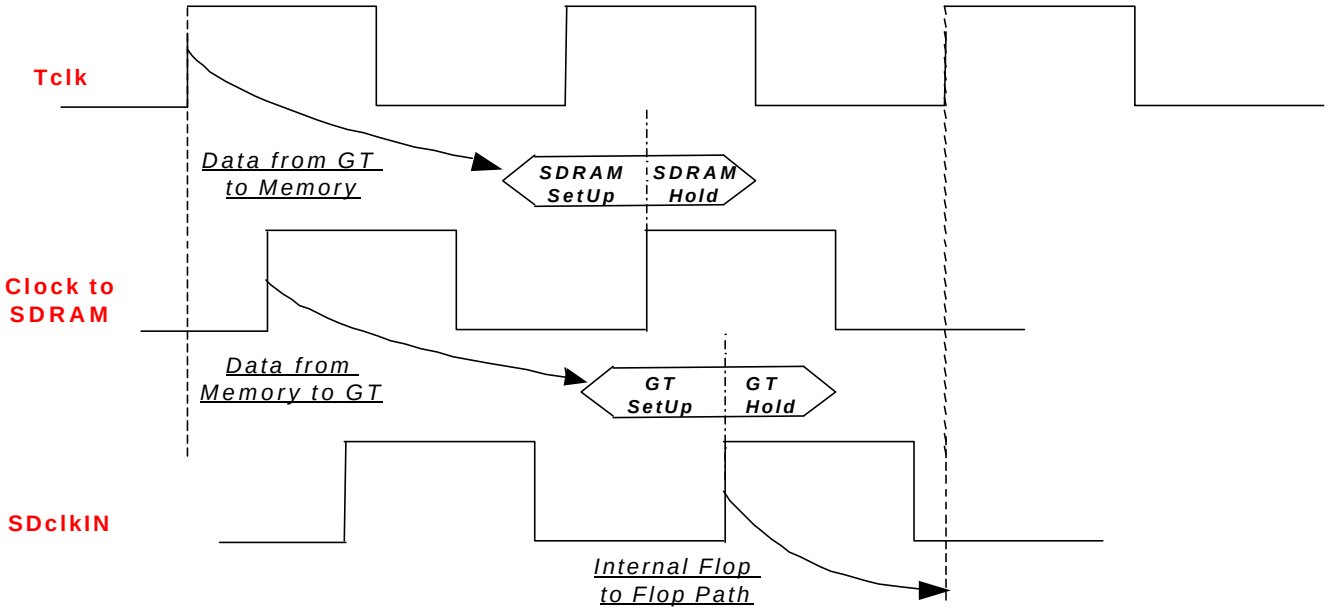
Figure 4: Timing when using SDClkIn



2.3.2 Calculating the correct clock skew

In order to achieve the desired skew between the clocks in figure 3, the equations below should be resolved. See also appendix B for an example of this calculation.

three equations define the clock skews (or clock trace lengths) needed:

2.3.2.1 Internal flop to flop path

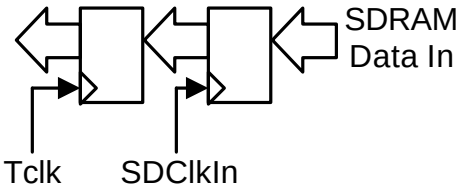
X+Y < Tcycle - 3.85

This equation comes from the fact that the incoming signals (data read) from the SDRAM are sampled first with SDClkIn, and then are sampled again (internally) with Tclk. The time allowed from the first sampling stage (that is clocked with SDClkIn) to the second stage (that is clocked with Tclk) is Cycle time minus 3.85nS (this includes clock-to-out, propagation and setup of this internal path).

X = additional delay to the clock going to the SDRAM compared to Tclk.

Y = additional delay to the clock going to the SDClkIn compared to the clock received by the SDRAM.

Figure 5: Sampling stage with SDClkIn



2.3.2.2 Path from GT to SDRAM

Tcycle > Tco1+Tfly1+Tsu1 - X

Tcycle = cycle time

Tco1 = clock to out time of the GT

Tfly1 = signal flight time + clock skew + clock jitter

Tsu1 = Setup time of the SDRAM

This equation reflects the requirements on signals going from the GT to the SDRAM (control, address, write data, ECC, etc.). This calculation needs to be repeated on the different types of signals as they have different timing (depending on AC specification of the device, trace routing, etc.). The largest sum of Tco1+Tfly1+Tsu1 is the number that should be used.

2.3.2.3 Path from SDRAM to GT

Tcycle > Tco2+Tfly2+Tsu2 - Y

Tco2 = clock to out time of the SDRAM

Tfly2 = signal flight time + clock skew + clock jitter

Tsu2 = Setup time of the GT

This equation reflects the requirements on signals going from the SDRAM to the GT (read data).

2.3.2.4 Verifying Hold Time Requirements

Once the above equations are solved and X and Y values are found, the result needs to be verified against Hold Time requirements. The following equations need to be satisfied:

Thold1+X < Tco3+Tfly3

Thold1 = Hold time of the SDRAM

Tco3 = Minimal clock to out time of the GT

Tfly3 = signal flight time - clock skew - clock jitter

Thold2+Y < Tco4+Tfly4

Thold2 = Hold time of the GT

Tco4 = Minimal clock to out time of the SDRAM

Tfly4 = signal flight time - clock skew - clock jitter

3. Implementation

The following diagram illustrates the implementation of the SDRAM clocking schemes in the GT-642xxA

The following points can be noticed:

SDClkOut/In - this ball can be configured as output (SDClkOut) or input (SDClkIn). The decision is made by the value sampled at reset on pin AD23. Sampling this pin as logical ’1’ configures the GT to drive SDClkOut by enabling the output driver. Sampling this ball as logical ’0’ configures the GT to receive the SDClkIn clock.

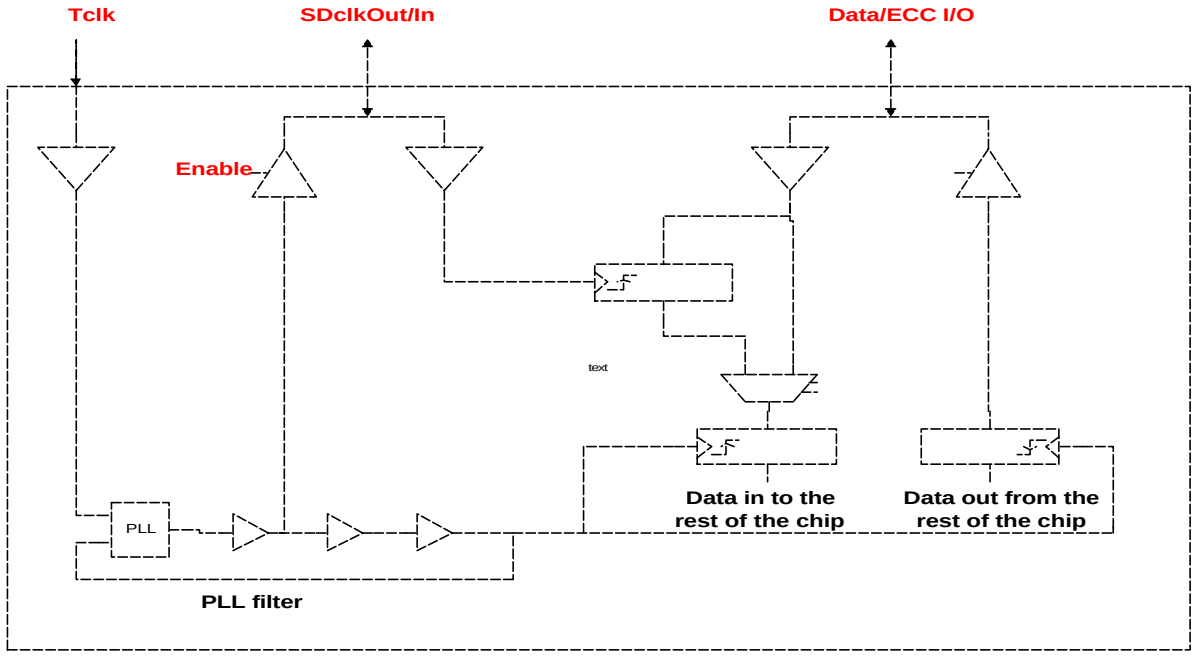
Added sampling stage - On the incoming path there is an additional sampling stage. This sampling stage receives it’s clock from either the SDClkOut or the SDClkIn, depending on the reset configuration as stated above.

Mux after sampling - The mux will select wether or not to utilize the sampling stage to synchronize the data from the SDClkOut or SDClkIn domain to the Tclk domain. When working in the Tclk mode, this synchronization is not needed. Determining the selection of the mux is done through the SDRAM timing parameters register at offset 0x4b4. Setting bit 12 of this register to ’1’ will select the synchronization path. Setting it to ’0’ will bypass the sampling stage.

Note

The default value for this bit is '0' and it must be set to '1' in order to work with SDClkIn

Figure 6: Implementation of SDRAM clocking in the GT-642xxA



4. Conclusions and recommendations

4.1 GT-642xx

- The GT-642xx has two SDRAM clocking options. As this device's maximum frequency is 100Mhz, working with Tclk should be the preferred method of clocking. This of course should be based timing IBIS simulations to prove that the design allows for this frequency.
- In the GT-642xx, working with SDClkOut will cause a latency increase of 1 clock cycle (one sampling stage added). As noted before, working in this mode is NOT recommended.
- Working with SDClkOut does not help in the read direction, only in the write direction.

4.2 GT-642xxA

- The GT-642xxA has three clocking options. If the system design permits, Tclk clocking method should be the preferred clocking method. For frequencies and designs that don't allow this, SDClkIn method should be used
- SDClkOut method should be avoided in any case when using the GT-642xxA

Appendix A - Implementation on the EV-642x0A

The schematics below are part of the EV-642x0A schematics.

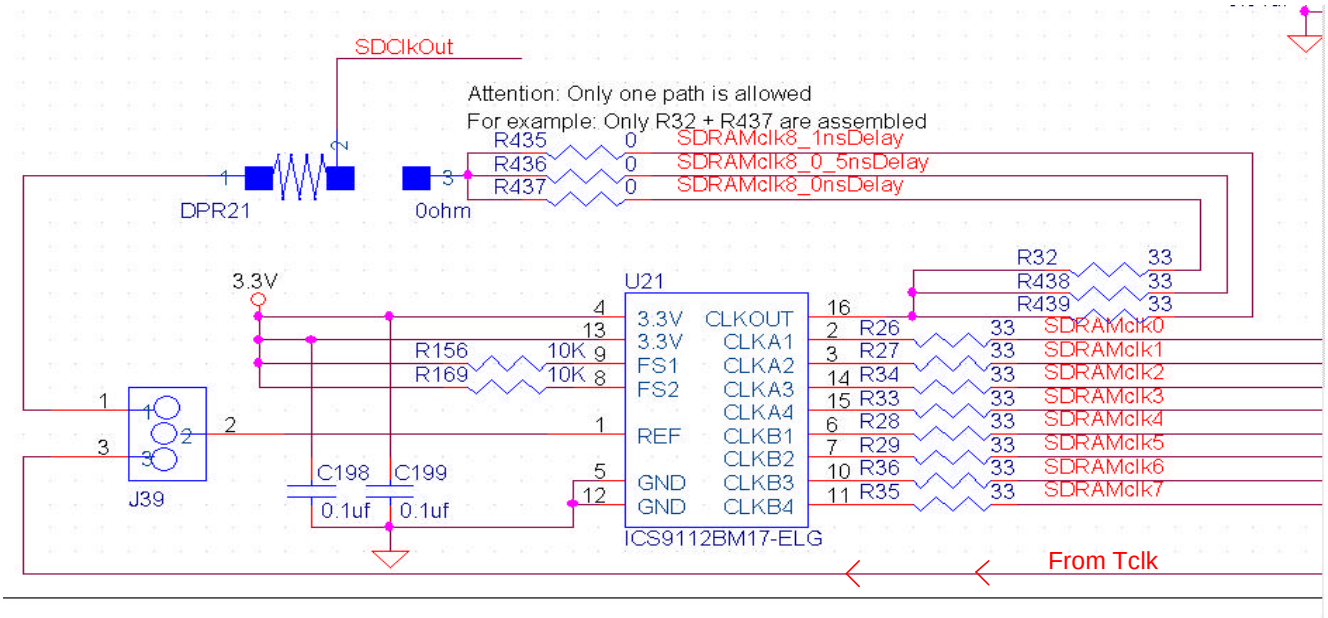
The implementation below allows for one of the three configurations to be chosen and used in the system:

Tclk - connecting J39 between pins 2 and 3 supplies the zero-delay clock buffer with a reference clock from Tclk. The SDRAM clock signals are fed by this buffer.

SDClkOut - Connecting J39 between pins 1 and 2, and assembling the 0 ohm resistor of the DPR21 between 1 and 2 feeds the clock buffer with the SDClkOut signal coming from the GT. In addition AD23 of the GT needs to be sampled high at reset to generate the SDClkOut signal. This delayed clock is then fed to the clock buffer that generates the SDRAM clocks.

SDClkIn - In this case, DPR21 is assembled between pads 2 and 3. J39 is connected between 2 and 3 feeding the clock buffer with Tclk. SDClkIn is fed back to the GT through one of the three resistor pairs (R32 and R437, R438 and R436, R439 and R435). Each pair is routed differently on the board resulting in different trace lengths. Assembling one of these three pairs chooses one of three possible trace lengths.

Figure 7: SDRAM clocking implementation in the EV-642x0A



Appendix B

The following is an example of how to calculate the trace lengths:

As stated before, the set of equations that needs to be solved is:

1. X+Y < Tcycle - 3.85
2. Tcycle > Tco1+Tfly1+Tsu1 - X
3. Tcycle > Tco2+Tfly2+Tsu2 - Y

The parameters in the equations:

Tcycle = 7.5nS (@ 133Mhz)

Tco1 = clock to out time of the GT. The GT's largest number is 4.8nS for ECC.

Tfly1 = signal flight time + clock skew + clock jitter. In our example we'll assume 2nS.

Tsu1 = Setup time of the SDRAM. "-7" SDRAM DIMMs give a number of 1.5nS.

Tco2 = clock to out time of the SDRAM is usually 5.4nS.

Tfly2 = signal flight time + clock skew + clock jitter. again we'll assume 2nS

Tsu2 = Setup time of the GT (1.8nS)

We get:

From Equation 2: 7.5 > 4.8+2+1.5-X. Solving this equation gives X > 0.8nS

From Equation 3: 7.5 > 5.4+2+1.8-Y. Solving this equation gives Y > 1.7nS

For the Hold requirements:

1. Thold1+X < Tco3+Tfly3. From this we get X < 1.1nS
2. Thold2+Y < Tco4+Tfly4. From this we get Y < 3.4nS

Thold1 = Hold time of the SDRAM = 0.8nS

Tco3 = Minimal clock to out time of the GT = 1.1nS

Tfly3 = signal flight time - clock skew - clock jitter = 0.8nS

Thold2 = Hold time of the GT = 0.4nS

Tco4 = Minimal clock to out time of the SDRAM = 3nS

Tfly4 = signal flight time - clock skew - clock jitter = 0.8nS

So we can define X=1nS; Y=2nS

assuming 1" = 180pS delay the result is

X=5.5" Y=11"