EV-642xx and EV-642xxA Development Platform Differences
Discovery System Controllers

Table 1

FEATURE	EV-64260	EV-64260A
SDClkIn / SDCclkOut		• Circuitry was added to drive an input clock to the Discovery system controller's SDClkOut pin.
DIMM registered / buffered mode select		• Pullup added on the RegE input signal of the SDRAM DIMM
JTAG connector Test Reset Signal - TRST	• None	• Included
SMP support simplified -- replaced resistor with jumper	• RNC7	• J61
BG0 / BG1 Swap Supported	• N/A	• Yes
SMP Systems: PCI interrupt supported on second CPU	• No	• Yes
Tclk	• 100Mhz	• 133Mhz. Note: MPC750/7400 and IBM750L platforms are shipped with a 100Mhz oscillator as they do not support 133Mhz.
CPU internal voltage supply-- auto-select supported	• Yes	• Yes; except for the EV-64240A-RM7000A. See Backplane Users Manual.
PCI Arbiter	• PCI arbiter can be implemented using an external PLD or using the on-chip PCI arbiter.	• PCI arbiter can only be implemented using the on-chip PCI arbiter. The external PLD is not assembled.

* **NOTES** applicable to the EV-642xxA Development Platform:

1) The PLD is automatically configured for I2C boot. The main PLD (U8) of the EV-642xxA detects that the system is booting with I2C sequence by sampling the "I2C boot enable" reset strapping of the Discovery system controller. If the I2C boot is enabled, the PLD will release the reset to the CPU only after the INIT ACT signal is received from the Discovery, indicating that the reset sequence has finished.

2) The CPU's VccIO jumpers, J21-23, were moved to a different location for mechanical reasons.

3) MPP 5 is connected to the main system reset to enable hard reset through software – the software can write to an MPP that will in turn generate a signal to the reset circuitry to generate a system reset.

4) The optional PCI test point Mictor footprints were removed from the EV-642xxA board.

5) The Discovery Rev A device made some changes to the reset strapping options. These new options are supported in the EV-642xxA board. See data sheet for details.

Discovery Revision A Development Platform Operating Speeds

Development Platform	Discovery Core	Bus	Memory I/f
• EV-64240A-RM7000A	133 MHz	SysAD - 133 MHz	133 MHz
• EV-64260A-MPC750	100 MHz	60x - 100 MHz	133 MHz
• EV-64260A-IBM750L	100 MHz	60x - 100 MHz	133 MHz
• EV-64260A-IBM750CXe	133 MHz	60x - 133 MHz	133 MHz
• EV-64260A-MPC7400	100 MHz	60x / MPX - 100 MHz	133 MHz
• EV-64260A-MPC7410	133 MHz	60x / MPX - 133 MHz	133 MHz
• EV-64260A-MPC7450	125 MHz	60x / MPX - 125 MHz	125 MHz
• EV-64260A-2XMPC7450	125 MHz	60x / MPX - 125 MHz	125 MHz