

Block Diagram:
Available in a separate document

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Rev Number	Remarks
1.0	

These schematic serves Galileo's GT64240A and GT64260A.
The difference is in the CPU interface, please note:
On the CPU's interface signals the name on the left is for PPC (GT64260A) and the one on the right is for MIPS (GT64240A).
For example: DL0\SysAD31.

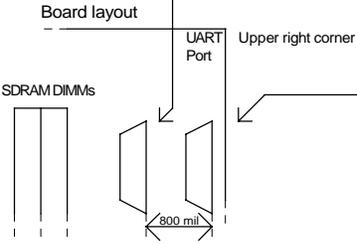
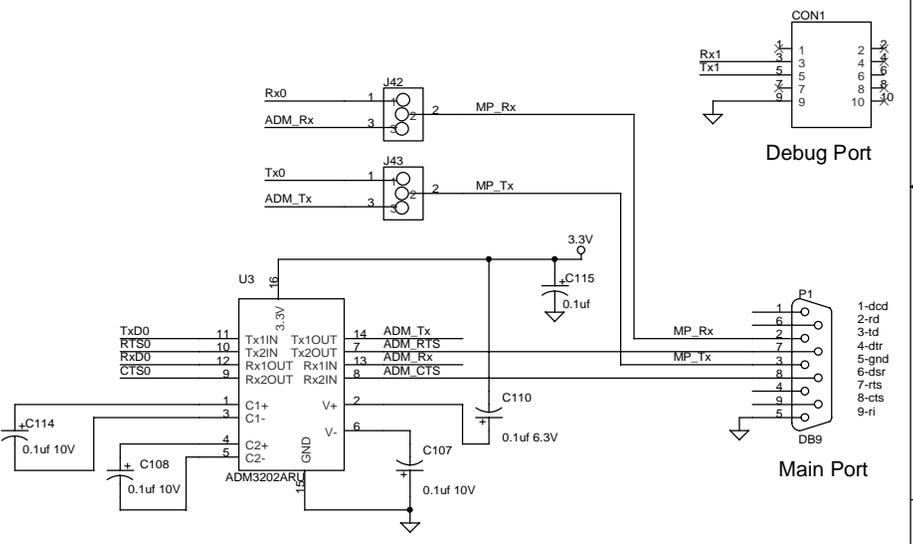
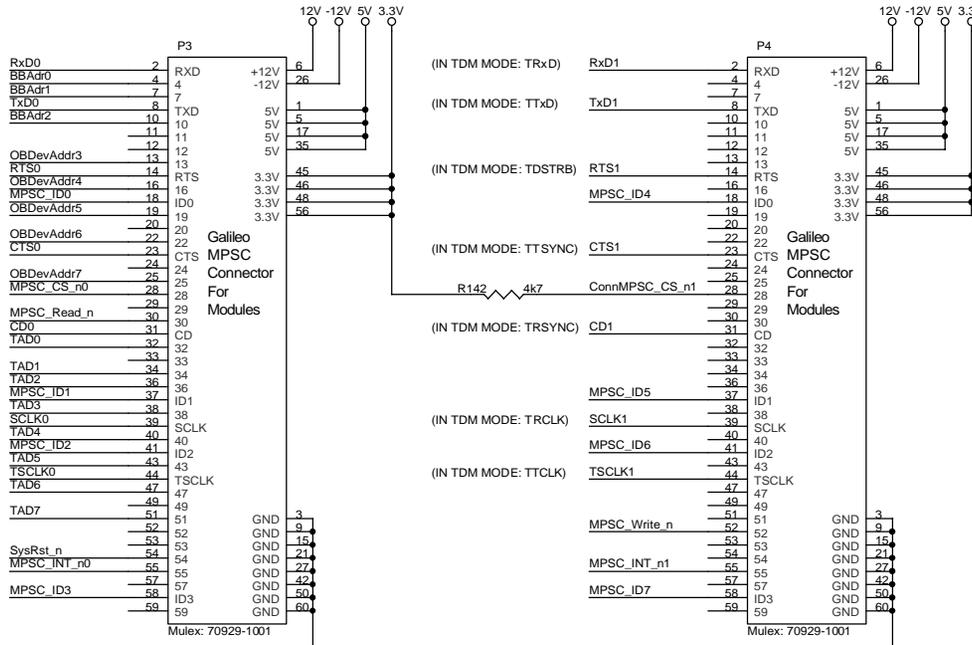
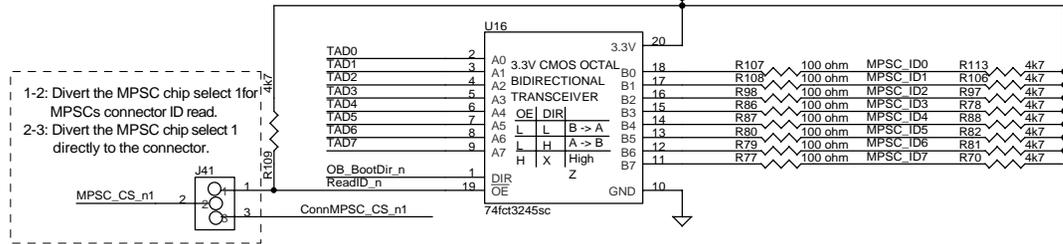
GALILEO TECHNOLOGY		
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CTS[1..0]
 CD[1..0]
 SCLK[1..0]
 TSCLK[1..0]

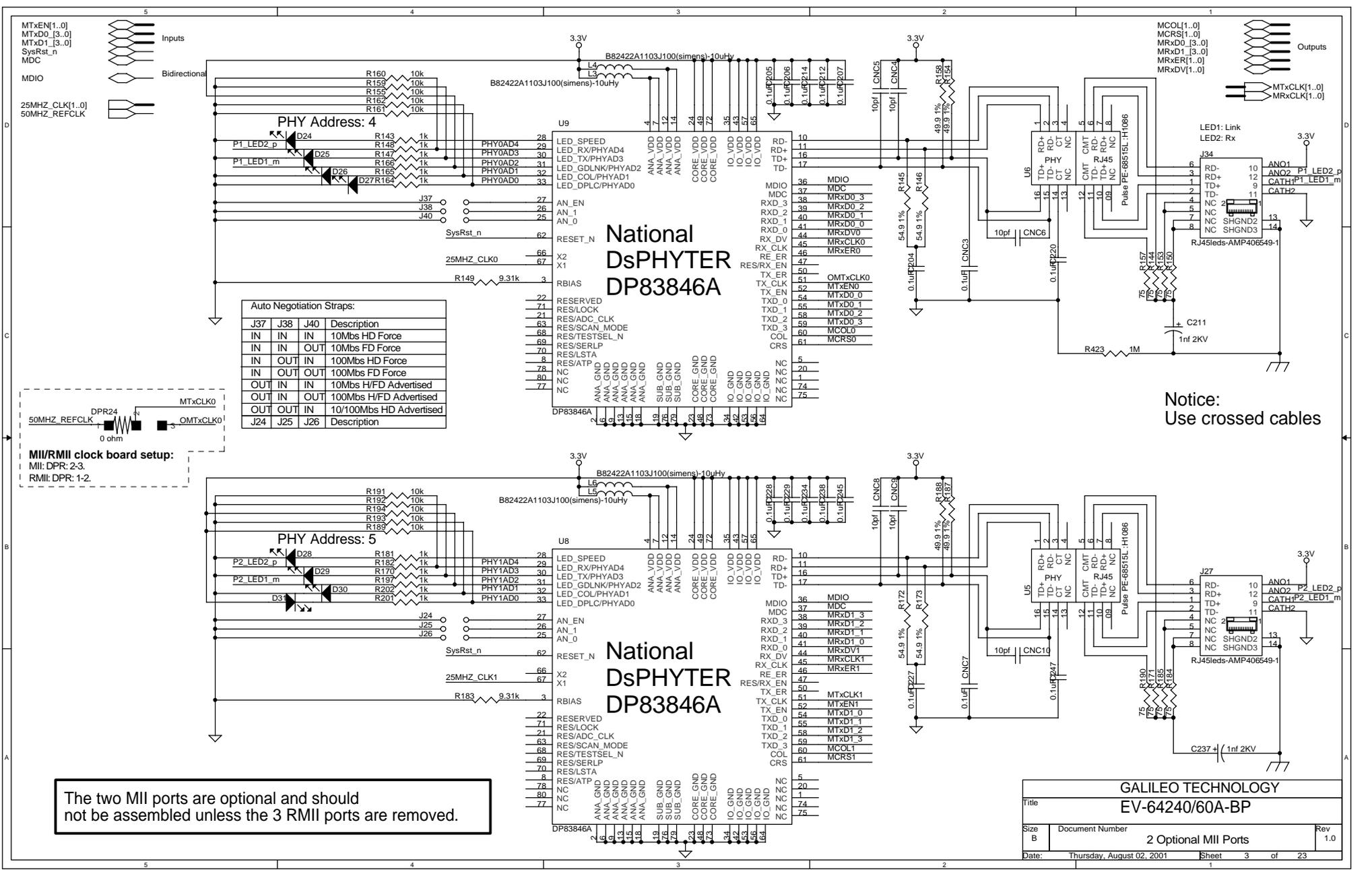
TxD[1..0]
 Tx[1..0]
 RTS[1..0]

MPSC_CS_n[1..0]
 MPSC_Read_n
 MPSC_Write_n
 BBAdr[2..0]
 OBDevAddr[7..3]
 SysRst_n
 OB_BootDir_n
 TAD[7..0]

RxD[1..0]
 Rx[1..0]
 MPSC_INT_n[1..0]



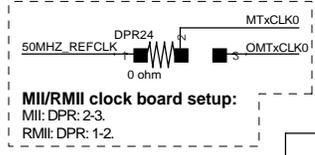
GALILEO TECHNOLOGY		
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	2 MPSC Connectors + UART	1.0
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National DsPHYTER DP83846A

Auto Negotiation Straps:

J37	J38	J40	Description
IN	IN	IN	10Mbps HD Force
IN	IN	OUT	10Mbps FD Force
IN	OUT	IN	100Mbps HD Force
IN	OUT	OUT	100Mbps FD Force
OUT	IN	IN	10Mbps H/FD Advertised
OUT	IN	OUT	100Mbps H/FD Advertised
OUT	OUT	IN	10/100Mbps HD Advertised
J24	J25	J26	Description



The two MII ports are optional and should not be assembled unless the 3 RMII ports are removed.

Notice:
Use crossed cables

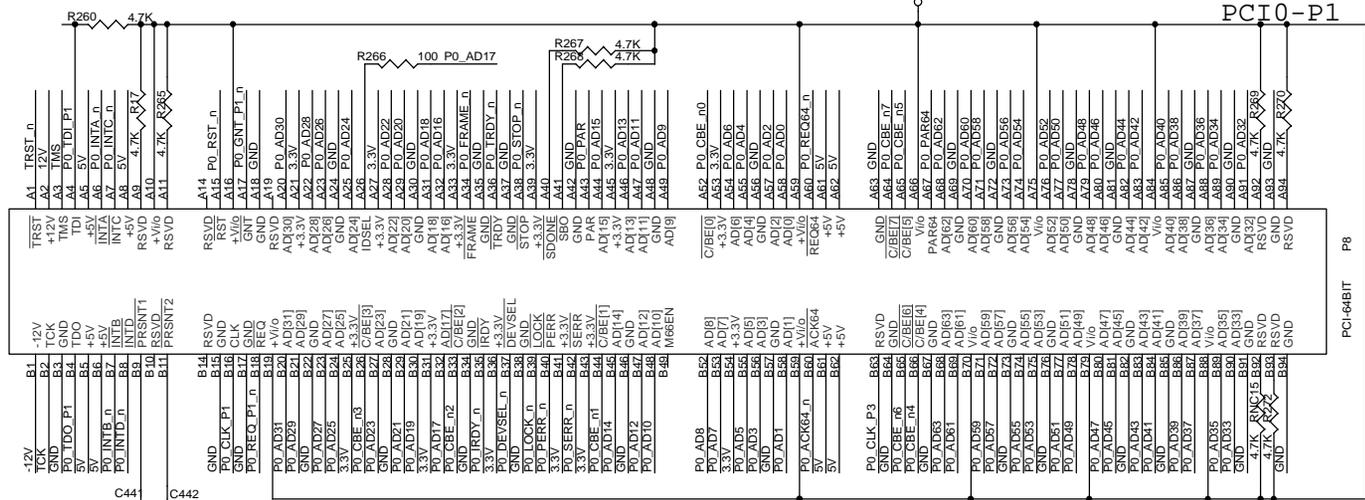
GALILEO TECHNOLOGY
EV-64240/60A-BP

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	2 Optional MII Ports	1.0
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P0_CBE_n[7..0]
P0_AD[63..0]
TMS
TRST_n
P0_INTA_n
P0_INTB_n
P0_INTC_n
P0_INTD_n
P0_FRAME_n
P0_TRDY_n
P0_IRDY_n
P0_STOP_n
P0_PAR
P0_DEVSEL_n
P0_PERR_n
P0_SERR_n
P0_ACK64_n
P0_PAR64_n
P0_REQ64_n

P0_GNT_P1_n
P0_GNT_P2_n
P0_CLK_P[4..1]
P0_RST_n
CPU_TDO

P0_AD32 R359 4.7K
P0_AD33 R383 4.7K
P0_AD34 R354 4.7K
P0_AD35 R384 4.7K
P0_AD36 R387 4.7K
P0_AD37 R388 4.7K
P0_AD38 R356 4.7K
P0_AD39 R382 4.7K
P0_AD40 R8 4.7K
P0_AD41 R38 4.7K
P0_AD42 R389 4.7K
P0_AD43 R380 4.7K
P0_AD44 R354 4.7K
P0_AD45 R379 4.7K
P0_AD46 R353 4.7K
P0_AD47 R378 4.7K
P0_AD48 R357 4.7K
P0_AD49 R37 4.7K
P0_AD50 R35 4.7K
P0_AD51 R376 4.7K
P0_AD52 R35 4.7K
P0_AD53 R37 4.7K
P0_AD54 R348 4.7K
P0_AD55 R374 4.7K
P0_AD56 R348 4.7K
P0_AD57 R374 4.7K
P0_AD58 R347 4.7K
P0_AD59 R372 4.7K
P0_AD60 R346 4.7K
P0_AD61 R37 4.7K
P0_AD62 R346 4.7K
P0_AD63 R370 4.7K
P0_CBE_n4 R369 4.7K
P0_CBE_n5 R344 4.7K
P0_CBE_n6 R368 4.7K
P0_CBE_n7 R344 4.7K
P0_ACK64_n R362 4.7K
P0_PAR64_n R344 4.7K
P0_FRAME_n R338 4.7K
P0_TRDY_n R338 4.7K
P0_IRDY_n R364 4.7K
P0_STOP_n R339 4.7K
P0_LOCK_n R366 4.7K
P0_PERR_n R1 4.7K
P0_SERR_n R2 4.7K
P0_INTA_n R26 4.7K
P0_INTB_n R26 4.7K
P0_INTC_n R26 4.7K
P0_INTD_n R26 4.7K

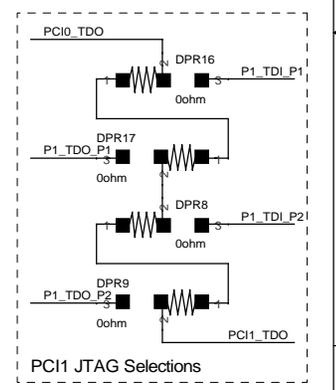
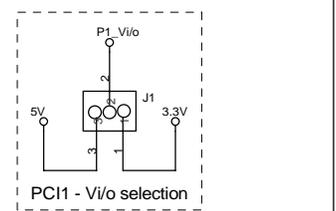
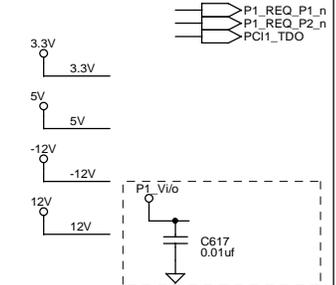
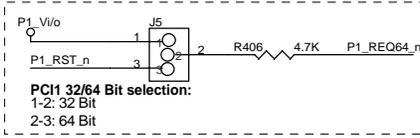
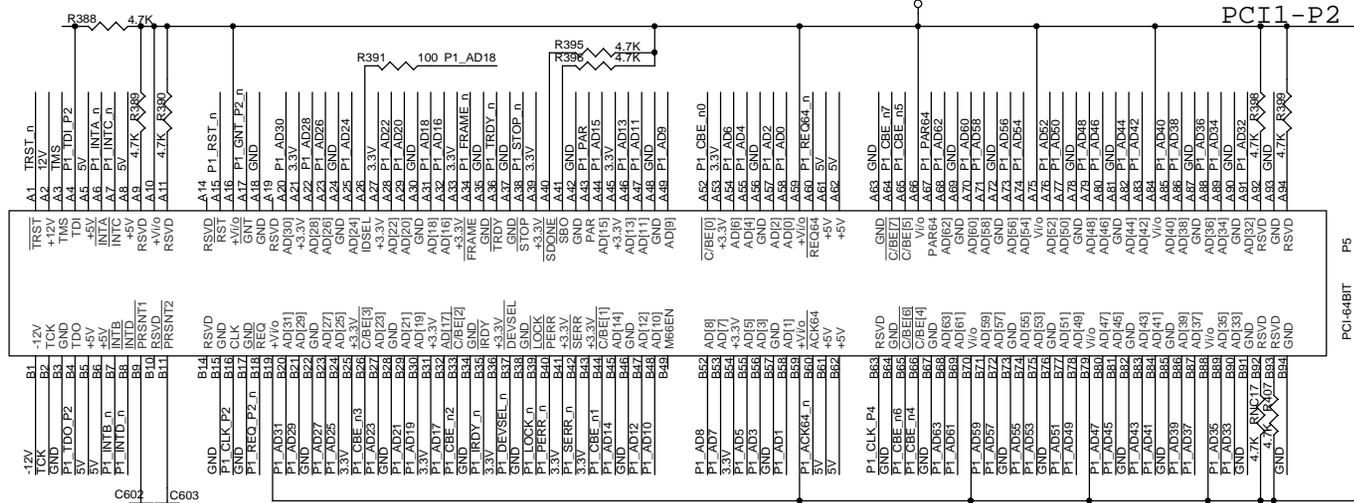
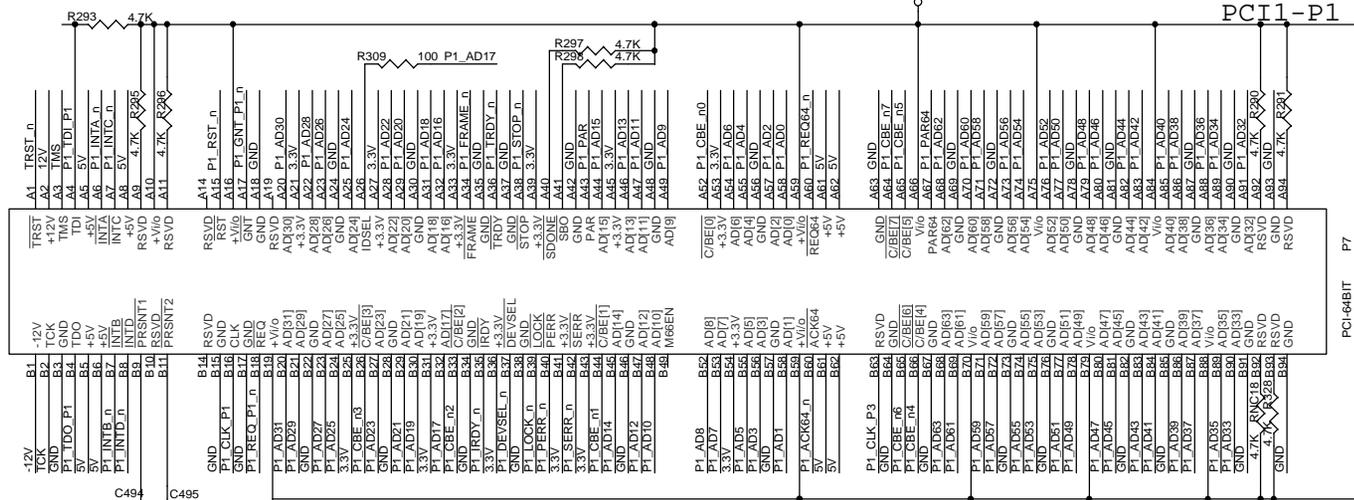


P1_CBE_n[7..0]
P1_AD[63..0]
TMS
TRST_n
P1_INTA_n
P1_INTB_n
P1_INTC_n
P1_INTD_n
P1_FRAME_n
P1_TRDY_n
P1_IRDY_n
P1_STOP_n
P1_PAR
P1_DEVSEL_n
P1_PERR_n
P1_SERR_n
P1_ACK64_n
P1_PAR64_n
P1_REQ64_n

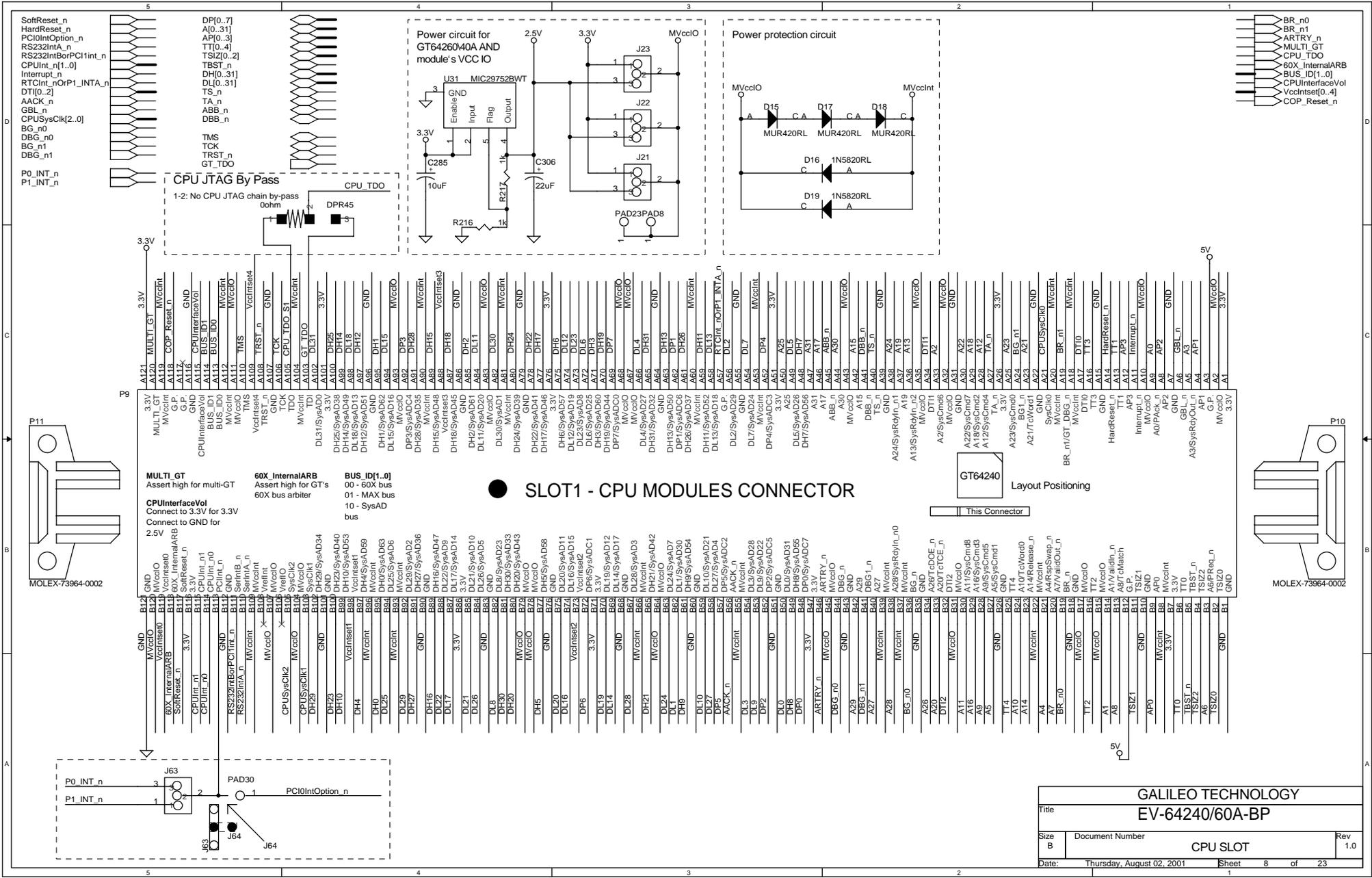
P1_GNT_P1_n
P1_GNT_P2_n
P1_CLK_P[4..1]
P1_RST_n
PCI0_TDO

P1_AD32 R289 4.7K
P1_AD33 R322 4.7K
P1_AD34 R288 4.7K
P1_AD35 R326 4.7K
P1_AD36 R287 4.7K
P1_AD37 R325 4.7K
P1_AD38 R286 4.7K
P1_AD39 R324 4.7K
P1_AD40 R285 4.7K
P1_AD41 R323 4.7K
P1_AD42 R15 4.7K
P1_AD43 R284 4.7K
P1_AD44 R283 4.7K
P1_AD45 R32 4.7K
P1_AD46 R282 4.7K
P1_AD47 R321 4.7K
P1_AD48 R281 4.7K
P1_AD49 R7 4.7K
P1_AD50 R28 4.7K
P1_AD51 R318 4.7K
P1_AD52 R280 4.7K
P1_AD53 R316 4.7K
P1_AD54 R279 4.7K
P1_AD55 R317 4.7K
P1_AD56 R278 4.7K
P1_AD57 R316 4.7K
P1_AD58 R277 4.7K
P1_AD59 R315 4.7K
P1_AD60 R276 4.7K
P1_AD61 R314 4.7K
P1_AD62 R275 4.7K
P1_AD63 R313 4.7K

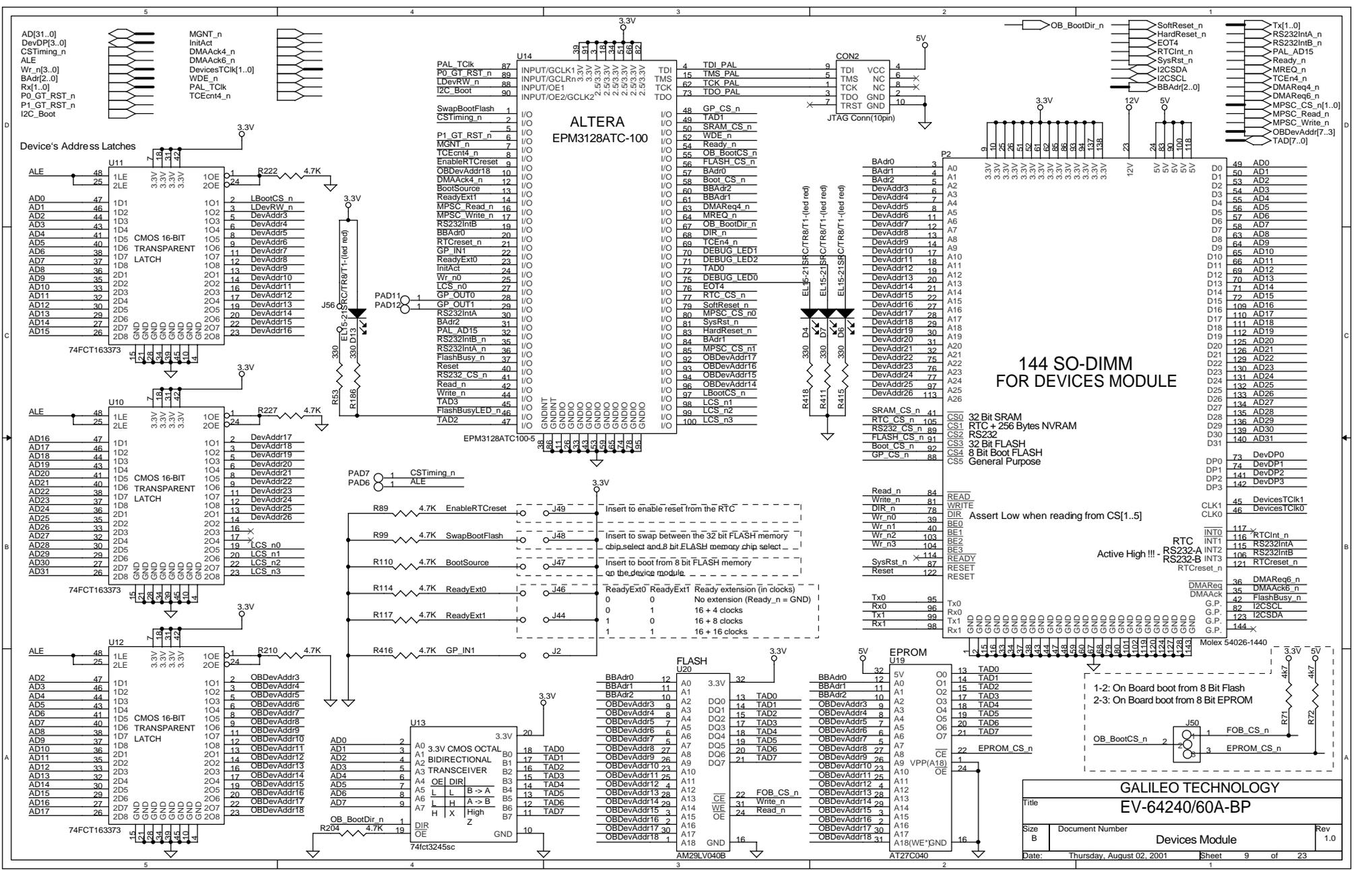
P1_CBE_n4 R312 4.7K
P1_CBE_n5 R274 4.7K
P1_CBE_n6 R31 4.7K
P1_CBE_n7 R273 4.7K
P1_ACK64_n R310 4.7K
P1_PAR64 R39 4.7K
P1_FRAME_n R392 4.7K
P1_TRDY_n R393 4.7K
P1_IRDY_n R40 4.7K
P1_STOP_n R394 4.7K
P1_DEVSEL_n R402 4.7K
P1_LOCK_n R404 4.7K
P1_PERR_n R404 4.7K
P1_SERR_n R40 4.7K
P1_INTA_n R29 4.7K
P1_INTB_n R306 4.7K
P1_INTC_n R308 4.7K
P1_INTD_n R307 4.7K



Title			
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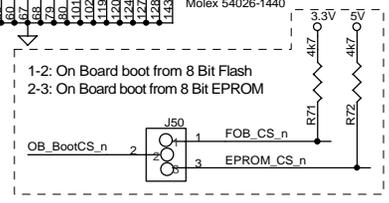


GALILEO TECHNOLOGY EV-64240/60A-BP		
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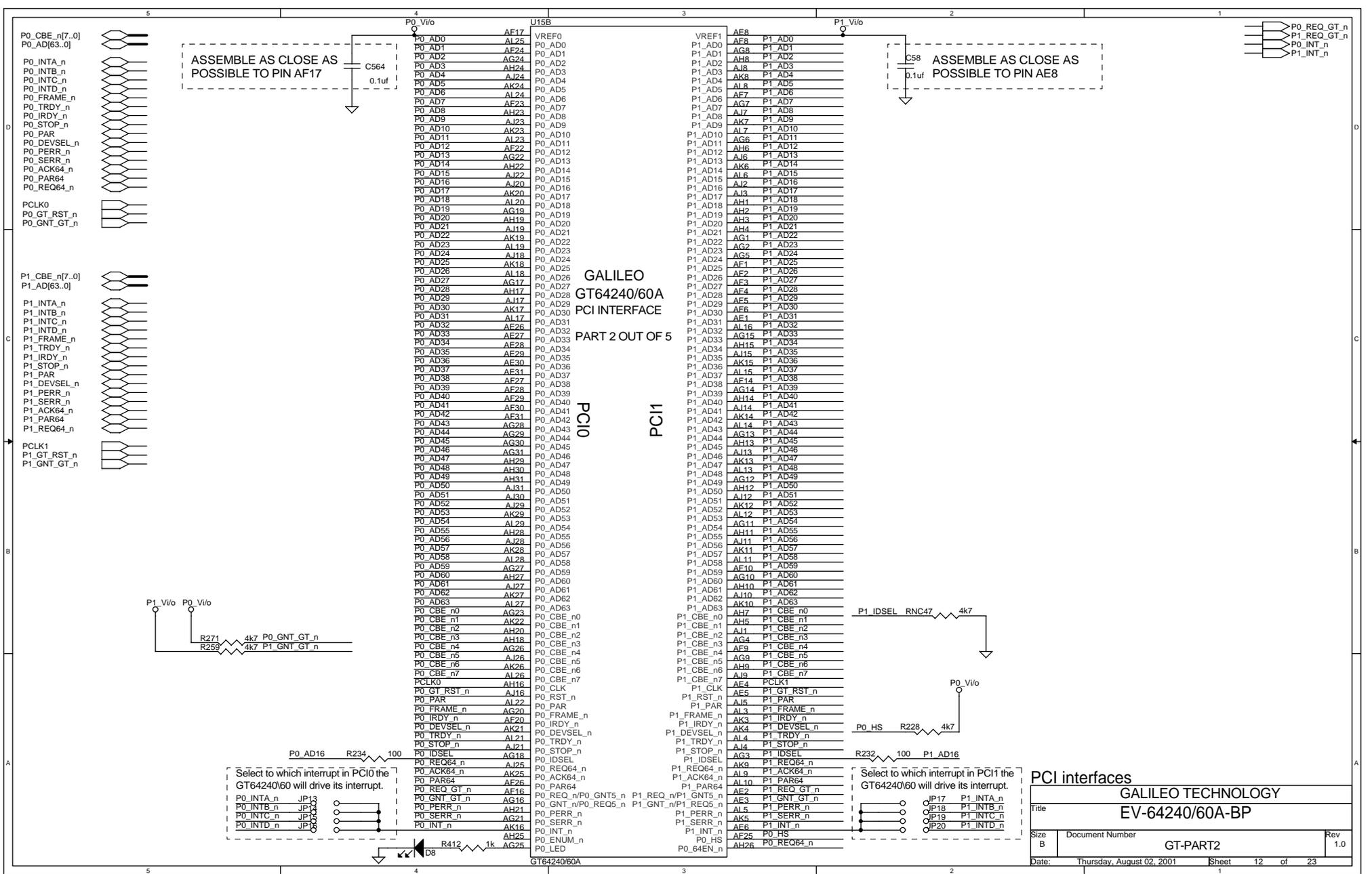


144 SO-DIMM FOR DEVICES MODULE

CS0	32 Bit SRAM	CS1	RTC + 256 Bytes NVRAM
CS2	RS232	CS3	32 Bit FLASH
CS4	8 Bit Boot FLASH	CS5	General Purpose
Read_n	84	READ	
Write_n	81	WRITE	
Dir_n	78	DIR	Assert Low when reading from CS[1..5]
Wr_n0	39	BE0	
Wr_n1	104	BE1	
Wr_n2	103	BE2	
Wr_n3	104	BE3	
SysRst_n	67	READY	Active High !!!
Reset	122	RESET	
Tx0	95	INT0	117
Rx0	96	INT1	116
Tx1	99	INT2	115
Rx1	98	INT3	106
		INT3	121
		DMAReset_n	36
		DMAReq6_n	35
		DMAAck6_n	42
		FlashBusy_n	G.P.
		G.P.	82
		IC2SCS	123
		IC2CSDA	G.P.
		IC2CS	144



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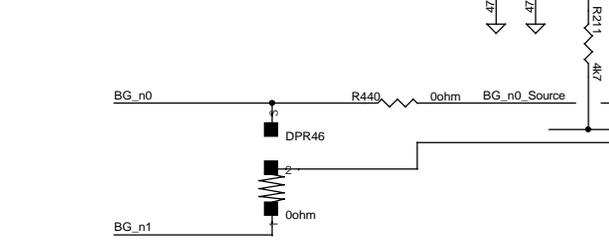


DL[0..31]
DH[0..31]
DP[0..7]
A[0..31]
API[0..3]
TTI[0..4]
TSIZ[0..2]
TBST_n
TS_n
TA_n
ABB_n
DBB_n

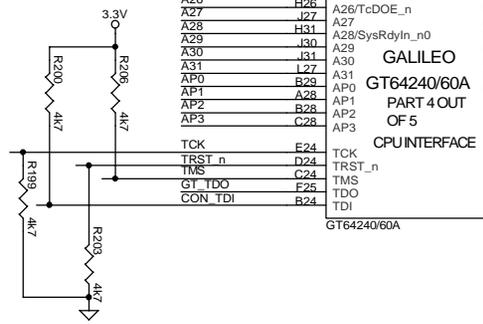
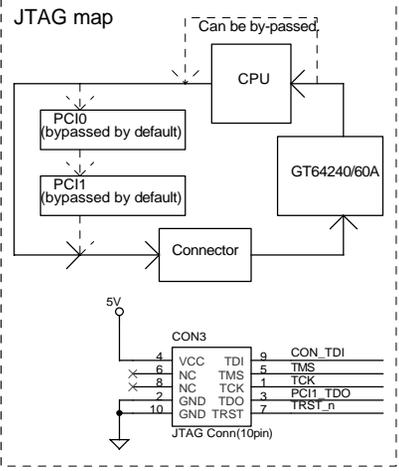
TCIk
GTSysCk
SysRst_n
BR_n0
BR_n1
ARTRY_n

TMS
TCK
TRST_n
PCI1_TDO

DTI[0..2]
AACK_n
GBL_n
Interrupt_n
BG_n0
DBG_n0
BG_n1
DBG_n1
GT_TDO



U15D		M26	
TCIk	F24	DL0/SysAD31	M26
GTSysCk	F25	DL1/SysAD30	R27
SysRst_n	E25	DL2/SysAD29	N28
Interrupt_n	C27	DL3/SysAD28	M27
TS_n	J28	DL4/SysAD27	L27
TBST_n	B25	DL5/SysAD26	L31
TSIZ0	A25	DL6/SysAD25	L30
TSIZ1	C26	DL7/SysAD24	M31
TSIZ2	A27	DL8/SysAD23	V27
TT0	B27	DL9/SysAD22	M30
TT1	C30	DL10/SysAD21	E28
TT2	D26	DL11/SysAD20	V29
TT3	D27	DL12/SysAD19	V27
TT4	E30	DL13/SysAD18	P27
GBL_n	D26	DL14/SysAD17	T30
AACK_n	N28	DL15/SysAD16	AC26
ABB_n	K28	DL16/SysAD15	V26
TA_n	F27	DL16/SysAD15	AA27
DTI0	D28	DL17/SysAD14	AC31
DTI1	G31	DL18/SysAD13	T31
DTI2	G28	DL19/SysAD12	V28
BR_n0	D29	DL20/SysAD11	V30
BG_n0_Source	H28	DL21/SysAD10	AA29
DBG_n0	K26	DL22/SysAD9	U31
BR_n1	D30	DL23/SysAD8	R29
DBG_n1_Source	H29	DL24/SysAD7	AB31
DBG_n1	K27	DL25/SysAD6	V28
DBB_n	J29	DL26/SysAD5	N31
ARTRY_n	K29	DL27/SysAD4	F28
A0	C25	DL28/SysAD3	AB29
A1	C31	DL29/SysAD2	W31
A2	G31	DL30/SysAD1	AD31
A3	A29	DL31/SysAD0	AC27
A4	E26	DH0/SysAD63	AC28
A5	F26	DH1/SysAD62	V31
A6	A26	DH2/SysAD61	U27
A7	D31	DH3/SysAD60	AC29
A8	E28	DH4/SysAD59	V30
A9	F28	DH5/SysAD58	V29
A10	E29	DH6/SysAD57	L29
A11	G26	DH7/SysAD56	I30
A12	F29	DH8/SysAD55	P30
A13	H27	DH9/SysAD54	AD26
A14	E27	DH10/SysAD53	P29
A15	K31	DH11/SysAD52	AC30
A16	F30	DH12/SysAD51	R30
A17	K30	DH13/SysAD50	AD27
A18	F31	DH14/SysAD49	AA30
A19	G30	DH15/SysAD48	AA31
A20	J26	DH16/SysAD47	V31
A21	E28	DH17/SysAD46	AA28
A22	G27	DH18/SysAD45	U28
A23	F31	DH19/SysAD44	W27
A24	H30	DH20/SysAD43	R31
A25	M27	DH21/SysAD42	W28
A26	H26	DH22/SysAD41	AD28
A27	J27	DH23/SysAD40	V29
A28	H31	DH24/SysAD39	AD29
A29	J30	DH25/SysAD38	P31
A30	L27	DH26/SysAD37	AB27
AP0	B29	DH27/SysAD36	AB28
AP1	A28	DH28/SysAD35	AD30
AP2	B28	DH29/SysAD34	V30
AP3	C28	DH30/SysAD33	L26
TCK	F24	DH31/SysAD32	I28
TRST_n	D24	DP0/SysADC7	L28
TMS	C24	DP1/SysADC6	R28
GT_TDO	F25	DP2/SysADC5	M28
CON_TDI	B24	DP3/SysADC4	AB30
		DP4/SysADC3	H29
		DP5/SysADC2	N30
		DP6/SysADC1	L29
		DP7/SysADC0	T29
			DP7

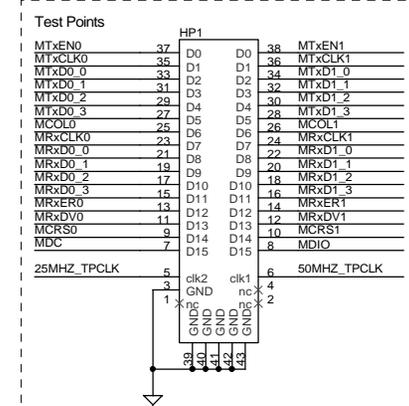
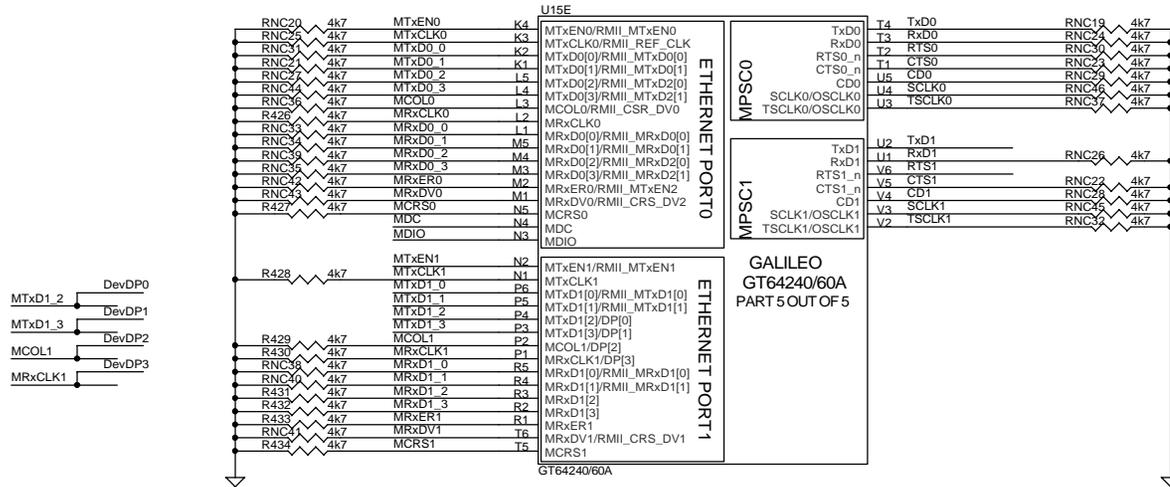


CPU and JTAG interfaces		
GALILEO TECHNOLOGY		
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B	GT-PART4	1.0
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MCOL[1..0]
MCRS[1..0]
MRxD0_[3..0]
MTxCLK[1..0]
MRxCLK[1..0]
MRxER[1..0]
MRxDV[1..0]
50MHZ_TPCLK
25MHZ_TPCLK

MDIO
RxD[1..0]
CTS[1..0]
CD[1..0]
SCLK[1..0]
TSCLK[1..0]
DevDP[3..0]

MTxEN[1..0]
MTxD0_[3..0]
MTxD1_[3..0]
RTS[1..0]
TxD[1..0]
MDC



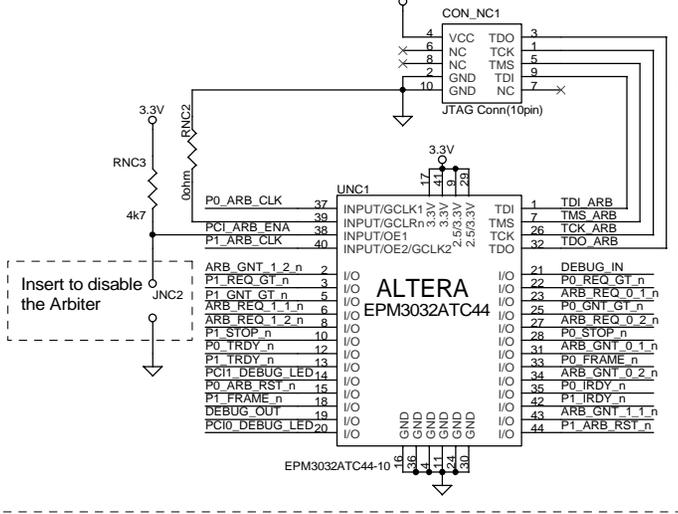
Communication ports interfaces

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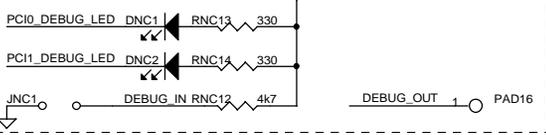
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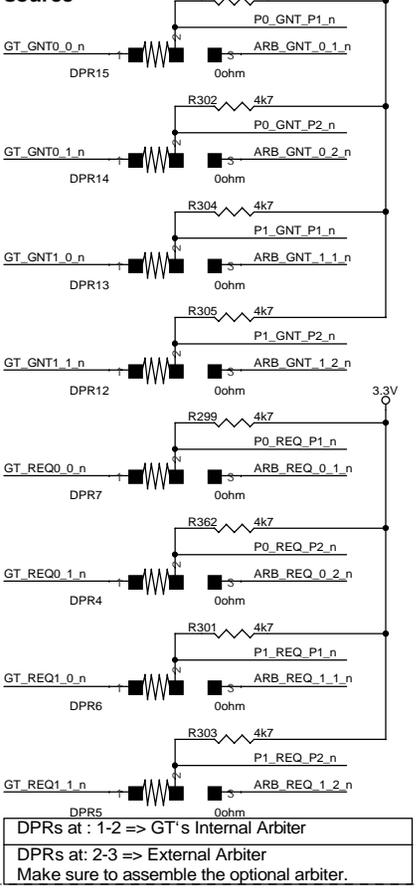
PCI Optional Arbiters



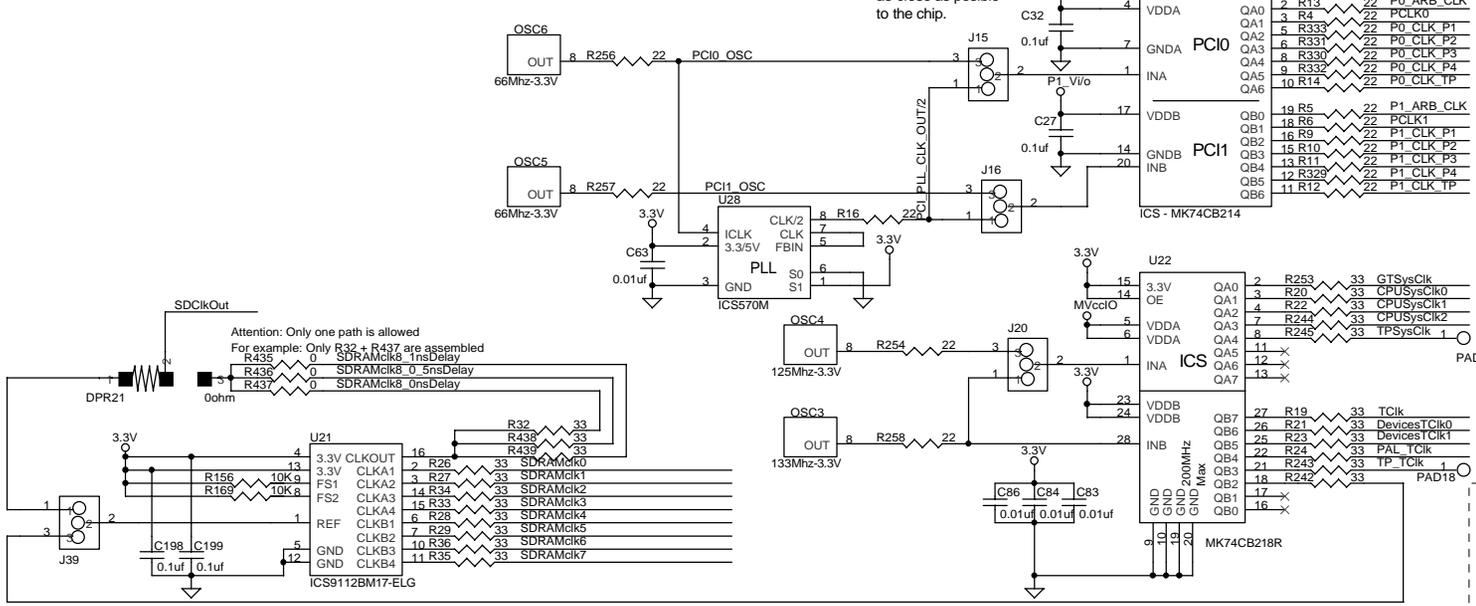
PCI Debug



PCI Arbitration source



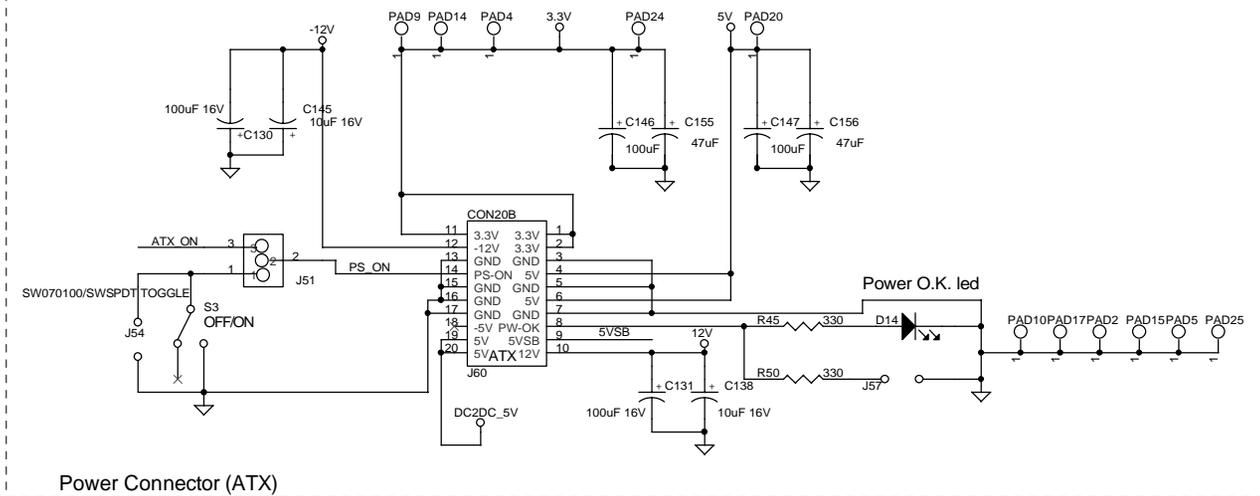
Clocks



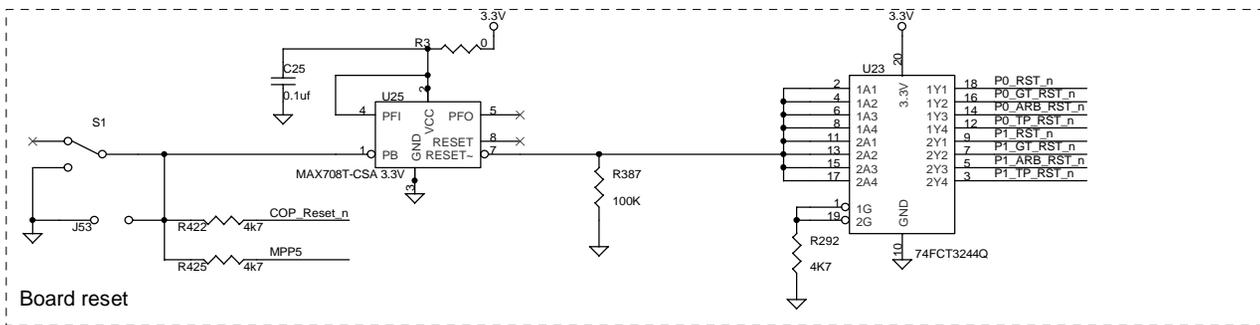
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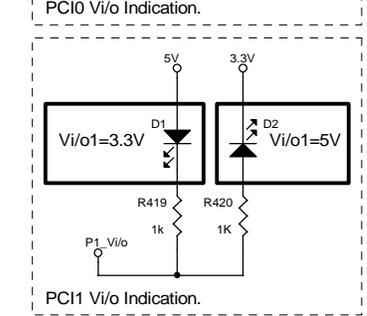
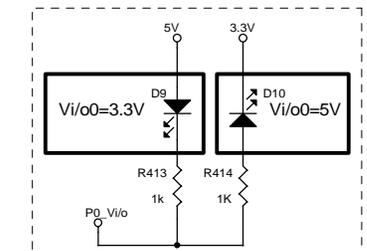
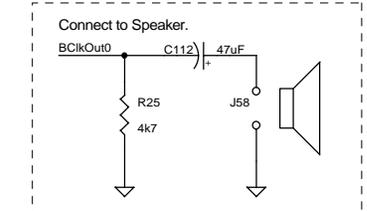
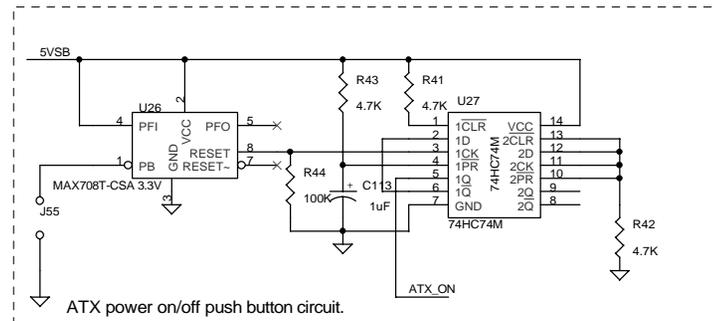
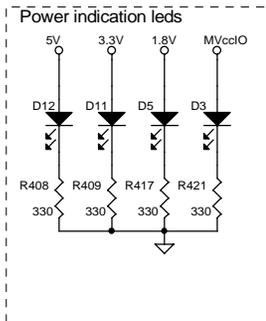
BClkOut0
COP_Reset_n
MPP5



Power Connector (ATX)



Board reset



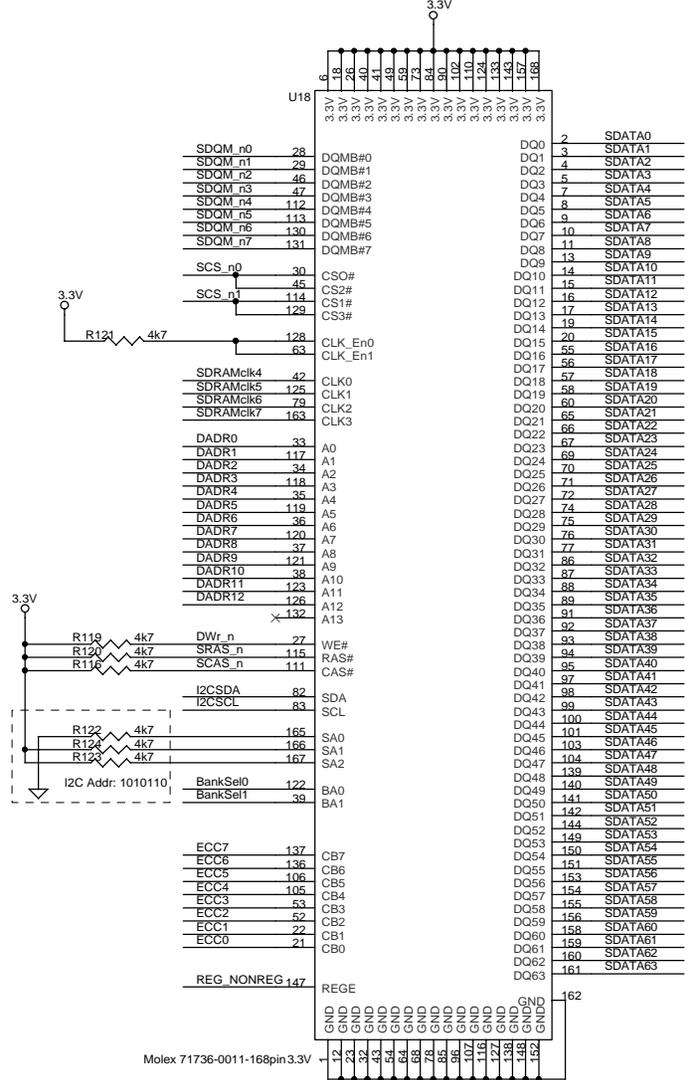
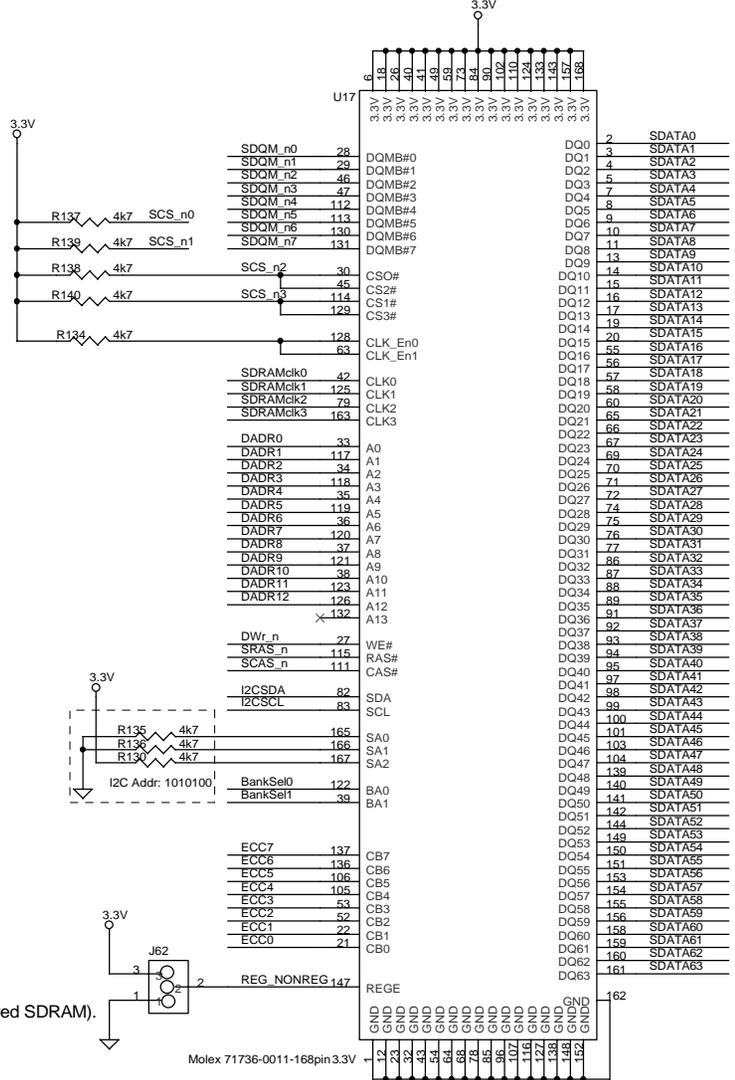
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EV-64240/60A-BP			
Title			
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SCAS_n
SRAS_n
DWr_n
BankSel[1..0]
DADR[12..0]
SDQM_n[7..0]
SCS_n[3..0]
SDRAMclk[7..0]

ECC[7..0]
SDATA[63..0]
I2CSDA
I2CSCL

Secondary DIMM (Banks 2 & 3)

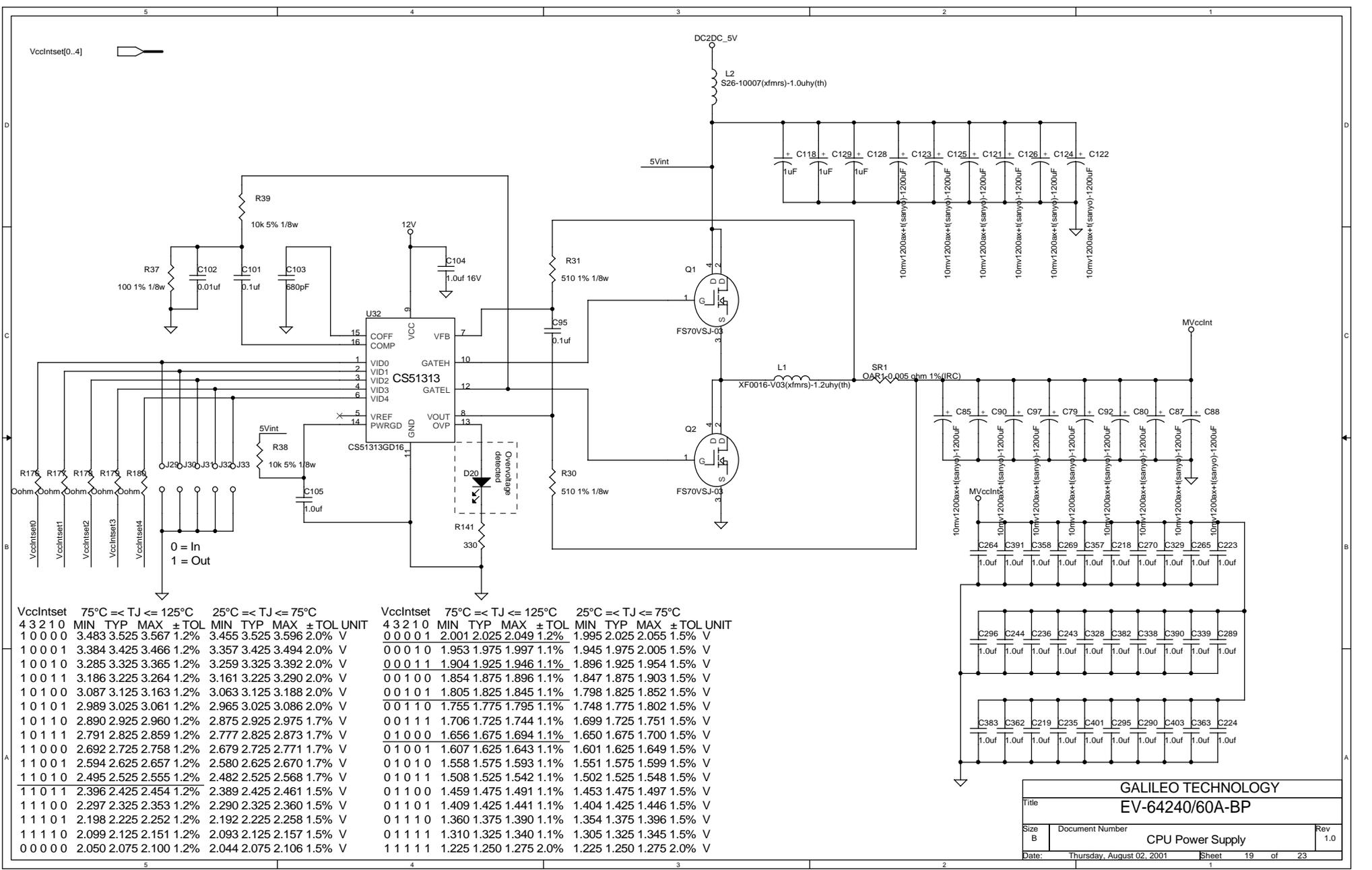
Main DIMM (Banks 0 & 1)



J62 set to 1-2: Buffered mode.
2-3: Registered mode.
(Applicable only with a registered SDRAM).

Use only PC133 SDRAM modules !!!

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VccIntset 75°C =< Tj <= 125°C 25°C =< Tj <= 75°C

4 3 2 1 0	MIN	TYP	MAX	±TOL	MIN	TYP	MAX	±TOL	UNIT
1 0 0 0 0	3.483	3.525	3.567	1.2%	3.455	3.525	3.596	2.0%	V
1 0 0 0 1	3.384	3.425	3.466	1.2%	3.357	3.425	3.494	2.0%	V
1 0 0 1 0	3.285	3.325	3.365	1.2%	3.259	3.325	3.392	2.0%	V
1 0 0 1 1	3.186	3.225	3.264	1.2%	3.161	3.225	3.290	2.0%	V
1 0 1 0 0	3.087	3.125	3.163	1.2%	3.063	3.125	3.188	2.0%	V
1 0 1 0 1	2.989	3.025	3.061	1.2%	2.965	3.025	3.086	2.0%	V
1 0 1 1 0	2.890	2.925	2.960	1.2%	2.875	2.925	2.975	1.7%	V
1 0 1 1 1	2.791	2.825	2.859	1.2%	2.777	2.825	2.873	1.7%	V
1 1 0 0 0	2.692	2.725	2.758	1.2%	2.679	2.725	2.771	1.7%	V
1 1 0 0 1	2.594	2.625	2.657	1.2%	2.580	2.625	2.670	1.7%	V
1 1 0 1 0	2.495	2.525	2.555	1.2%	2.482	2.525	2.568	1.7%	V
1 1 0 1 1	2.396	2.425	2.454	1.2%	2.389	2.425	2.461	1.5%	V
1 1 1 0 0	2.297	2.325	2.353	1.2%	2.290	2.325	2.360	1.5%	V
1 1 1 0 1	2.198	2.225	2.252	1.2%	2.192	2.225	2.258	1.5%	V
1 1 1 1 0	2.099	2.125	2.151	1.2%	2.093	2.125	2.157	1.5%	V
0 0 0 0 0	2.050	2.075	2.100	1.2%	2.044	2.075	2.106	1.5%	V

VccIntset 75°C =< Tj <= 125°C 25°C =< Tj <= 75°C

4 3 2 1 0	MIN	TYP	MAX	±TOL	MIN	TYP	MAX	±TOL	UNIT
0 0 0 0 1	2.001	2.025	2.049	1.2%	1.995	2.025	2.055	1.5%	V
0 0 0 1 0	1.953	1.975	1.997	1.1%	1.945	1.975	2.005	1.5%	V
0 0 0 1 1	1.904	1.925	1.946	1.1%	1.896	1.925	1.954	1.5%	V
0 0 1 0 0	1.854	1.875	1.896	1.1%	1.847	1.875	1.903	1.5%	V
0 0 1 0 1	1.805	1.825	1.845	1.1%	1.798	1.825	1.852	1.5%	V
0 0 1 1 0	1.755	1.775	1.795	1.1%	1.748	1.775	1.802	1.5%	V
0 0 1 1 1	1.706	1.725	1.744	1.1%	1.699	1.725	1.751	1.5%	V
0 1 0 0 0	1.656	1.675	1.694	1.1%	1.650	1.675	1.700	1.5%	V
0 1 0 0 1	1.607	1.625	1.643	1.1%	1.601	1.625	1.649	1.5%	V
0 1 0 1 0	1.558	1.575	1.593	1.1%	1.551	1.575	1.599	1.5%	V
0 1 0 1 1	1.508	1.525	1.542	1.1%	1.502	1.525	1.548	1.5%	V
0 1 1 0 0	1.459	1.475	1.491	1.1%	1.453	1.475	1.497	1.5%	V
0 1 1 0 1	1.409	1.425	1.441	1.1%	1.404	1.425	1.446	1.5%	V
0 1 1 1 0	1.360	1.375	1.390	1.1%	1.354	1.375	1.396	1.5%	V
0 1 1 1 1	1.310	1.325	1.340	1.1%	1.305	1.325	1.345	1.5%	V
1 1 1 1 1	1.225	1.250	1.275	2.0%	1.225	1.250	1.275	2.0%	V

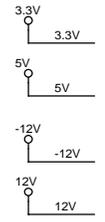
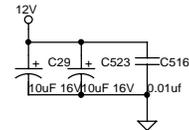
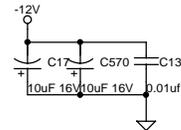
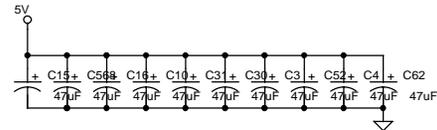
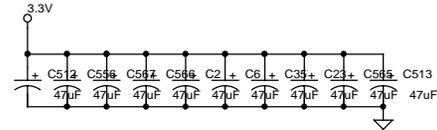
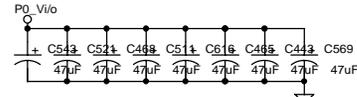
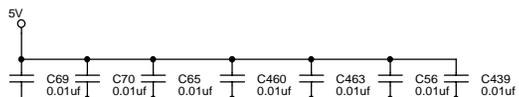
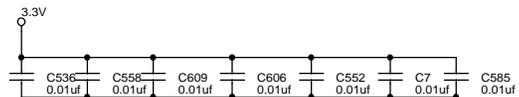
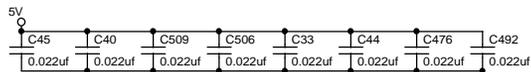
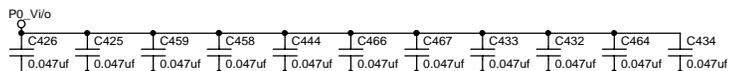
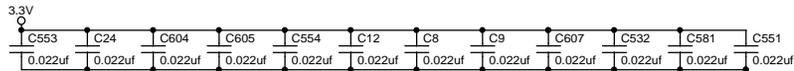
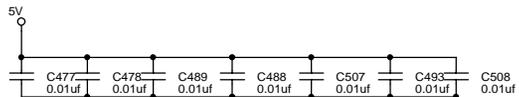
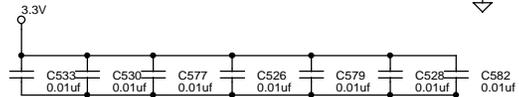
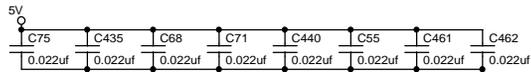
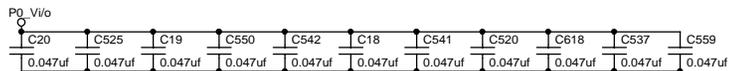
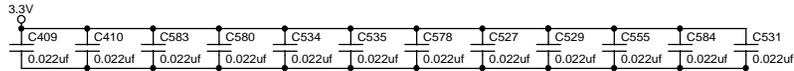
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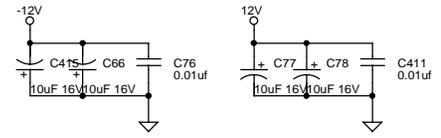
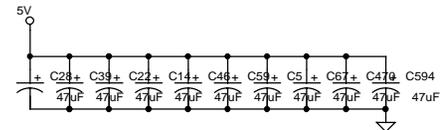
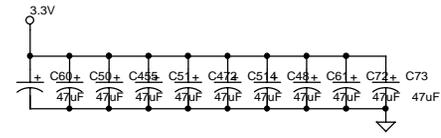
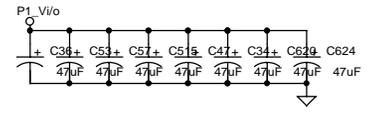
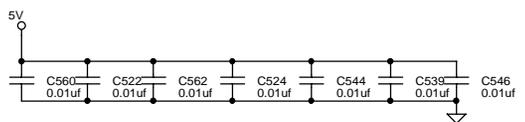
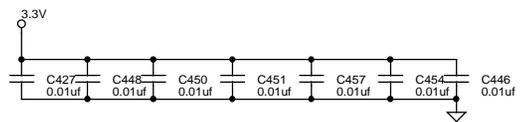
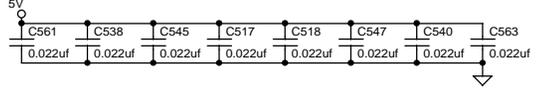
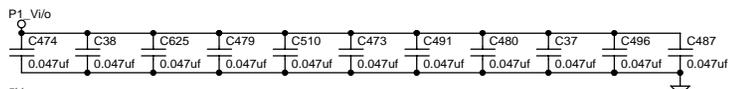
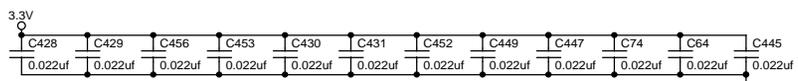
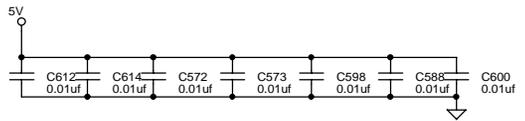
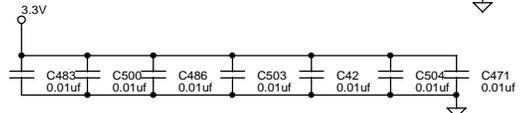
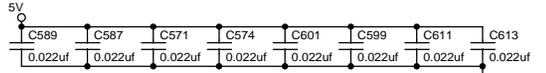
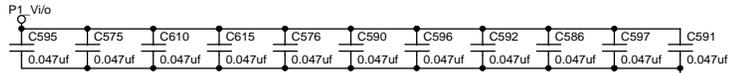
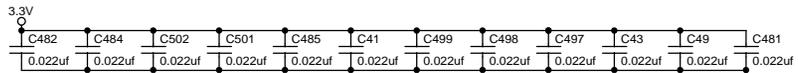
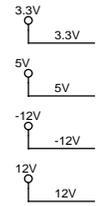
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CAPACITORS TO BE CONNECTED TO THE 5V V_{I/O} AND 3.3V PINS
(AS CLOSE AS POSSIBLE AND NO MORE THEN 0.25")



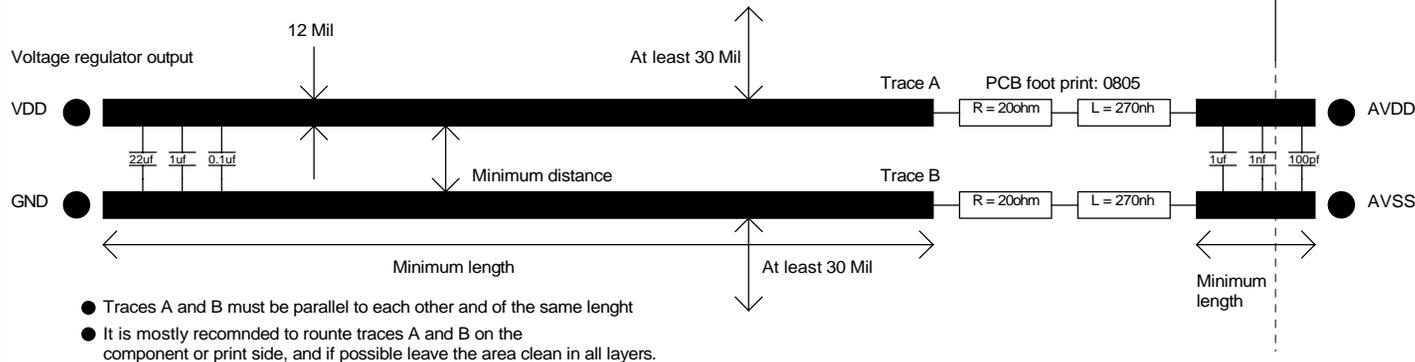
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CAPACITORS TO BE CONNECTED TO THE 5V VI/O AND 3.3V PINS
(AS CLOSE AS POSSIBLE AND NO MORE THEN 0.25")

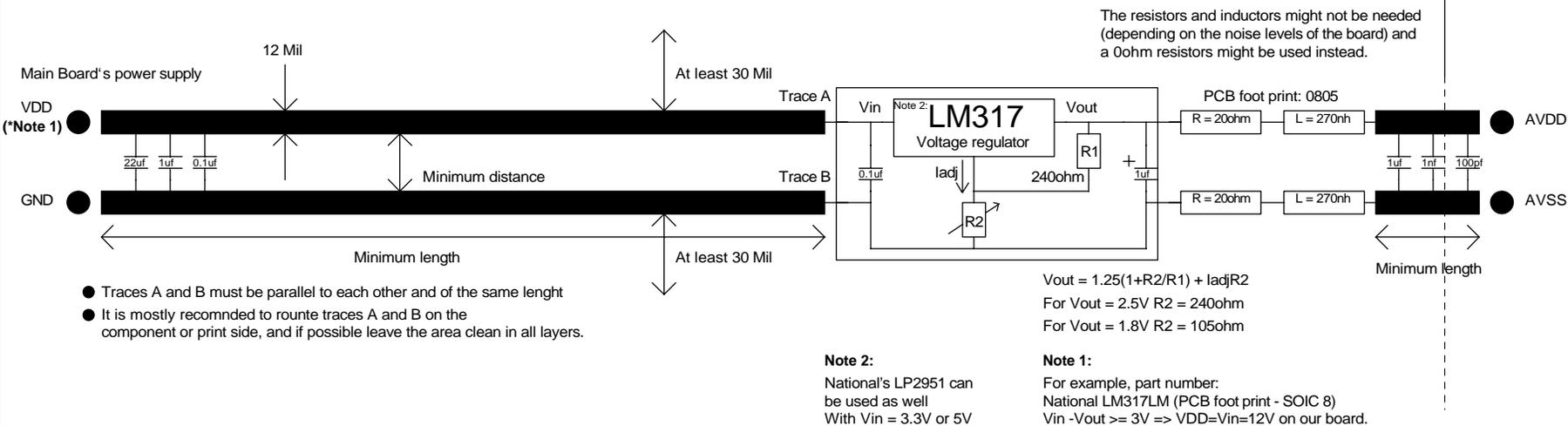


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Application note for a PCI add on card.



Application note for a back-plane layout



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