1. Introduction

This Technical Bulletin provides information for designing a system using the MV643xx.

Use this document as an addition to the following related documentation:

- MV64340/1/2, System Controller for MIPS Processors, Doc. No. MV-S100613-00
- MV64360/1/2, System Controller for PowerPC Processors, Doc. No. MV-S100614-00
- DB-64340/60-BP, Development Board for the MV64340/60, Doc. No. MV-L100051-10

2. Hardware Issues

2.1 DDR Interface Power Supplies and Filtering for DIMMs Design Configuration

The DDR Interface was designed according to the JEDEC DDR SSTL-2 specification. However, as a result of lab tests, a few changes were made to improve signal integrity during the DB-64340/60-BP rev. 1 (development board) ramp up.

2.1.1 Design of the DDR Interface Power Supplies

The DDR interface requires three power supplies:

- Vref - 1.25V for the Vref supply inputs to both the MV643xx and DIMMs
- VTT - 1.25V for the parallel terminations
- VDDQ - 2.5V

The following descriptions for the connections, placement, and filtering of the VTT and Vref pins were determined by lab measurements during the DB-64340/60-BP rev. 1 ramp up.

This topology is the final implementation for the DB-64340/60-BP rev. 2.2.

Vref Supply

In the DB-64340/60-BP rev. 1, the SSTL-Vref was driven from a special SSTL-Vref/VTT DC2DC component. The supply was driven to balls D24 (SSTL_VREF0) and E10 (SSTL_VREF1) in the MV643xx and to pin-1 in both DDR-DIMMs.

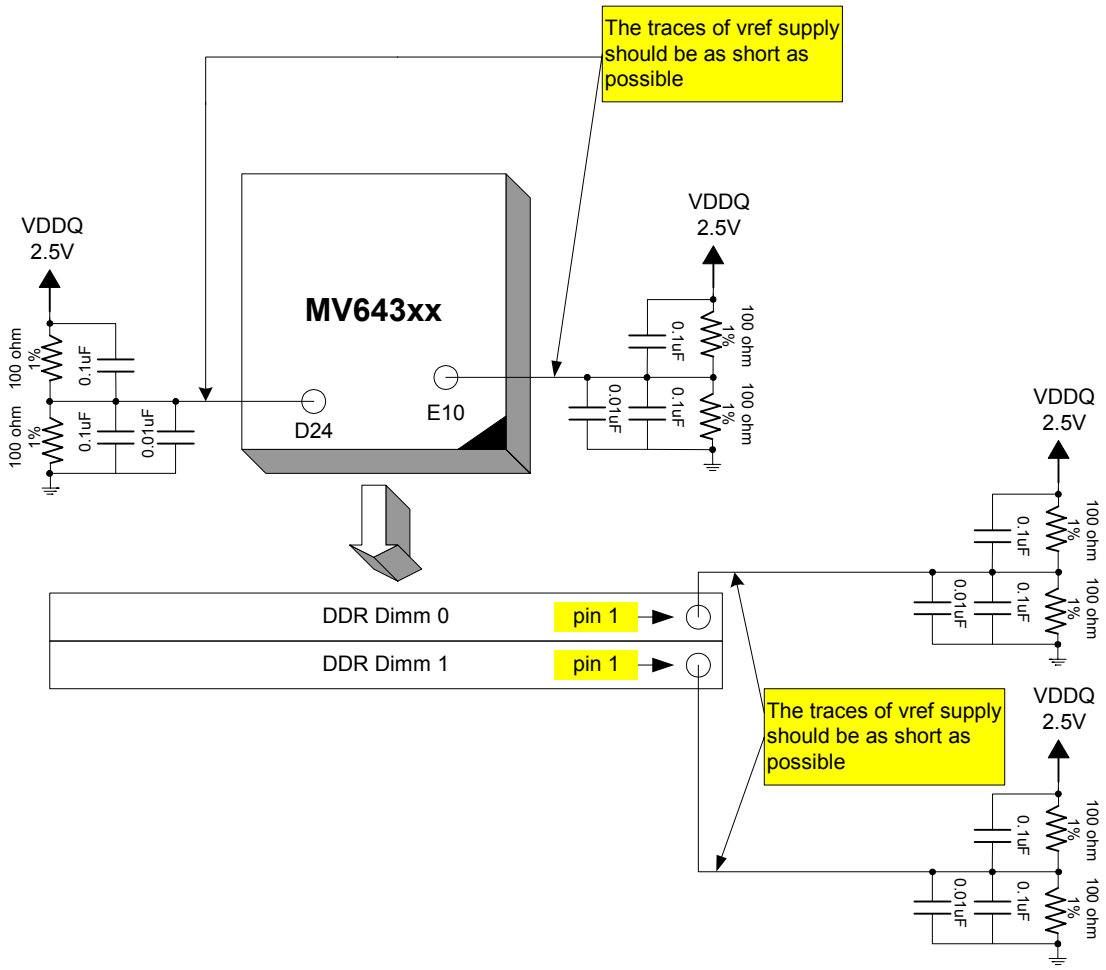
In the new board revision, four separated simple voltage dividers with capacitors are used (two MV643xx balls and the two DIMMs). This change was due to lab experiments that tested the premise that if one trace connects between all four consumers, it causes the Vref signal to be longer, which exposes the Vref supply to noise. Any ripple on the Vref bias might effect the receiver (MV643xx or DIMM) at data sampling.

Figure 1 shows how to connect the Vref.

Notes

- The MV643xx Vref signals must not be connected to the DDR DIMMs Vref. Use a different Vref divider for each MV643xx SSTL-Vref pin and for each DIMM SSTL-Vref pin.
- The implementation of the recommended Vref generation was taken from the internal implementation of a common DC2DC Vref/VTT power-supply (e.g., FairChild ML6554).

Figure 1: Recommended Vref Connection

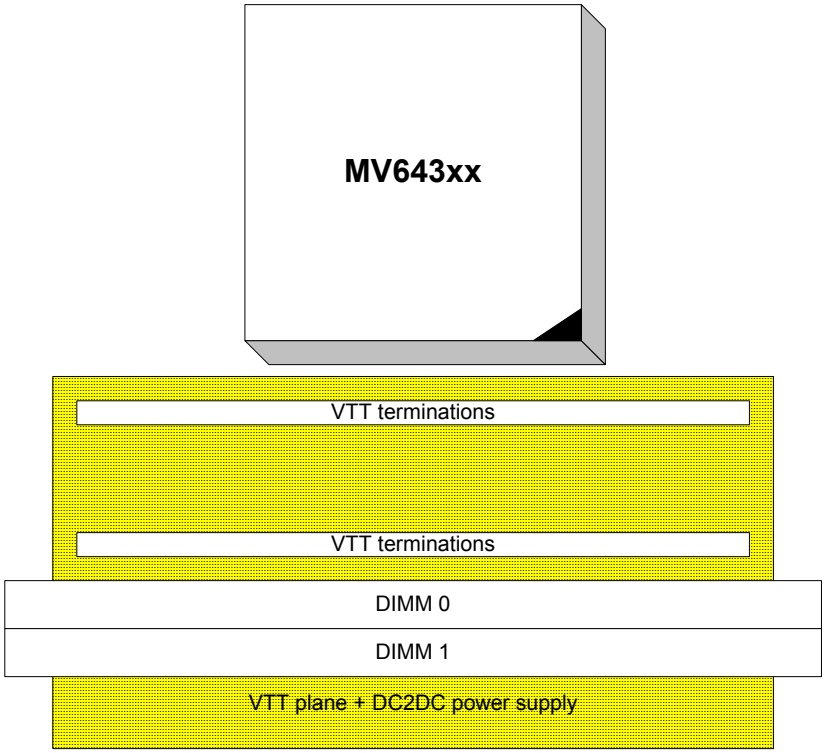


VTT Supply

The VTT supply is used for parallel terminations. Use a strong power supply which can source and sink high current for the VTT supply, since the termination current consumption might be very high.

In the DB-64340/60-BP rev. 1, two parallel terminations were used for each signal. One was placed near the MV643xx and the other near the DIMMs. Figure 2 shows the layout topology designed for the DB-64340/60-BP rev. 1.

Figure 2: DB-64340/60-BP Rev. 1 VTT Layout

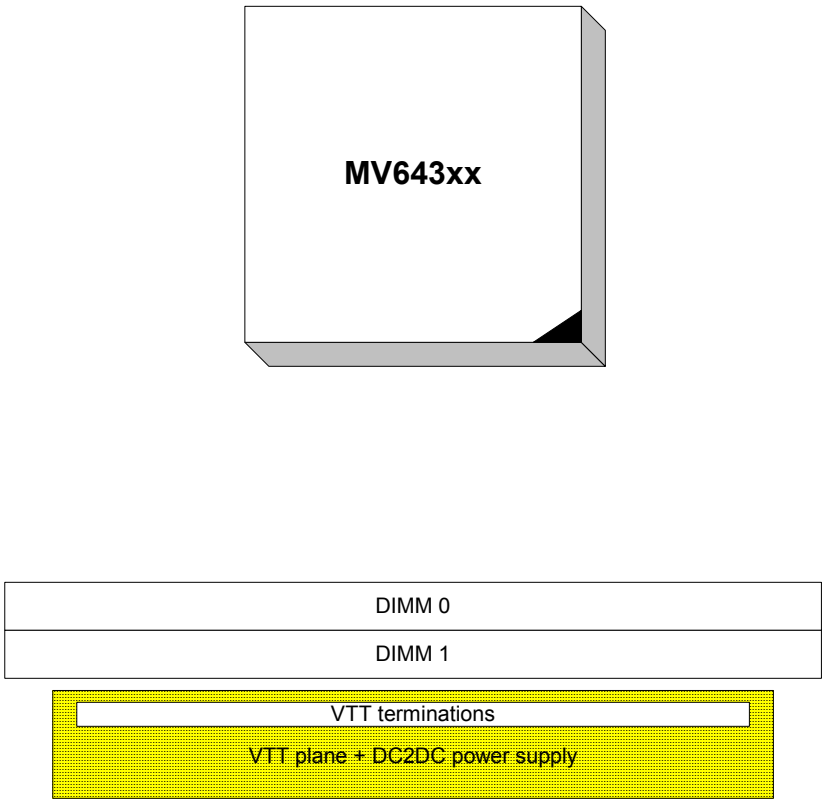


DB-64340/60-BP rev. 1 used two parallel terminations on each signal, as suggested in the JEDEC SSTL-2. But as shown in Figure 2, the VTT polygon needed to cross layers. This caused instability in the VTT voltage level.

During the electrical test-plan, it was observed that while the DDR interface was in IDLE, the VTT measured was 1.25V ±10mV, but when Read/Write transactions (especially SSO) were performed, levels of 1.25v ±180mV were measured These spikes changed the values of expected data on both Read/Write transactions.

To avoid this stability problem on the VTT supply, the DB-64340/60-BP rev. 2 uses a new design for the VTT power supply. This new design provides improved VTT supply. In this revision, the layout and compensation capacitors have been modified. It is also recommended to place the VTT polygon on the component side, not in one of the inner layers. Figure 3 shows how the polygons for the VTT supply differ from Figure 2.

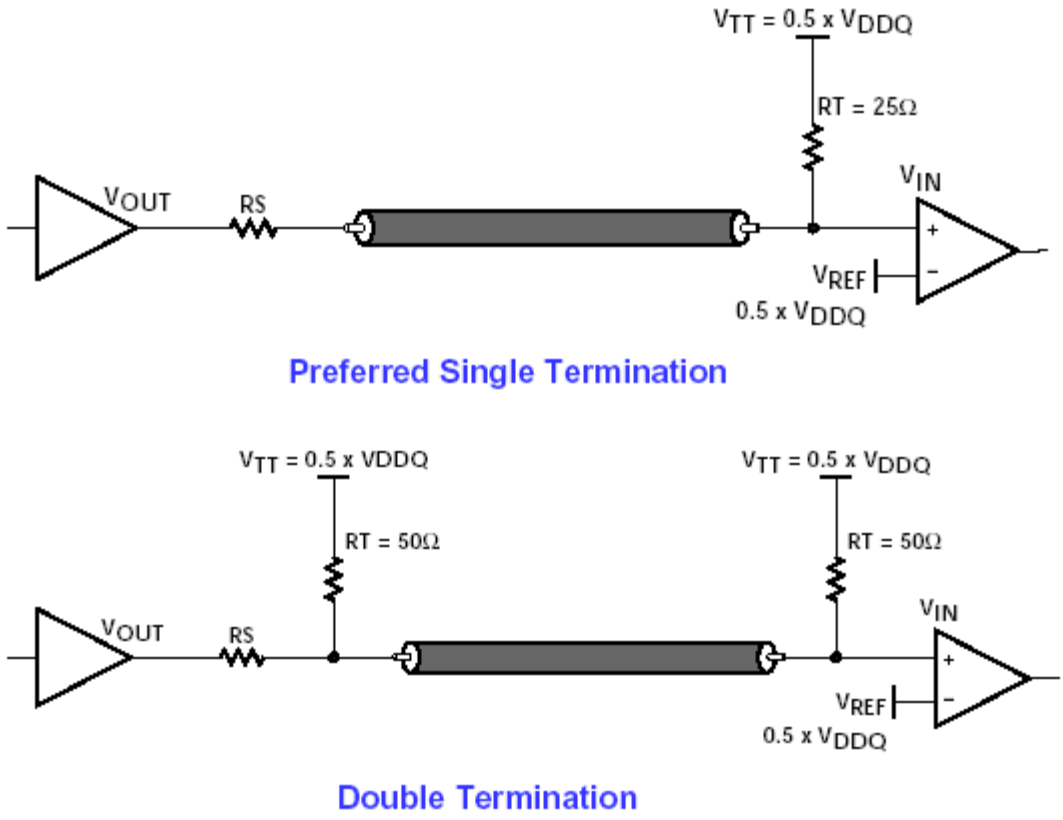
Figure 3: DB-64340/60-BP Rev. 2 VTT Layout



DB-64360-BP rev 2 was designed according to the Micron DDR layout recommendation, as described in Figure 4. The upper termination shows that Micron recommends a single termination on a DDR DIMM designs. These guidelines were followed, except for the following minor changes:

- In the development board RT = 59 Ohm was used. This value gives the best signal integrity on the SSTL signals.
- The termination is behind the DIMM receiver. This keeps the VTT plane as small as possible and prevents cross-over to another layer.

Figure 4: Micron DDR Layout Recommendation



VTT Termination

Figure 7 shows the VTT plane layout and its compensation capacitors.

- RNET are the parallel terminations.
- CNET are push-pull compensation capacitors.

For every two parallel terminations, two capacitors are placed as close as possible to the resistors. One capacitor is a 100 nF capacitor to VSS and the other is a 100 nF capacitor to VDDQ (2.5V). Two capacitors are required since the VTT supply is a "push-pull" supply and the current flows in both directions (VDDQ and GND) (see Figure 6).

Figure 7 also illustrates three low ESR capacitors that are equally located on the VTT plane. In rev. 1 of the board, only one low ESR capacitor was placed on the board. In rev. 2, two additional capacitors were needed for compensation purposes.

Additionally, in rev. 2 three additional capacitor types are placed on the SSTL VTT plane. Those capacitors are:

- Three 10 uF
- Four 100 nF
- Four 100 pF

Figure 5: Extra Capacitor

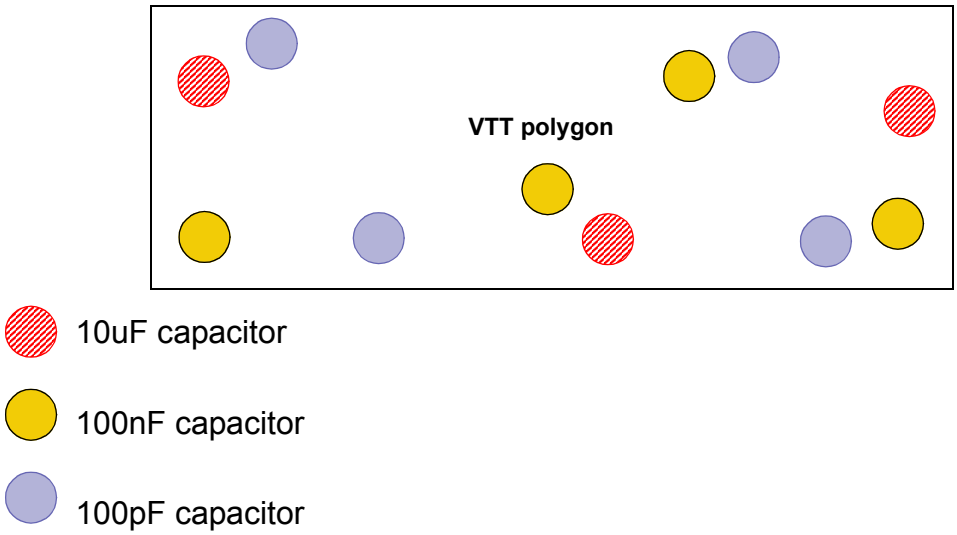


Figure 6: Push-Pull Compensation Capacitors

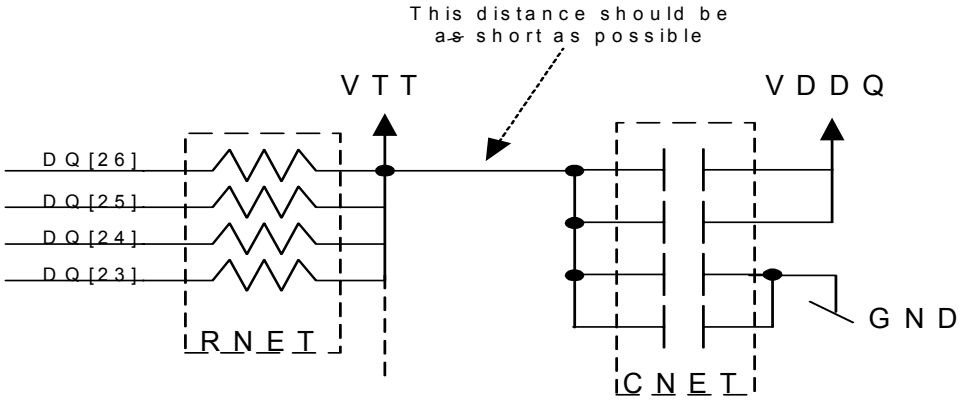
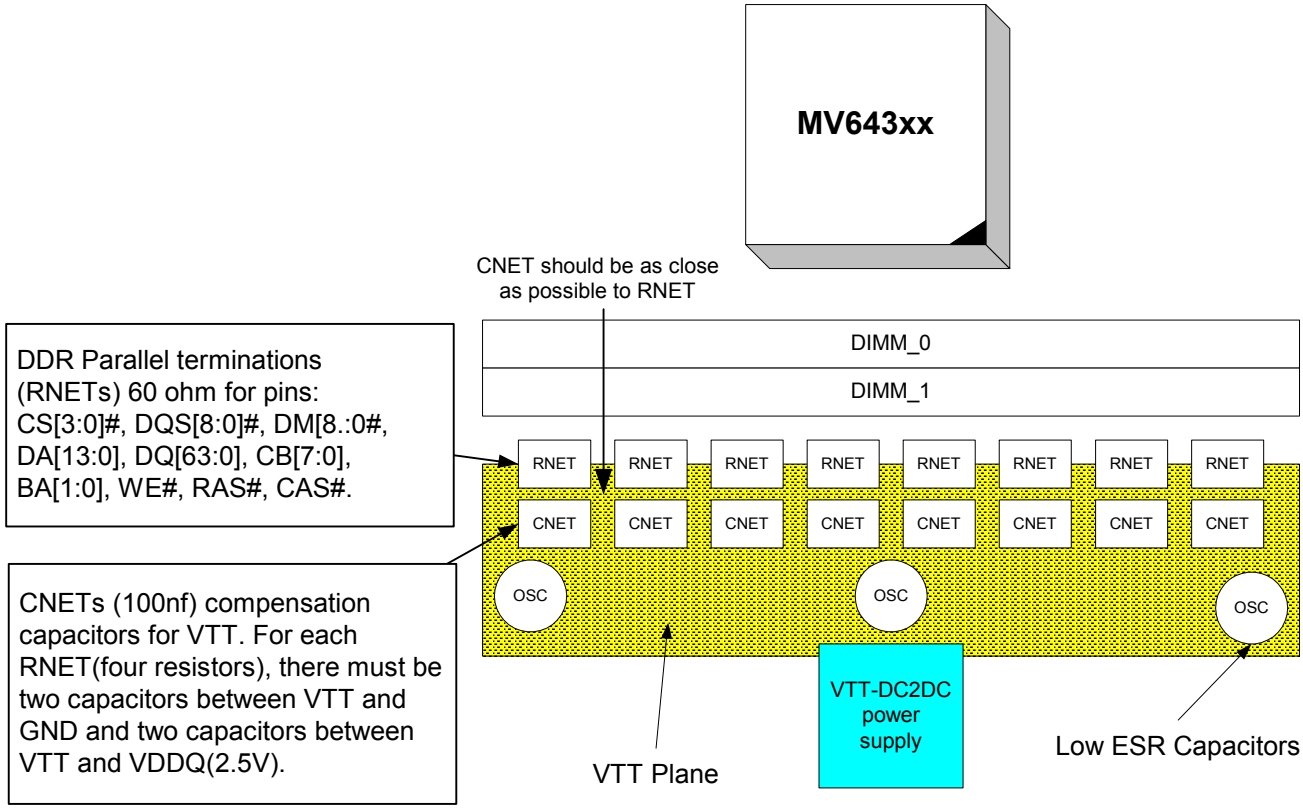


Figure 7: VTT Plane and Components



2.2 Routing of the StartBurst and FDBclk Signals

There are two modes of operation when interfacing the DDR–- Sync and Async. In Sync mode, the DDR clock frequency is equal to the Tclk frequency. In Async mode, the frequencies are independent.

In Sync mode, StartBurst and FBClk are internal to the chip, however it is highly recommended to route them as in Async mode (further details in the following sections).

In Async mode, the StartBurst and FDBClk are routed externally and are subject to board noise. To avoid errors, route Start-Burst and FDBClk as far as possible from high frequency, strong drive signals. This prevents these signals from being disrupted by crosstalk and other noise effects.

The two pairs (StartBurstIn-StartBurstOut and feedBackClockOut) use a parallel termination (60-Ohm) to VTT and are routed with a minimum clearance of 20 mil from other signals and between themselves.

More details on how to calculate the exact length of these two pairs is explained in the next section.

2.3 DDR Signal Routing and Length for DIMMs Design Configuration

According to JEDEC all DDR signals (Address, Data, Clock and Control) should be at same length ±100mil from the Controller to the DDR DIMMs. The total length of these signals also depends on the MV643xx timing parameters. The following two sections are the length restrictions for Sync & Async modes:

2.3.1 Sync Mode

According to the JEDEC specification, all DDR signals must be routed with the same length. This restriction alone is not sufficient, because designers will be able to route them at different lengths. The traces length limit is defined with a new timing parameter, $t_{DqsClkOutskew}$.

$t_{DqsClkOutskew}$ is DQS input skew in reference to ClkOut.

According to MV643xx timing: 0.6ns < $t_{DqsClkOutskew}$ < 3.4 ns.

The DQSin signal returning from DDR DIMM (in Read transaction) is sampled with the same clock with which the Read command was driven to the DDR (clkOut).Therefore there is a timing restriction on the skew allowed between DQSin and ClkOut.

$t_{DqsClkOutskew}$ = TClkOutFT + TClkBuffPD + TDdrClkDqs - TClkBuffDeskew + TDqsFT

where:

TClkOutFT = Clkout fly time to the DDR SDRAM device. (Figure 9, “Sync Mode Parameters,” on page 10).

TClkBuffPD = Clock buffer propagation delay. (Should be taken from the Clock Buffer datasheet.)

TClkBuffDeskew = Clock buffer feedback clock delay. (Figure 9, “Sync Mode Parameters,” on page 10).

TDdrClkDqs = DDR SDRAM Clock to DQS output delay. (Should be taken from the DDR SDRAM DIMMs datasheet, where it is usually called "tDQSCK".)

TDqsFT = DQS fly time. (Figure 9, “Sync Mode Parameters,” on page 10).

Figure 8 is an example of all timing definitions mentioned above and the relation between them.

Note

The FBclkin/FBclkout and StartBurstOut/StartBurstIn pairs are not mentioned in this section, since they are not sampled by the device. However, it is highly recommended to route them in the manner described in Section 2.3.2 "Async Mode" on page 11, so they will be able to support higher frequencies in the future. Otherwise, connect FBClkIn and StartBurstIn to a pull up resistor, or just connect them to StartBurstOut and FBClkOut respectively.

Table 1: DDR SDRAM AC Timing 133 MHz Frequency[1]

Signals	Description	Min.	Max.	Units
ClkOut/ClkOut#	Frequency	100	133	MHz
ClkOut/ClkOut#	Cycle Time	7.5	10	ns
ClkOut/ClkOut#	Duty Cycle	48	52	%
ClkOut/ClkOut#	Slew Rate	1		V/ns
DQ[63:0], CB[7:0][2]	t_{DSi} (Data input setup relative to DQS input.)	-1.2		ns
DQ[63:0], CB[7:0][2]	t_{DHi} (Data input hold relative to DQS input.)	2.1		ns
A[13:0], BA[1:0]	Address output delay (relative to ClkOut)	0.9	2.2	ns
RAS#, CAS#, WE#, CS[3:0]#, StartBurst#	Control output delay (relative to ClkOut)	0.9	2.1	ns

Table 1: DDR SDRAM AC Timing 133 MHz Frequency[1] (Continued)

Signals	Description	Min.	Max.	Units
DQ[63:0], CB[7:0], DM[8:0]	t_{DS} (Data output setup relative to DQS.)	0.6		ns
DQ[63:0], CB[7:0], DM[8:0]	t_{DH} (Data output hold relative to DQS.)	1.7		ns
DQ[63:0], CB[7:0], DM[8:0]	t_{DIPW} (Data output pulse width)	2.3		ns
DQS input to ClkOut/ClkOut# skew[2]	$t_{DqsClkOutskew}$	0.6	3.4	ns

1. This table was taken from the MV-643xx datasheet, Rev. B. It is recommended that you refer to the latest revision of the datasheet for the most up-to-date information.
2. This parameter is not defined in Rev B. It will be added to Rev C of the datasheet.

Figure 8: DQS Input to ClkOut Skew Waveform

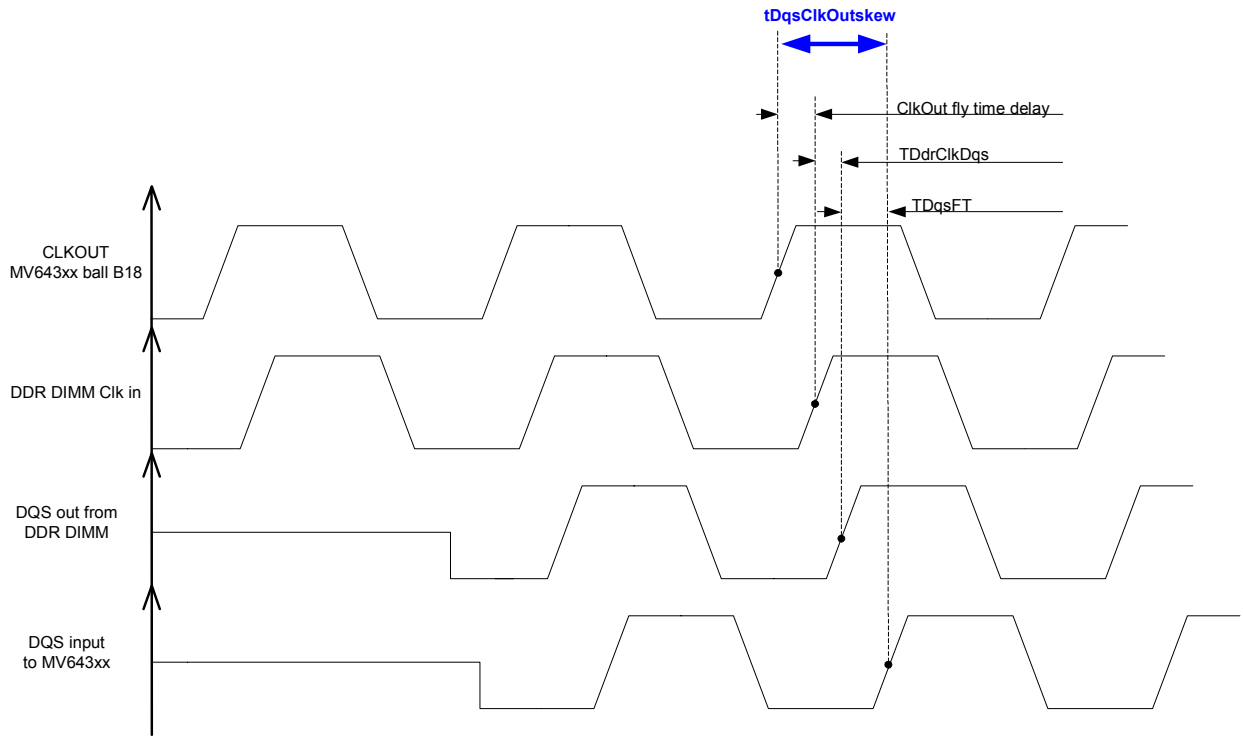
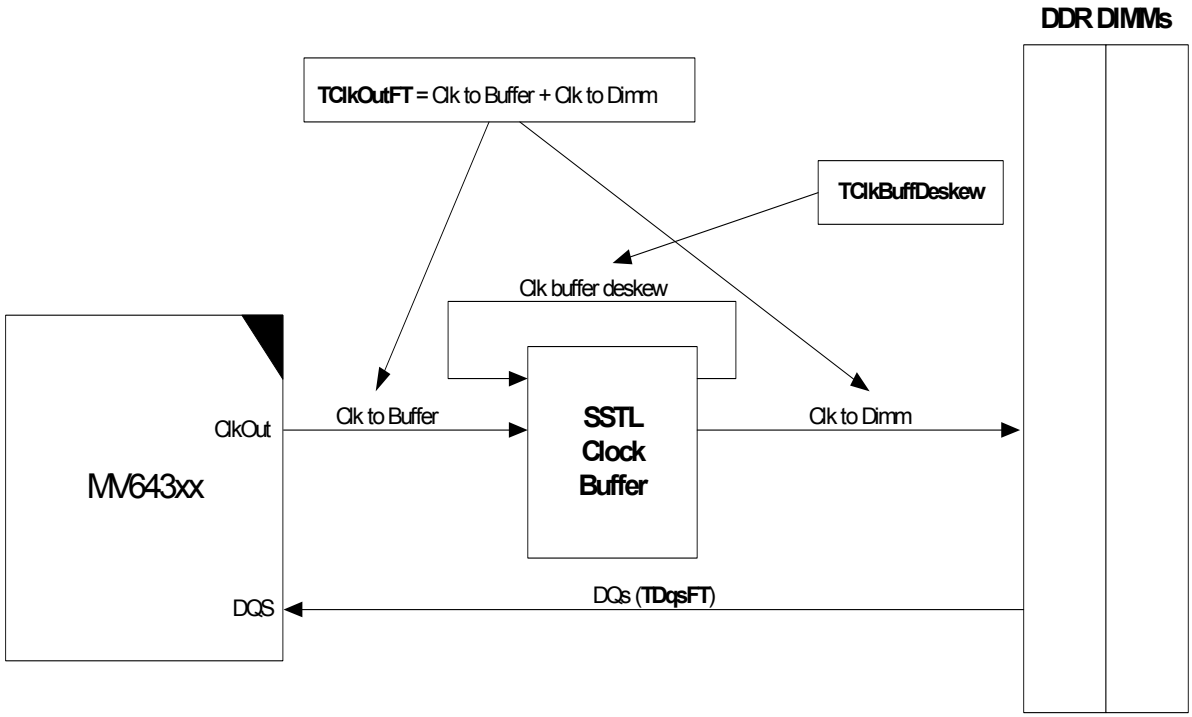


Figure 9: Sync Mode Parameters



Example: Let us presume the following lengths:

Clk to Buffer = 1.8"

Clk buffer deskew = 0.5"

Clk to DIMM = 2.7"

Dqs = 4"

TDdrClkDqs = ± 0.8 ns

$t_{DqsClkOutskew}$ = TClkOutFT + TClkBuffPD + TDdrClkDqs - TClkBuffDeskew + TDqsFT

$t_{DqsClkOutskew}$ = (1.8"+2.7") X 0.18 + 0.1 ns ± 0.8 ns - 0.5" X 0.18 + 4" X 0.18 = 0.81 ns + 0.1 ns ± 0.8 ns - 0.09 ns + 0.72 ns = 1.54 ns ± 0.8 ns

Notes

- All lengths (in inches) were multiplied by 0.18 [ns/inch].
- Make sure that the clock deskew of the clock buffer is inside the Access window of DQs from CK/CK# define in the DDR device datasheet.
- Make sure that the recommended setup and hold time are not violated by the clock deskew.
- It is highly recommended to place the DDR SDRAM devices as close as possible to the Discovery II device. The signals trace length must not exceed 8".

2.3.2 Async Mode

In Section 2.3.1 "Sync Mode"the MV643xx timing restriction is between DQs returning from the DDR DIMMs to DDR clock out. In the Async mode we use the FBClkIn and FBClkOut pins. The FBClkOut is routed out of the MV643xx and reconnected to the MV643xx to the FBClkIn ball.

tDqsFBClkinskew is DQS input skew in reference to FBClkin.

tDqsFBClkinskew = TClkOutFT + TClkBuffPD + TDdrClkDqs - TClkBuffDeskew + TDqsFT + ClkOut_FBClk_Skew - FBClkFT

where:

TClkOutFT = Clkout fly time to the DDR SDRAM device. (Figure 11, “ASync Mode Parameters,” on page 14)

TClkBuffPD = Clock buffer propagation delay. (should be taken from the Clock Buffer datasheet.)

TClkBuffDeskew = The Clock buffer feedback clock delay. (Figure 11, “ASync Mode Parameters,” on page 14)

TDdrClkDqs = DDR SDRAM Clock to DQS output delay. (Should be taken from the DDR SDRAM DIMMs datasheet.)

TDqsFT = DQS fly time. (Figure 11, “ASync Mode Parameters,” on page 14)

ClkOut_FBClk_Skew = Skew between ClkOut to FBClkout. (± 0.1ns) (Figure 8, “DQS Input to ClkOut Skew Waveform,” on page 9)

FBClkFT = Total Length of: FBClkout + FBClkin

tDqsFBClkinskew must be equal to -3.3 ns < tDqsFBClkinskew < 0.7 ns

After calculating the FBClkIn + FBClkOut routing length, the StartBurstOUT + StartBurstIn length should be calculated.

The StartBurstOut + StartBurstIn total length must be calculated according to the following timing restrictions:

StartBurstOut output delay in reference to FBClkOut: min=0.6; max=1.4 (1 ± 0.4); Units = ns

StartBurstIn to FBClkIn skew; min = -0.32; max = 0.6; Units = ns

-0.32 ns =< (StartBurst_Length" - FBClk_Length") X 0.18 + 1 ns ± 0.4 ns =< 0.6 ns

Thus: 4.44" =< FBClk_Length" - StartBurst_Length" =< 5.11"

Example: Let us presume the following lengths:

Clk to Buffer = 1.8"

Clk buffer deskew = 0.5"

Clk to DIMM = 2.7"

Dqs = 4"

TDdrClkDqs = ± 0.8 ns

FBClkout + FBClkin [in length] = 10"

tDqsFBClkinskew = (1.8"+2.7") X 0.18 + 0.1 ns ± 0.8 ns - 0.5" X 0.18 + 4" X 0.18 ± 0.1 ns - 10 X 0.18 = -0.26 ns ± 0.9 ns

In this example we are in the range of: -3.3 ns < -0.26 ns ± 0.9ns < 0.7 ns, but we can improve the margin by enlarging the FBClkout + FBClkin to a longer trace.

For example if we enlarge FBClkout + FBClkin [in length] to 12" then:

tDqsFBClkinskew - FBClkFT = 1.54 ns ± 0.9ns - 12 X 0.18 = -0.62 ns ± 0.9 ns

4.44" =< 12" - (StartBurstOut + StartBurstIn) =< 5.11"

Thus the best StartBurstOut + StartBurstIn trace length would be 7.22"

Notes

- All lengths (in inches) were multiplied by 0.18 [ns/inch].
- It is highly recommended to place the DDR SDRAM devices as close as possible to the Discovery II device. The signals trace length must not exceed 9".

Figure 10 is an example of all timing definitions mentioned above and the relation between them.

Table 2: DDR SDRAM AC Timing 183 MHz Frequency[1]

Signals	Description	Min.	Max.	Units
ClkOut/ClkOut#	Frequency	133	183	MHz
ClkOut/ClkOut#	Cycle Time	5.5	7.5	ns
ClkOut/ClkOut#	Duty Cycle	48	52	%
ClkOut/ClkOut#	Slew Rate	1		V/ns
DQ[63:0], CB[7:0][2]	t_{DSi} (Data input setup relative to DQS input.)	TBD		ns
DQ[63:0], CB[7:0][2]	t_{DHi} (Data input hold relative to DQS input.)	TBD		ns
A[13:0], BA[1:0]	Address output delay (relative to ClkOut)	0.9	2.2	ns
RAS#, CAS#, WE#, CS[3:0]#, StartBurst#	Control output delay (relative to ClkOut)	0.9	2.1	ns
DQ[63:0], CB[7:0], DM[8:0]	t_{DS} (Data output setup relative to DQS.)	0.65		ns
DQ[63:0], CB[7:0], DM[8:0]	t_{DH} (Data output hold relative to DQS.)	0.92		ns
DQ[63:0], CB[7:0], DM[8:0]	t_{DIPW} (Data output pulse width)	1.75		ns
DQS input to FBCLKIN skew[2]	$t_{DqsFBClkinskew}$	-3.3	0.7	ns

1. This table was taken from the MV-643xx datasheet, Rev. B. It is recommended that you refer to the latest revision of the datasheet for the most up-to-date information.
2. This parameter is not defined in Rev B. It will be added to Rev C. of the datasheet.

Figure 10: DQS Input to FBClkin Skew Waveform

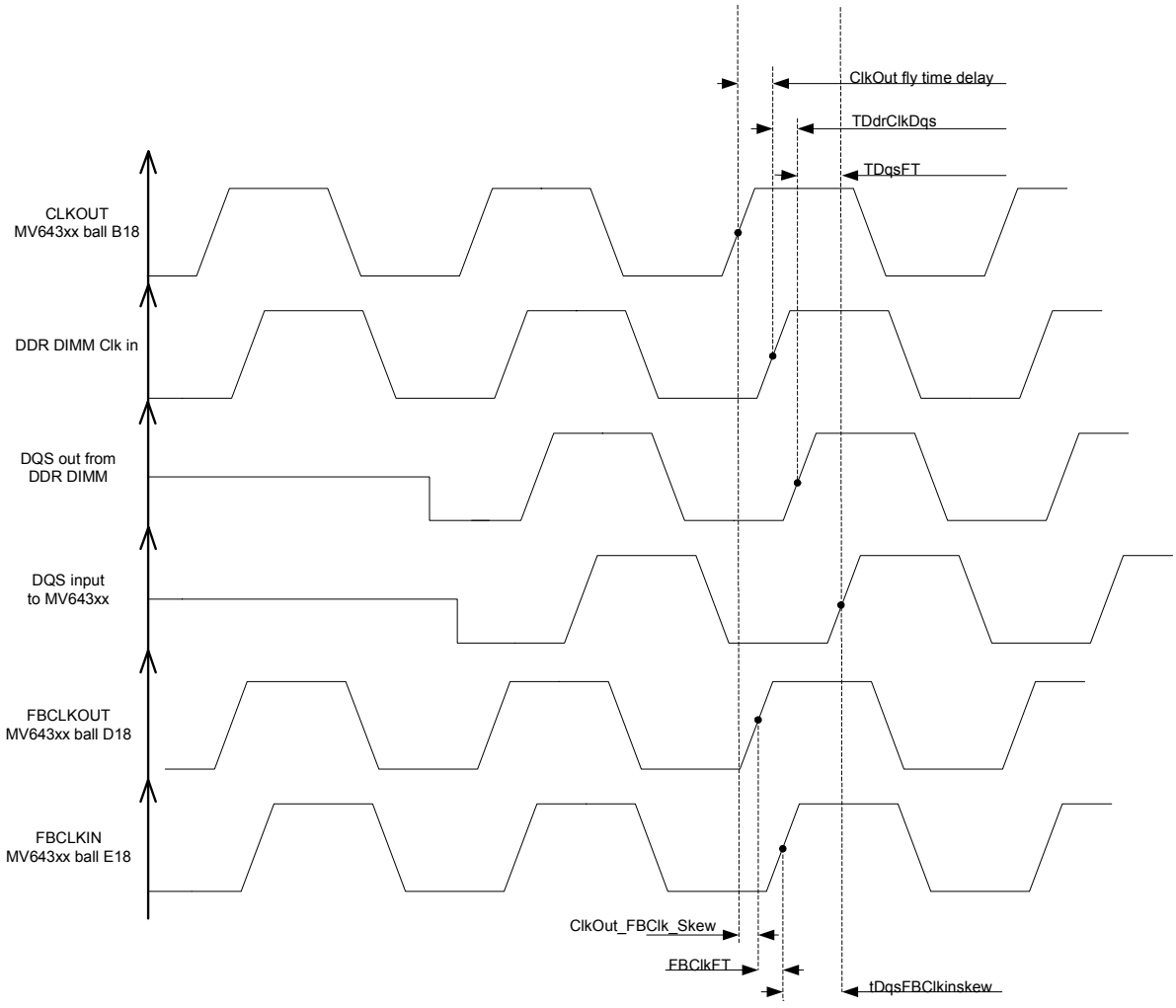
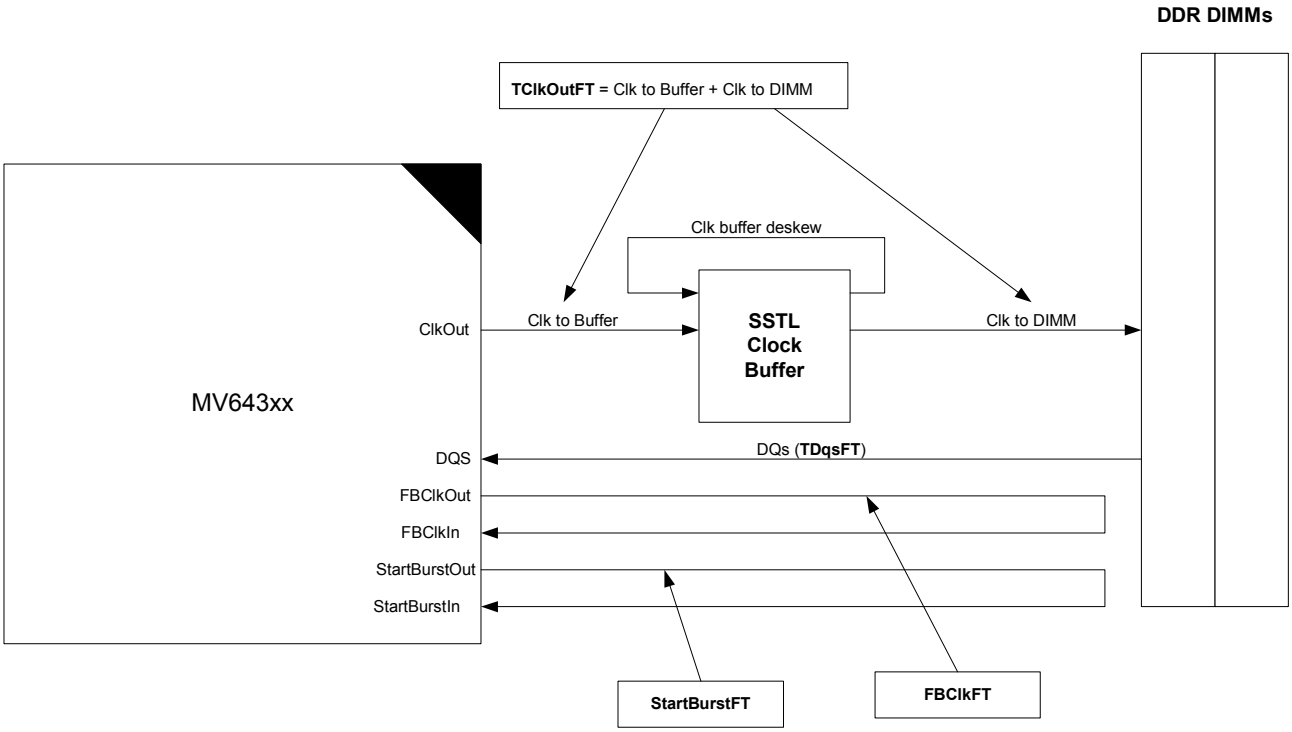


Figure 11: ASync Mode Parameters



2.4 Miscellaneous Issues Fixed in the Board Rev. 2.0

When working with the internal PCI Arbiter, until the software (DINK32, VxWorks, Linux or other client monitor) configures the MV643xx to internal arbiter mode, the PCI bus isn't parked on any agent. Therefore, a pulldown is required on signals P0_GNT_GT# and P1_GNT_GT#. This guarantees that both PCI buses are parked on the MV643xx. Note that only one PCI agent should park on the bus. This means that pulldown should be used only on PCI agents that drive the bus. A pullup should be used on all other PCI agents.

2.5 DDR Boot Strapping at Reset

The following strapping is recommended to get the MV-64340/60 working with the DDR unit in Sync or Async mode.

2.5.1 DDR Unit in Sync Mode

Note

In Sync mode, the M and N values that are sampled at reset have no effect.

The DDR unit is in Sync mode when the DDR memories are running on the DiscoII Core clock (Tclk) and the returning data is in sync with the internal core clock (Tclk).

To enter Sync mode use the following reset strapping configuration:

- DevAD[18] = 1 (DDR Clock is the same as Core clock.)
- DevAD[19] = 1 (Address/Control toggle at Posedge.)
- DevAD[20] = 1 (One Stage of Control Pipe-Line.)
- DevAD[21] = 0 for 133 MHz or 1 for 183 MHz (One/three Stage of Control Pipe-Line.)
- DevAD[22] = 0 (The Incoming data is in sync to core clock.)
- DevAD[23] = 0 (No DFCDL is needed for the FBCLKIN.)
- DevAD[24] = 0 (No DFCDL is needed for the FBCLKIN.)

For further information, see the "Reset Configuration" section of the datasheet

The Dunit Control (Low) register (Offset: 0x1404) must be set as shown in Table 3.

Note

The bits [9:7] values required for using the DDR in Sync mode are different than the fields' initial values.

Table 3: Dunit Control (Low)
Offset: 0x1404

Bits	Field	Type/ Init Value	Description
6:0	Various	Various	See the MV643xx datasheet.
7	RdPipe	RW 0x1	Number of pipeline stages in the Read Data Path. 0 = Bypass
8	RdSyncEn	RW 0x1	Read Data Path Synchronization 0 = Disabled
9	RMWSyncEn	RW 0x1	RMW Path Synchronization 0 = Disabled
23:10	Various	Various	See the MV643xx datasheet.
26:24	StBurstDel	RW 0x3	Number of sample stages on StartBurstIn. Program StBurstDel based on CL, registered/non-buffered DIMM, and frequency. See Table 4 for the recommended values, depending on the DIMM type and CL used.
27	StBurstNeg	RW 0x0	StartBurstIn is first sampled on the falling edge of clock. 0 = Disabled
28	StBurstSrc	RW 0x0	StartBurst source 0 = Generated in the Dunit internally.
31:29	Various	Various	See the MV643xx datasheet.

Table 4: DDR Unit in Sync Mode StBurstDel Settings

CAS Latency	1.5	2	2.5	3	3.5	4
UnBuffered DIMM	011	011	100	100	101	101
Reg-DIMM	100	100	101	101	110	110

2.5.2 DDR Unit in Async Mode

The DDR unit is in Async mode when the DDR memories are running on the DiscoII DDR clock and the returning data is in sync with the feedback clock (FBCLKIN).

To enter Async mode (in the Incoming data path) use the following reset strapping configuration:

- DevAD[18] = 0 (DDR Clock is different from Core clock.)
- DevAD[19] = 1 (Address/Control toggle at Posedge.)
- DevAD[20] = 1 (One Stage of Control Pipe-Line.)
- DevAD[21] = 0 (One Stage of Control Pipe-Line.)
- DevAD[22] = 1 (The Incoming data is sync to Feedback clock.)
- DevAD[23] = 0 (No DFCDL is needed for the Core Clock.)
- DevAD[24] = 0 (No DFCDL is needed for the Core Clock.)
- DevWE[3:0]/DevDP[3:0] = DRAM PLL N Divider (For more information, see the "DRAM Clocking" section of the datasheet.)
- TxD0[6:1] = DRAM PLL M Divider (For further information, see the "DRAM Clocking" section of the datasheet.)

Also, The Dunit Control (Low) register (Offset: 0x1404) must be set as shown in Table 5.

Table 5: Dunit Control (Low)
Offset: 0x1404

Bits	Field	Type/Init Value	Description
6:0	Various	Various	See the MV643xx datasheet.
7	RdPipe	RW 0x1	Number of pipeline stages in the Read Data Path. 1 = One stage
8	RdSyncEn	RW 0x1	Read Data Path Synchronization 1 = Enabled
9	RMWSyncEn	RW 0x1	RMW Path Synchronization 1 = Enabled
23:10	Various	Various	See the MV643xx datasheet.
26:24	StBurstDel	RW 0x3	Number of sample stages on StartBurstIn. Program StBurstDel based on CL, registered/non-buffered DIMM, and frequency. See Table 6 for the recommended values depending on the DIMM type and CL used.
27	StBurstNeg	RW 0x0	StartBurstIn is first sampled on the falling edge of clock. 1 = Enabled

Table 5: Dunit Control (Low)
Offset: 0x1404 (Continued)

Bits	Field	Type/Init Value	Description
28	StBurstSrc	RW 0x0	StartBurst source 1 = Generated from StartBurstIn input pin.
31:29	Various	Various	See the MV643xx datasheet.

Table 6: DDR Unit in Async Mode StBurstDel Settings

CAS Latency	1.5	2	2.5	3	3.5	4
UnBuffered DIMM	010	011	011	100	100	101
Reg-DIMM	011	100	100	101	101	110

2.6 Calibration Resistors

The MV643xx requires the following resistor values for correct drive calibration on the different interfaces:

- DDR SSTL class-2 25 ohms
- PCI 36 ohms
- CPU interface 50 ohms

2.7 Reset Timing

The MV643xx requires 138 Tclk clock cycles between the release of reset and the first access from the CPU.

During this time, the device performs its auto-calibration sequence and initializes the DDR SDRAM.

2.8 PLL/DLL Filtering

The MV643xx contains three PLLs:

- PLL_0 - clock tree deskew.
- PLL_1 - used for the DDR Async mode.
- DLL - Digital PLL for the PCI synchronized module.

These three PLL/DLL units require a stable power supply. Figure 12 shows a special filtering circuit that has been designed, tested, and modified according to lab measurements. The supplies for these three filtering circuits are not driven directly from the planes. Instead, these circuits are routed from the power supply sources, along with their ground (see Figure 13). All traces widths and differential width are strongly recommended for the PLLs supply stability. Figure 13: "Filtering Supply Routing", on page 19 includes all information relevant for this routing.

Figure 12: PLL DLL Recommended Filtering

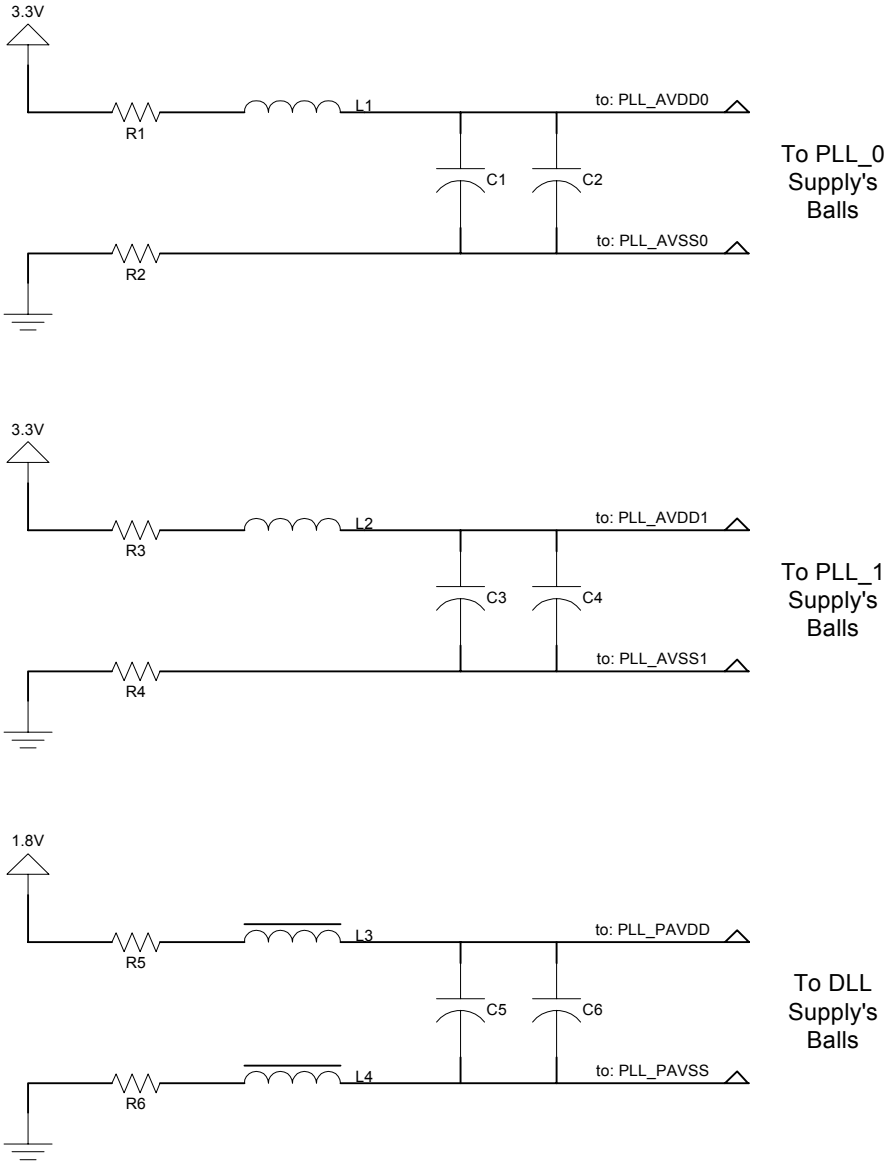


Figure 13: Filtering Supply Routing

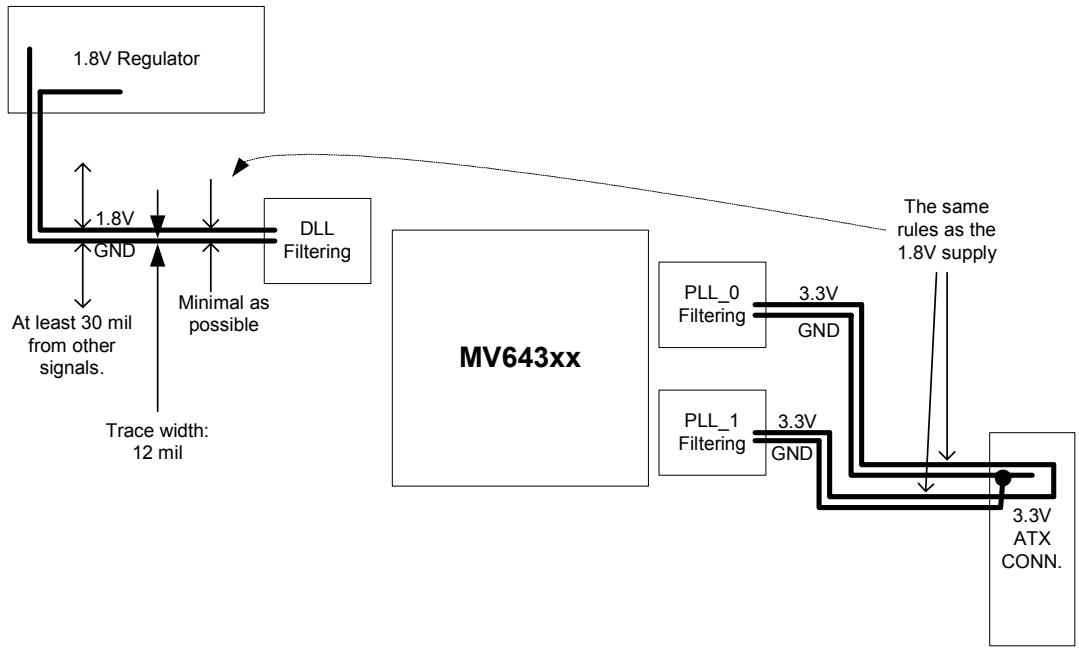


Table 7: Component Value

Ref Designator	Value	Description	Package	P/N Recommended
R1, R2, R3, R4	0 ohm 1%		0603	
R5, R6	10 ohm 5%		0603	
L1, L2	1uH 10%	450 mA	1210	NL322522T-1R0K
L3, L4	50 ohm 600 mA @ 100 MHz	Ferrite	1206	ILB1206
C1, C3, C5	10uF 20% 10V	Tantalum	Type B	
C2, C4, C6	0.1uF 20% 16V		0603	

2.9 Designing with SDRAM DDR Discrete Components on Board

The former sections, Section 2.1.1 "Design of the DDR Interface Power Supplies" and Section 2.3 "DDR Signal Routing and Length for DIMMs Design Configuration" referred to designs with DIMMs on-board (or on add-in cards). When designing a system based on discrete SDRAM DDR components, a number of changes are required. These are described in the following sections.

2.9.1 Design of the DDR Interface with Discrete Components' Power Supplies

Vref Supply

In Section 2.1.1 "Design of the DDR Interface Power Supplies" the recommendation is to supply each DIMM with its own Vref supply by voltage divider. Each DIMM contains only one input pin for the Vref, therefore, in the worst case, two voltage dividers are needed for the two DIMMs. In discrete component topology, each SDRAM component has its own Vref input pin. Thus, if you are designing memory with four components, you will need four voltage dividers to supply the Vref to all components. In theory, this is the recommended method, but there are ways to minimize the amount of dividers needed, as shown in Figure 14, where there are four DDR SDRAMs (combined into 64-bits data). Only ***one*** voltage divider supplies the Vref for the four components. This topology can be used if the memories are close to the MV64360 and a tight design is forced, to save place on the board.

If the DDR SDRAM components are placed on both side of the PCB plane (half on the components side and half on the print side), it is highly recommended that you use two voltage dividers—one on each side of the PCB plane. This will save the Vref trace from crossing from the component side to the print side.

VTT Supply

All recommendations about the VTT supply in Section 2.1.1 "Design of the DDR Interface Power Supplies" are also applicable to the DDR SDRAM discrete components design. Figure 15 shows the recommended topology.

VTT plane, filtering and compensation capacitors should be designed as recommended in Section 2.1.1 "Design of the DDR Interface Power Supplies".

Note

Due to physical limitations, system simulation must be used to avoid the use of VTT terminations.

Figure 14: Vref Supply with Discrete Components

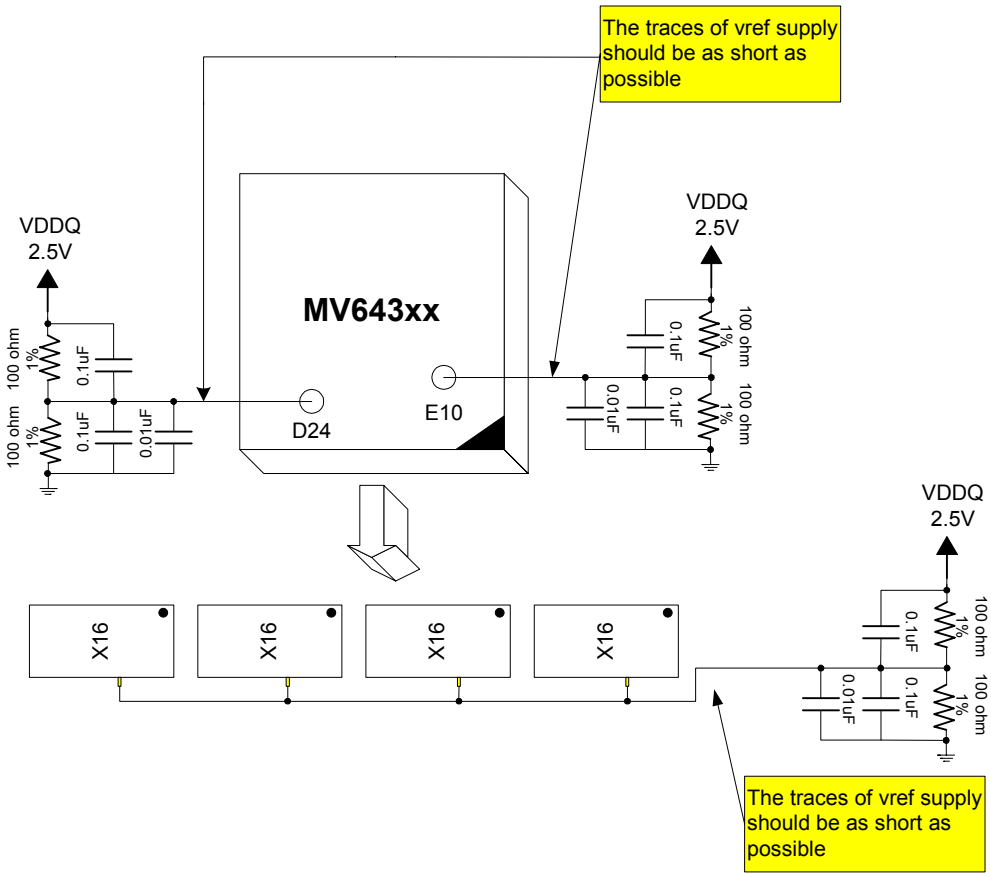
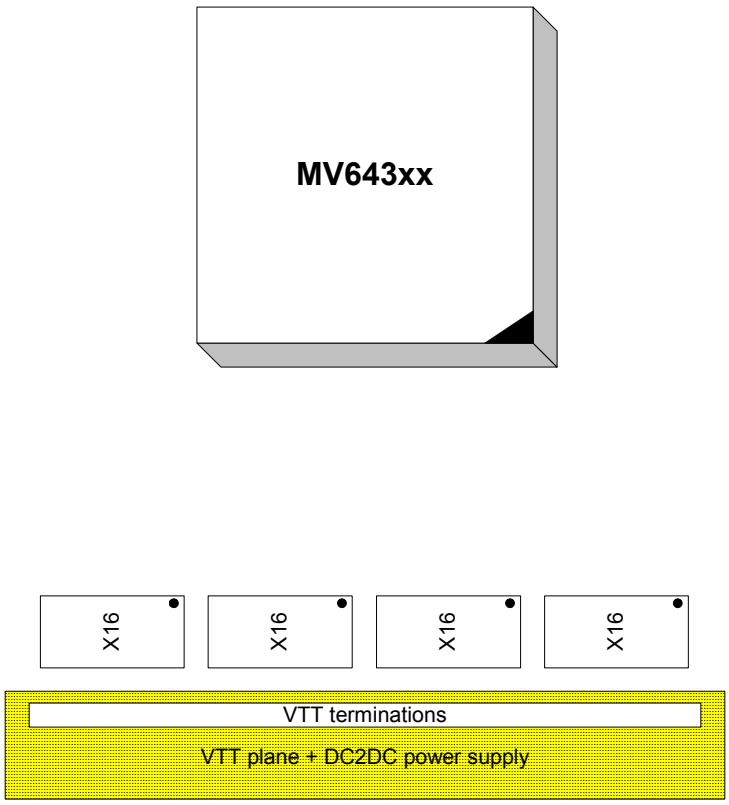


Figure 15: Vref Supply with Discrete Components



2.9.2 DDR Signals Length in Sync and Async Modes

The DDR signal length is calculated according to the MV643xx timing. Thus the same calculations are applicable in the DDR SDRAM discrete design. For further information see Section 2.3.1 "Sync Mode" or Section 2.3.2 "Async Mode", according to your preferred mode.

2.9.3 Routing Topology

As mentioned in Section 2.3.1 "Sync Mode" and Section 2.3.2 "Async Mode", all DDR signals should be the same length. Therefore the DDR signals must be routed in a star topology. For example, if according to the calculation, DDR signals length is 5", according to Section 2.9.2 "DDR Signals Length in Sync and Async Modes", the routing will resemble Figure 16 and Figure 17.

Figure 16: Discrete DDR SDRAM Star Topology for DQ and DQS Signals

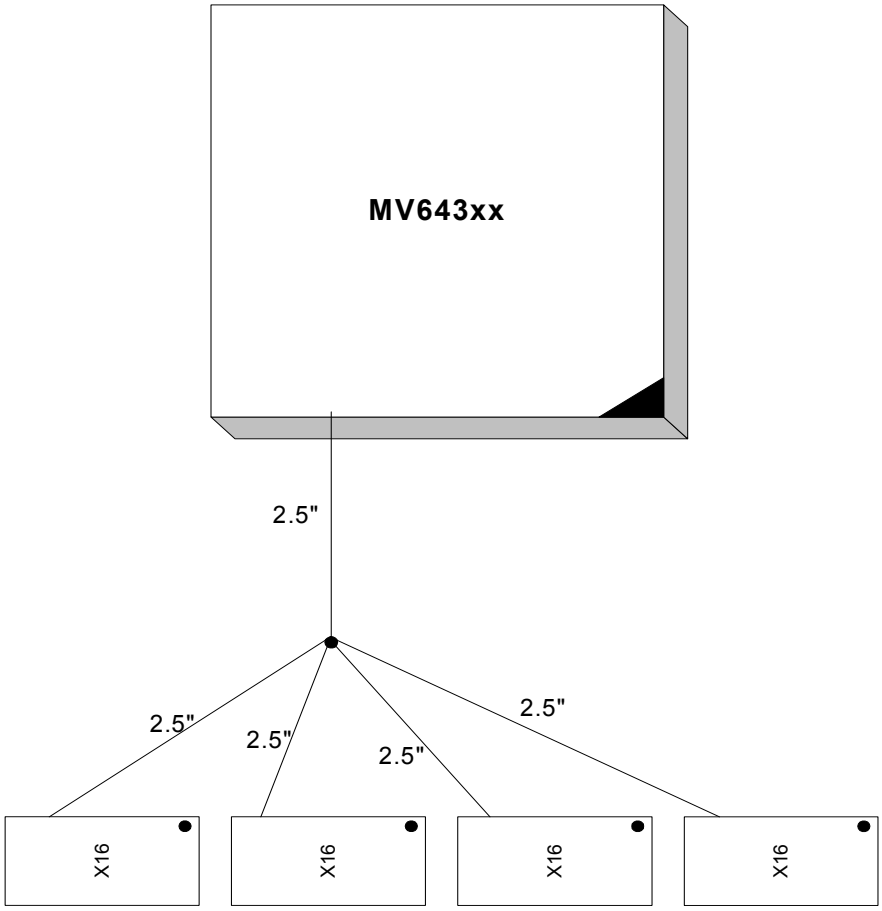
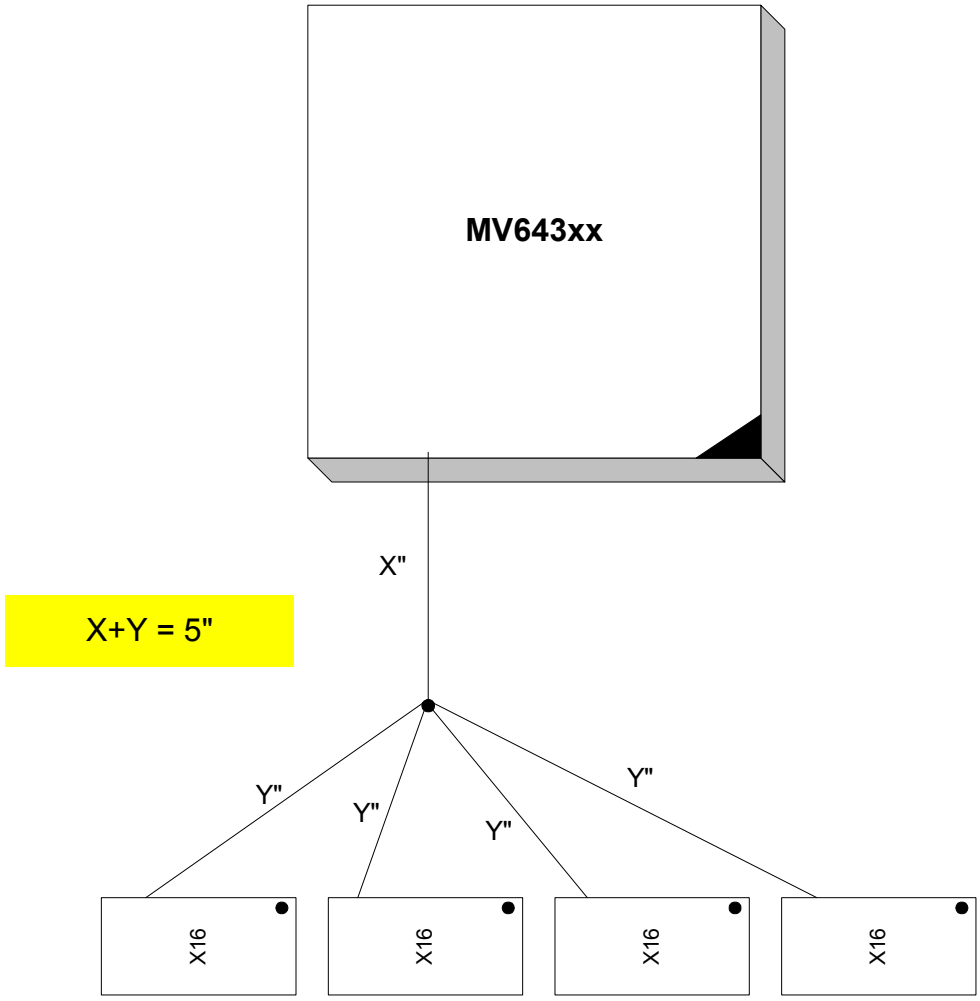


Figure 17: Discrete DDR SDRAM Star Topology for Address/Control Signals



2.9.4 Address/Control Signals Considerations

Background

According to the JEDEC requirements the Address/Control signals must be skewed from the clock signal. For example, DIMM JEDEC specification for

4.20.5 - 184 PIN PC1600/2100 DDR SDRAM UNBUFFERED DIMM DESIGN SPECIFICATION.

Figure 18 is the clock length inside the DIMM, as specified in the JEDEC DDR SDRAM DIMM.
The minimum clock length allowed is TL0+TL1+TL2+TL3 = 1.68".

Figure 19 is the net structure routing for Address and Control, as specified in the JEDEC DDR SDRAM DIMM.
The maximum Address/Control length allowed is TL0+TL2+TL3+TL4+TL5 = 7.67".

Therefore the skew (in inches) between Address/Control and the Clock is: 7.67"-1.68" = 5.99"

There are two options to implement the skew, which essential for timing:

1. Route the Address/Control signals with the necessary skew, according to the JEDEC specification.

Note

The skew between the Address/Control to the clock is not fixed. In the JEDEC specification, there are three topologies: Row A, Row B, or Row C, depending on the number of components being placed on the PCB DIMM. To determine the exact skew, see the JEDEC specification.

2. The MV64360 drives the Address/Control signals on the negative edge clock instead of the positive edge clock. With this simple support, the timing needed to compensate for the skew between the Address/Control and the Clock is achieved. Driving the Address/Control in the negative edge clock is set by a sample at reset DevAD[19]:
   0 = DRAM Address/Control signals toggle on falling edge of DRAM clock.
   1 = DRAM Address/Control signals toggle on rising edge of DRAM clock.
   For further details see the Reset Configuration section of the datasheet.

Note

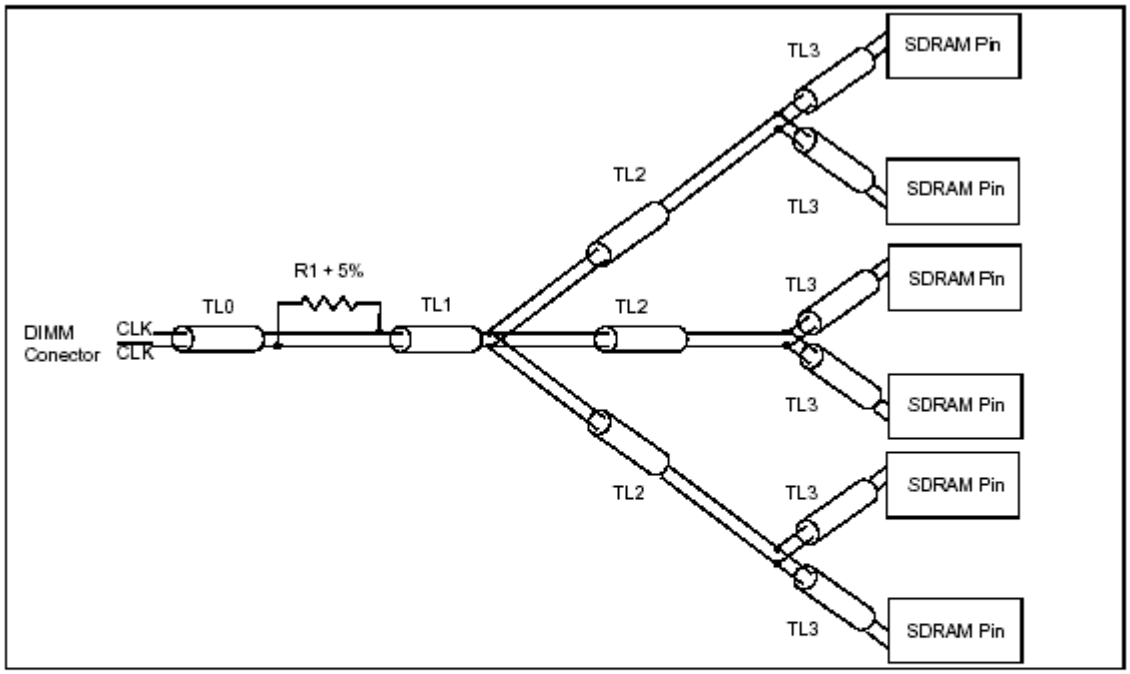
The second solution (working with Address/Control driven on the negedge clock) is applicable to133 MHz and up to10 DDR SDRAM components. When working with more than 10 components or with higher frequency, the first option should be used, i.e., design the length and skew as if you are designing a DDR DIMM PCB. It this case it is highly recommended to check with 4.20.5 – 184 PIN PC1600/2100 DDR SDRAM UNBUFFERED DIMM DESIGN SPECIFICATION and design your routing according to one of the three topologies suggested in the JEDEC. (Each of the suggested topologies is determined according to the number of components with which you wish to use it with.)

2.9.5 Clock Buffer

According to JEDEC specifications, each SSTL_2 clock (CK/CK#) should be driven to 6 loads. Figure 20 shows the Logical Clock Net Structure, as implemented on DDR DIMM PCB. Therefore, when using more than 6 DDR SDRAM components, you must use a clock buffer. Otherwise you must use the CK/CK# clock outputs, which are driven from the MV64360 and follow JEDEC recommendations, as shown in Figure 20.

Figure 18: Clock length inside the DIMM

Net Structure Routing for Clocks



Trace Lengths for Clock Net Structures

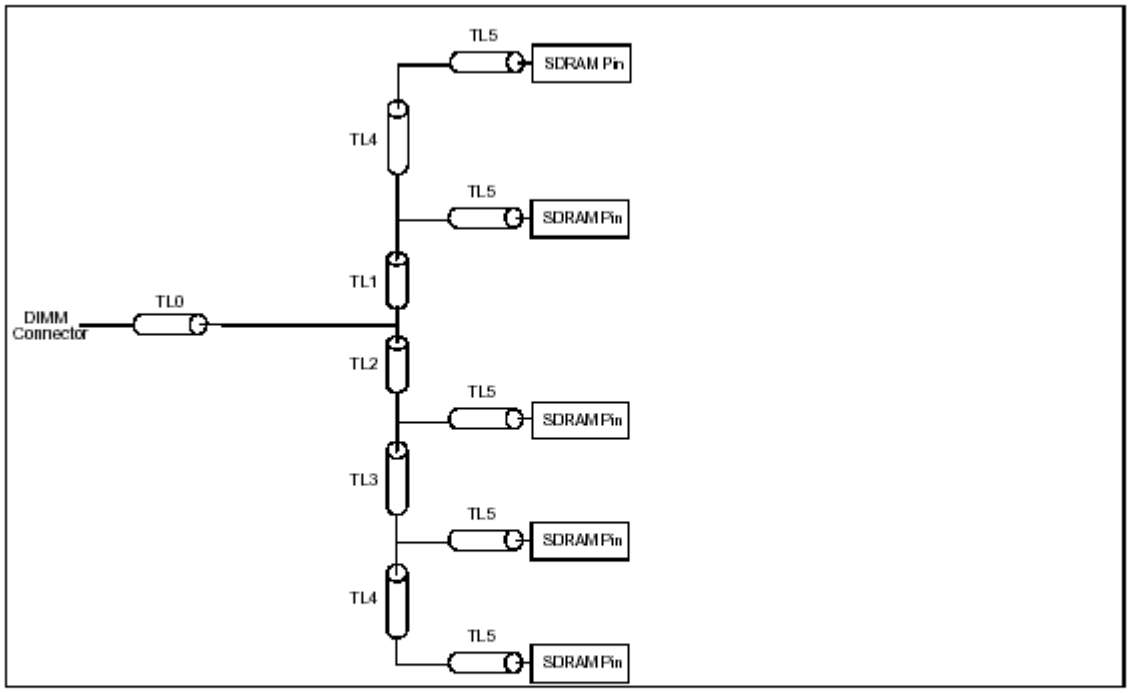
Raw Card	TL0		TL1		TL2		TL3		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
A,B	.15	.16	.04	.05	1.13	1.14	.36	.37	120	1,2
C	.15	.16	.04	.05	1.13	1.14	.36	.37	120	1,2

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch
2. Logical clock structures on page 15 must be followed. In some cases the loads will be equivalent capacitors.

Figure 19: Address and Control Length Inside the DIMM

Net Structure Routing for Address and Control (Raw Card Version C)

A, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ for Raw Card Version C

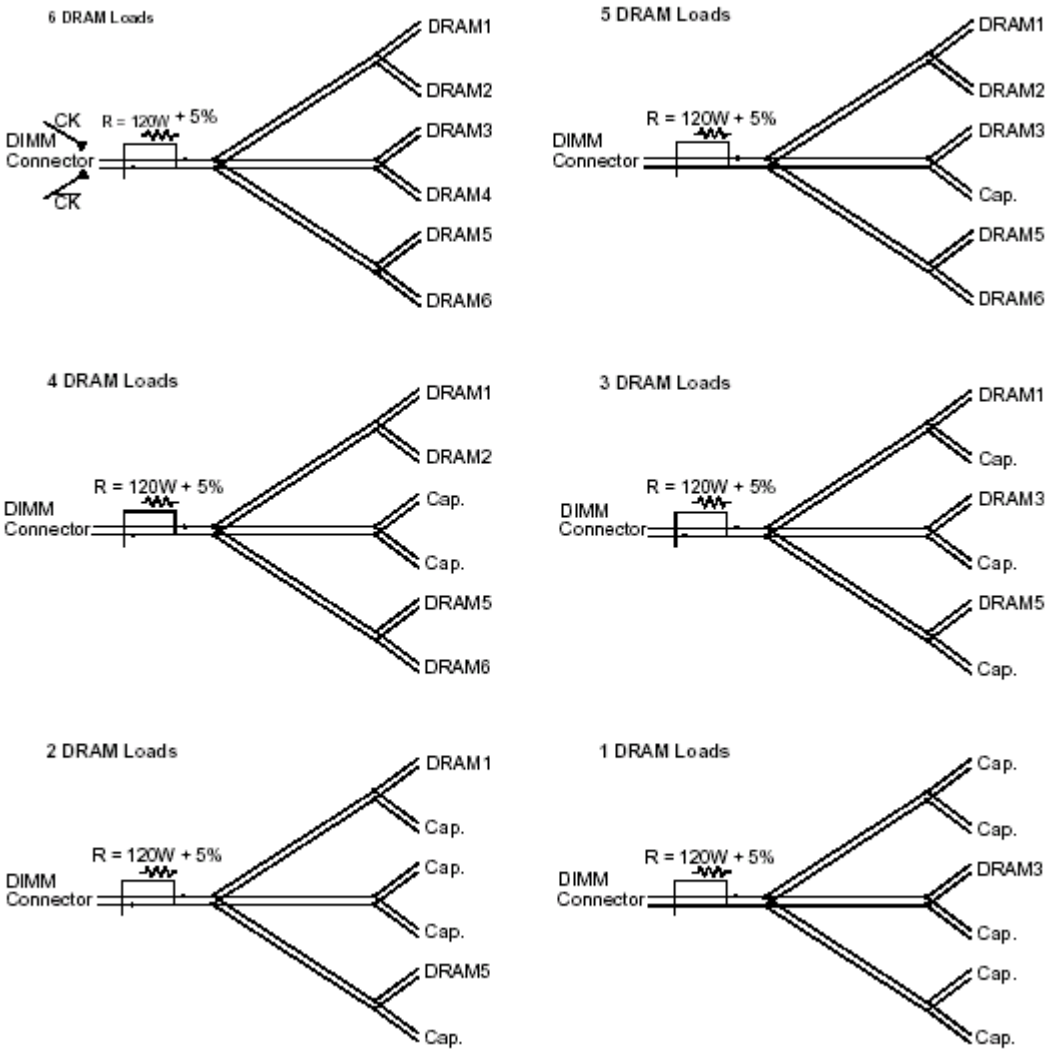


Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	5.58	5.75	.91	.92	.29	.30	.62	.63	.84	.85	.07	.14	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Figure 20: Logical Clock Net Structure



Cap. = 1/2 DDR SDRAM input capacitance

3. Software Settings

3.1 Register Settings on the DB643x0

In the basic monitor supplied with the development board, the following DDR registers must be configured as follows, when using registered or non-registered DDR SDRAM DIMM.

3.1.1 Non-Registered DDR SDRAM DIMM

- SDRAM configuration (0x1400) = 0x58200400
- SDRAM timing high (0x140C) = 0x9
- Open Pages (0x1414) = 0x0 (All open)
- The software reads the Two-Wire Serial Interface (TWSI) of the DDR to find the minimum CAS Latency (CL) it supports and configures the system to this latency. In addition, the software checks the mode of operation (Sync or Async mode), according to <ClkSync> bit [0] in Dunit Control (Low). Because it affects the settings for the different CL's, the lower bits of the Dunit Control (Low) are sampled at reset.

Table 8: Non-Registered DDR SDRAM DIMM Register Settings

CAS Latency	Sync Mode	Async Mode
1.5	0x141C = 0x52 0x1404 = 0x23110051	0x141C = 0x52 0x1404 = 0x1A1107d2
2	0x141C = 0x22 0x1404 = 0x03110051	0x141C = 0x22 0x1404 = 0x3B1107d2
2.5	0x141C = 0x62 0x1404 = 0x24110051	0x141C = 0x62 0x1404 = 0x1B1107d2
3	0x141C = 0x32 0x1404 = 0x24110051	0x141C = 0x32 0x1404 = 0x3C1107d2

- Set the DDR density setting according to the Information from the DDR TWSI:
  - 64–128 Mb: DDR_ADDRESS_CONTROL (0x1410) = 0x2
  - 256–512 Mb: DDR_ADDRESS_CONTROL (0x1410) = 0x12
  - 1–2 Gb: DDR_ADDRESS_CONTROL (0x1410) = 0x22
- SDRAM_TIMING_CONTROL_LOW (0x1408) = 0x11511220 (for 133 MHz)

3.1.2 Registered DDR SDRAM DIMM

Table 9: Registered DDR SDRAM DIMM Register Settings

CAS Latency	Sync Mode	Async Mode
1.5	0x141C = 0x52 0x1404 = 0x24110051	0x141C = 0x52 0x1404 = TBD
2	0x141C = 0x22 0x1404 = 0x04110051	0x141C = 0x22 0x1404 = TBD
2.5	0x141C = 0x62 0x1404 = 0x25110051	0x141C = 0x62 0x1404 = TBD
3	0x141C = 0x32 0x1404 = 0x05110051	0x141C = 0x32 0x1404 = 0x2C1107F2

Following are the register settings when using 133 MHz register DIMMs:

- SDRAM configuration (0x1400) = 0x58320400
- SDRAM timing low (0x1408) = 0x11511220
- SDRAM timing high (0x140c) = 0x9
- SDRAM Address Control (0x1410) = 0x12
- SDRAM Address Pads Control (0x14c0) = 0x7D5014A
- SDRAM Data Pads Calibration (0x14c4) = 0x7D5014A

3.2 DFCDL Delays

The DDR interface unit incorporates Delay Lines (DFCDLs) for three different purposes:

- Delay of the incoming DQS for DQs capture in read-cycle.
- Delay of the outgoing DQs related to DQS in write-cycle.
- Delay of the clock that syncs the unpacked data (128 bit). (Optional)

After the system is reset, the DFCDL must be initiated each time, by writing to the DFCDL SRAM. The entry of the SRAM is divided into three, 6-bit fields. Each field is used for a different DFCDL function.

31 24	23 18	17 12	11 6	5 0
Reserved	Delay of the FBCLKIN (Async mode) or the Core Clock (Sync mode).	Reserved	Delay of the outgoing DQ's.	Delay of the incoming DQS's.

Note

The following DFCDL values are for 133 MHz frequency. Other frequencies require different DFCDL values.

To initialize the DFCDL, the following steps must be completed:

1. Execute 64 consecutive writes to SRAM Data0 register (Offset: 0x1494). Due to AC timing analysis for 133 MHz, the DFCDL delays for incoming DQSs and outgoing DQs are configured to a quarter cycle. The DFCDL for FBCLKIN is not used, thus it does not need to be initialized.

For the above conditions, the 64 consecutive data writes are:

Table 10: 64 Consecutive Data Writes to SRAM Data0 Register - 133 MHz Sync Mode

Writes 0–7	Writes 8–15	Writes 16–23	Writes 24–31	Writes 32–39	Writes 40–47	Writes 48–55	Writes 56–63
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F
32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F	32'H0000014F

2. After initialization of DFCDL SRAM, write 0x00300000 to DFCDL Configuration0 register (Offset: 0x1480) to enable dynamic delay line updating. Basically, this write resets `<BlockUpd>` bit [15]. All other bits are left in their default value.

Appendix A. Revision History

Table 11: Revision History

Document Type	Revision	Date
Initial release.	A	March 9, 2003
Release	B	May 29, 2003
Modifications were made in: 1. Both AC timing tables (Table 1 and Table 2): DQ[63:0], CB[7:0], DM[8:0] tDIPW (Data output pulse width) was changed to 2.3 ns from 1.25 ns. 2. Section 2.3.1 "Sync Mode" and Section 2.3.2 "Async Mode". Updated the TDdrClkDqs from 0.8 to +/- 0.8 and made additional changes. 3. Information was added, e.g., Figure 13, “Filtering Supply Routing,” on page 193. 3V filtering circuit requirements were updated. In addition, the units in the figure were changed from ml to mm. 4. Section 3.1.2 "Registered DDR SDRAM DIMM": D UNIT Control high and low registers values were removed from the list, since they are not required.		
Release	C	July 3, 2003
1. Added Section 2.9 "Designing with SDRAM DDR Discrete Components on Board" and Figure 14 to Figure 20.		

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