TECHNICAL BULLETIN

TB-102

Differences Between the Discovery III and Discovery II Devices for PowerPC CPUs

1. Introduction

The Discovery III is the newest member of the Marvell® Discovery™ family of system controllers. It introduces an additional upgrade both in performance and features that include:

- Process 0.15 (1.5V core voltage).
- CPU bus frequency of up to 200 MHz.
- Reduced CPU to DRAM latency.
- Supports the Fujitsu's Fast Cycle RAM (FCRAM) DDR SDRAM.
- Improves DRAM cache coherency performance.
- New XOR engine for Redundant Array of Independent Disks (RAID) applications.
- Gigabit Ethernet (GbE) ports support RGMII interface, enabling the utilization of all three ports, while still having two 64-bit PCI interfaces.
- Corrects Discovery II PCI ordering issues.
- Each gigabit port can also work as an 8/16-bit synchronous FIFO interface, for easy connection to user specific logic.
- Internal data path parity protection.
- PowerPC Big/Little Endian support.
- ECC protection on internal SRAM.

2. Pinout Changes

The Discovery III is NOT pin compatible to the Discovery II device. In addition, the following changes have been implemented:

- Due to the change of process, the core voltage is reduced to 1.5V, instead of 1.8V. The Core VCC pins are the same as in the Discovery II.
- The CPU interface can run up to 200 MHz, yet the rest of the system's maximum frequency is 133 MHz. For this reason, an additional clock pin is needed. This means the Discovery III uses a dedicated clock for the CPU and DDR interfaces, called SysClk (up to 200 MHz), and a core clock, called Tclk (up to 133 MHz). The Discovery II device only uses SysClk.
- The Discovery III package is a 805 PBGA.

3. CPU Bus Frequency

As CPU core frequencies are getting higher and higher (~1 GHz), bus frequencies are also being pushed to frequencies much higher than 133 MHz. The Discovery III CPU interface is targeted to 200 MHz.

Note

The 200 MHz is targeted to a point-to-point configuration (a single CPU interfacing a single Discovery III device). For other configurations, this frequency may not be achievable.

The Discovery III supports two clocking modes:

- The CPU and DRAM interfaces are running with the same clock (SysClk), up to 200 MHz.
- The rest of the chip is running with a separate core clock (TClk), up to 133 MHz.

4. CPU-to-DRAM Latency

In typical applications, the CPU-to-DRAM access is very latency sensitive, while the IO access to DRAM is more throughput sensitive. To satisfy both sensitivities, the Discovery III design minimizes CPU-to-DRAM latency, while maintaining the high DRAM throughput for the IO.

The Discovery III reduces CPU-to-DRAM read latency by four cycles, compared to Discovery II. This is achieved by a new, dedicated fast path between the CPU and DRAM interface.

Since the rest of the chip is running at the TClk clock domain frequency, a CPU access to other interfaces (e.g., PCI) goes through synchronization logic. Similarly, any IO access to DRAM (e.g., PCI-to-DRAM) goes through synchronization logic.

Note

The synchronization logic on the IO path to DRAM, does not affect DRAM throughput, since the design is fully pipelined. The integrated 2 Mb SRAM runs at the SysClk frequency. A CPU access to SRAM does not go through synchronization logic.

5. Fast Cycle RAM

In parallel to the JEDEC standard DDR DRAM devices, some DRAM vendors have developed alternative DRAM technologies that allow for better performance for random accesses. For instance, one of these technologies is the new, FCRAM technology.

In addition to the standard JEDEC DDR DRAM, the Discovery III DRAM controller supports FCRAM. It supports 256 Mb devices (by Fujitsu, Toshiba and Samsung) in x8 and x16 configurations.

6. PowerPC Little Endian Mode Support

The Discovery III PowerPC Little Endian mode is different than the conventional Little Endian mode. The PowerPC CPU performs address manipulation (munging) on the three least significant bits of the address. If the CPU Configuration register's AMung bit is set to '1', the Discovery III performs address munging before driving the transaction to the target interface (internal registers, DRAM, PCI etc.).

7. Cache Coherency

The cache coherency implementation requires generation of a snoop transaction on the CPU bus, per each cache line (32 bytes). This means that long burst accesses to cache coherent memory must be cut to multiple cache line accesses. This results in low efficiency of the DRAM interface – DDR DRAM is especially effective in long burst accesses.

The Discovery II implementation requires that the transaction originator cuts the burst to a 32 byte access. For example, a 128 byte access from PCI-to-DRAM must be split up by the Discovery II PCI slave into four 32 byte transactions.

Although there is no deed in the Discovery III to split the read transactions, write transactions must be split in the initiator unit by setting the write MBurst to 32 bytes. The DRAM controller automatically generates multiple snoop requests, per each transaction (four snoop requests for the above example). Once all of the snoop transactions are resolved, it accesses the DRAM with one long burst (128 byte for the above example).

8. XOR Engine

RAID applications require XOR operations between multiple disc sectors. Typically, the XOR operation was performed by software or by external hardware (e.g., FPGA seating on Discovery II device bus). The Discovery III integrates this functionality.

The Discovery III contains two independent DMA engines, in addition to the Discovery II four IDMA channels. Each DMA is working with a link list of descriptors. Each descriptor indicates the size of the block to be manipulated, the addresses of up to eight sources, and the destination address. The DMA reads data from the sources, performs bitwise XOR, and writes the result to the destination.

9. Reduced GMII

The Discovery II GbE interface supports GMII and TBI interfaces, at 25-bits wide. To utilize all three Discovery II GE ports, it is necessary to sacrifice the upper side of PCI_1 interface (PCI_1 becomes a 32-bit interface).

The new Marvell Gigabit Ethernet PHYs support a Reduced GMII (RGMII) 12-bit interface. The Discovery III supports RGMII (in addition to GMII and TBI). This enables utilizing all three GE ports while still having two 64-bit PCI interfaces and two RGMII + 8-bit FIFO interface configurations, see Figure 1.

Figure 2 shows the Discover III configured for GMII.

Note

For additional configurations and mixtures of the FIFO/GbE/PCI interfaces, see Section 12. "FIFO Interface", on page 5.

Figure 1: Discovery III RGMII with 8-bit FIFO Configuration

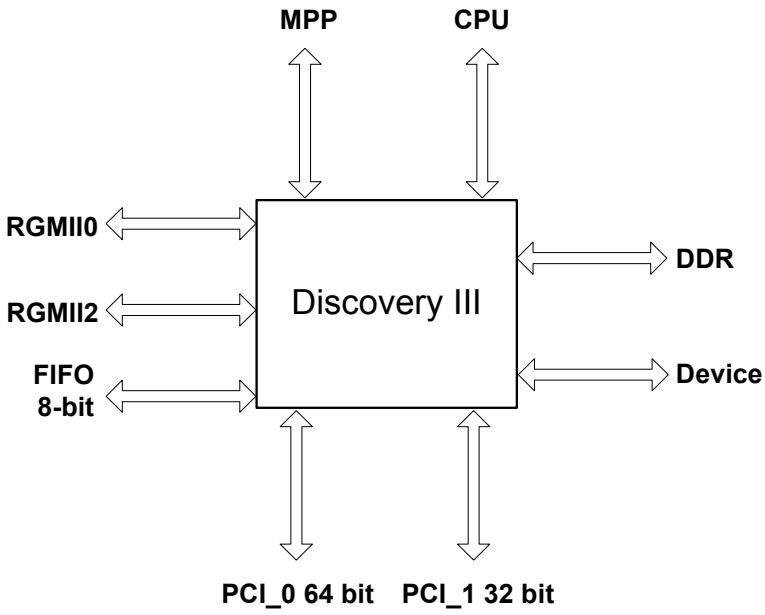
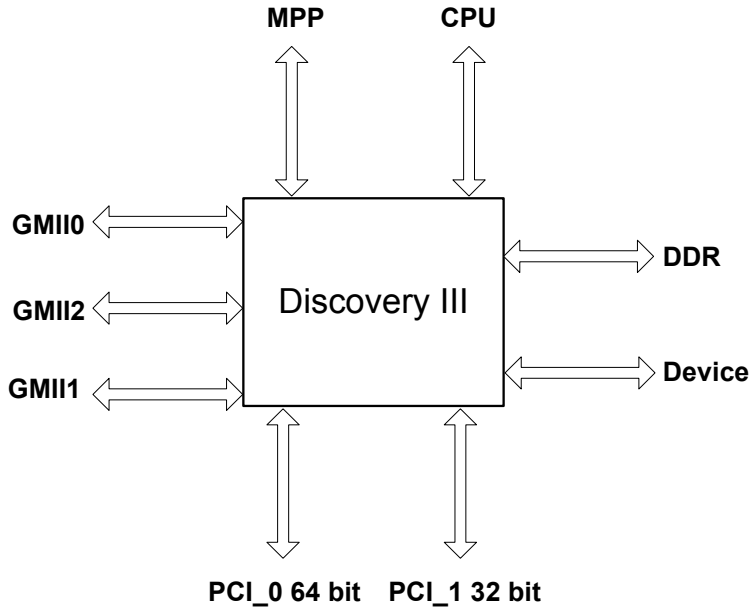


Figure 2: Discovery III with GMII Configuration



10. PCI Interface

- The Discovery II PCI master supports only a cache line size of 0x8 (32 bytes). The Discovery III PCI master supports the following cache line sizes: 0x4 (16 bytes); 0x8 (32 bytes); 0x10 (64 bytes); 0x20 (128 bytes). It's only relevance to the PCI2.2 specification determines what type of command to issue on the bus.
- In PCI2.2 mode, the Discovery III master supports the issue of a second read when the first one is terminated by a target with RETRY
- The Discovery III implements new sync barrier mechanisms to both PCI master and slave, in addition to the Discovery II mechanisms.
- The PCI Configuration registers are preset to their default value when moving from D3 to D0 power states.
- There is improved new data path parity protection (new error bit DPErr).
- Corrected PCI 2.2 specification compliance issues that existed in Discovery II.

11. PCI Ordering

The PCI specification defines bridge ordering rules that guarantee proper operation of the producer/consumer model. The Discovery II supports these ordering rules via it's sync barrier mechanism. However, it is best if the sync barrier is activated by the software.

The Discovery III supports PCI bridge ordering rules by hardware, transparent to the software.

Note

For full details on PCI ordering implementation in Discovery family, see *AN-84: PCI Ordering Implementation* and *AN-85: PCI Deadlock Considerations*.

12. FIFO Interface

In many applications, user proprietary logic requires a high throughput access to memory. Typically this logic is placed on the PCI, device, or the 60x bus. These interfaces are often inconvenient to deal with. The Discovery III introduces an alternative simple synchronous FIFO interface.

Each of the three GE ports can be configured to work as a FIFO interface. As such, the port is still working with a chain list of descriptors (same as in the case of Gb Ethernet port). However, it no longer works with the Ethernet header, does not perform address filtering, but simply receive/transmits the packet data on a simple 8 or 16-bit interface.

The interface runs at up to 133 MHz. It also implements a simple flow control mechanism that enables the Rx and Tx sides to "back pressure" traffic, when the FIFO becomes full.

The Discovery III supports several configurations and mixtures of the FIFO/Gb Ethernet/PCI interfaces such as:

- Three GE ports (GMII): The third port is muxed on the PCI_1 pins, meaning PCI_1 becomes 32-bit.
- Three GE ports (RGMII): Both PCI interfaces are 64-bit.
- Three 8-bit FIFO interfaces: The third port is muxed on the PCI_1 pins.
- Two GE ports (RGMII) + one 8-bit FIFO interface: Both PCI interfaces are 64-bit.
- Single 16-bit FIFO interface + one GE port (GMII) muxed on the PCI_1 pins.

13. Internal Data Path Parity

Systems and chips are basically exposed to two types of errors - hard and soft errors. The traditional parity protection on the interfaces is sufficient for detecting hard failures. However, this parity protection is not enough for detection of soft errors in memory arrays.

The Discovery II device, already supports ECC on the DRAM, and parity protection on it’s integrated SRAM.

In the Discovery III, the integrated SRAM is ECC protected. More over, all data path buffers are parity protected (bit per entire buffer entry). Parity is generated per each data on the input side and checked when pulled out of the buffer.

Note

Since soft errors are typically single bit errors, parity protection per the entire buffer entry is acceptable.

14. Reset Strapping

Discovery III reset strapping is slightly different than the Discovery II. The Discovery III uses the same signals but some of the reset strapping has different functionality. See the Discovery II data sheet for more information.

15. Additional Feature Support

In addition to the previously described improvements, the Discovery III also supports the following features:

- Single bit ECC error repair: The XOR DMA can periodically scan the entire DRAM space, or sections of it, and fix single bit errors.
- Memory initialization: The XOR DMA can initialize a memory window with a fixed data value. This feature is useful for DRAM and SRAM initialization.
- CRC-32 generation: The XOR DMA can calculate CRC-32 on a memory buffer, and append the result to the end of the buffer.
- Improved multi-GT AC timing.
- Bank interleaving as in Discovery I (two transactions).
- There is a new configuration bit that disables ECC checking, while still allowing ECC generation. This is an easier method for initializing DRAM. A partial write to non-initialized DRAM causes a read of junk data with bad ECC and a write back of the new data with good ECC.

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