TECHNICAL BULLETIN

TB-112

Differences Between the MV6436x Stepping A2 and B0

Introduction

This technical bulletin summarizes the differences between the MV6436x-A2 and MV6436x-B0 devices.

Note

For further information about the MV6436x features, refer to the *MV6436x Datasheet* (Doc. No. MV-S100614-00)

Errata Fixes

The following shows the MV6436x errata that are corrected in the B0 stepping of the device.

Note

For the latest MV6436x errata and restrictions document, see *MV64360 Functional Errata and Restrictions* (Doc. No. MV-S300193-00).

Errata	Stepping A2	Stepping B0
FEr CPU-#3 Wrong swapping indication on CPU accesses to the PCI interface register.	Exist	Fixed
FEr CPU-#4 Incorrect data is stored when using AltiVec operands at address offset 0x10.	Exist	Fixed
FEr ETH-#5 Gigabit Ethernet port hangs on LLC/SNAP or jumbo frames.	Exist	Fixed
FEr MISC-#3 The MV6436x is not fully compliant with the PCI HotSwap plug-in electrical specification.	Exist	Fixed

New or Updated Features and Device Changes

This table summarizes the MV6436x new/updated features and changes to the device that are implemented in the B0 stepping.

Features/Changes	MV6436x Rev A2	MV6436x Rev B0
ESD performance	The ESD HBM sensitivity is defined as "Class 1B" per JEDEC Standard no. 22-A114-B, Section 6.	The target is to bring the ESD HBM sensitivity as defined by JEDEC Standard no. 22-A114-B, Section 6. (Will be tested when the device is available).

Features/Changes	MV6436x Rev A2	MV6436x Rev B0
Add Crossbar to DDR interface new arbitration mode	The crossbar contains programmable arbitration mechanisms to optimize the performance of accesses to the DDR interface, according to the system requirements. For more information, see the MV6436x datasheet.	The default configuration for the crossbar to DDR interface arbitration is the same as the A2 stepping. However, when bit [0] in PUnit MMask Register (offset 0x3E4) is set to '1', one of the crossbar paths to the DDR interface unit is dedicated for CPU to DDR interface transactions. The other crossbar path to the DDR interface is shared by all other interfaces. In this configuration the Pizza arbiter is applicable only to the second path and all the CPU slices will be considered as NULL. The following sequence must be used to set this bit: 1. The code is must run outside of the DDR SDRAM (e.g. from boot device). 2. No interface UNIT can access the DDR interface, e.g. PCI, IDMA, GE etc. 3. In the PUnit MMask Register, set bit 0 to '1'. 4. Read the register value back and make sure that bit 0 was set to '1'.
JTAG rev ID update	The JTAG ID register value is: "0001" & -- Version Number "0100001101100000" & -- Part Number "00010101011" & -- Manufacturer ID "1"; -- Required by IEEE Std. 1149.1-1990	The JTAG ID register value is: "0010" & -- Version Number "0100001101100000" & -- Part Number "00010101011" & -- Manufacturer ID "1"; -- Required by IEEE Std. 1149.1-1990
PCI rev ID update	The RevID bits [7:0] in the PCI Class Code and Revision ID register and the PCI Configuration Register is: 0x2	The RevID in the PCI Class Code and Revision ID PCI Configuration Register is: 0x3
Write DQS preamble	Most DDR SDRAM devices require DQS write preamble (t_{WPRE}) of 25%. Only a few of these devices them require t_{WPRE} of 30%. The MV6436x write preamble is 32% for 133 MHz and 27% for 183 MHz.	The MV6436x write preamble is 40% for 133 MHz and 37% for 183 MHz.
DLL power supplies in the PCI interface.	The MV6436x PCI DLL power pins are connected internally in the device to the internal core voltage (V_{DD}Core).	The MV6436x PCI DLL power pins are connected to the external PAVDD and PAVSS pins. The same recommended filtering circuit on these signals is required for the A1 and B0 revisions.

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