Quick Guide to Common Flash Interface

Application Note

By: Frank Cirimele

1. Introduction

Common Flash Interface, or CFI, is a standard introduced by the Joint Electron Device Engineering Council (JEDEC) to allow in-system or programmer reading of Flash device characteristics, which is equivalent to having data sheet parameters located in the device. The JEDEC Solid State Technology Association defines industry standards for semiconductor devices, with CFI being one of many. The CFI is used to standardize Flash device characteristics and to define feature differences between various Flash manufacturers. For a detailed definition of CFI, please refer to the JEDEC CFI publications JEP137 and JESD68. The Spansion® application note “Common Flash Interface Version 1.4 Vendor Specific Extensions” provides an overview of versions 1.3 and 1.4 CFI implementations, with v 1.3 covering Addresses 10h - 50h and v 1.4 beyond Address 50h.

2. Common Flash Interface

CFI is a way of defining the Flash device characteristics in silicon. It is implemented in a set of tables, which define the various characteristics of the Flash device that application software can interrogate. The CFI tables are divided into five separate parts, consisting of the “CFI Query Identification String”, “System Interface String”, “Device Geometry Definition”, “Primary Vendor-Specific Extended Query”, and “Alternate Vendor-Specific Extended Query” table sections.

The “CFI Query Identification String”, “System Interface String”, and “Device Geometry Definition” table descriptions are identical for all Flash manufacturers. The “Primary Vendor-Specific Extended Query” and “Alternate Vendor-Specific Extended Query” table sections allow Flash manufacturers to indicate unique features. Spansion has not included the “Alternate Vendor-Specific Extended Query” table section in its current CFI definitions.

CFI addressing depends on the device and its mode of operation. For x8-only device, x16-only device, x32-only device, x8/x16 capable device operating in the x16-mode, or x16/x32 capable device operating in the x32 mode, byte addressing starts at 10h and is incremented by a factor of one. For x8/x16 capable device operating in the x8-mode or x16/x32 capable device operating in the x16-mode, word addressing starts at 20h and is incremented by a factor of two. For x8/x32 capable device operating in the x8-mode, double-word addressing starts at 40h and is incremented by a factor of four.

CFI addressing in the following examples will be shown with the maximum data bus width, which means x32 or x16/x32 capable device in x32-mode, x16 or x8/x16 capable device in x16-mode, and x8 device in x8-mode. The CFI codes were taken from various Flash devices and do not represent individual devices.

3. CFI Tables

3.1 CFI Query Identification String

The “CFI Query Identification String” table starts from Flash device physical address 10h and ends at 1Ah.

Addresses 10h to 12h define the ASCII string “QRY” that is used in “Query Structure Output” to indicate the Flash device bus width and its bus mode.

Table 3.1 Query Structure Output

Address	Data (x8)	Data (x16)	Definition
10h	51h	0051h	'Q' in ASCII
11h	52h	0052h	'R' in ASCII
12h	59h	0059h	'Y' in ASCII

Addresses 13h and 14h define the Flash manufacturer identification number, or the “Primary Vendor Command Set and Control Interface ID Code”. The Spansion Manufacturer ID for Flash devices is 0002h (historically the AMD ID was 0002h and the Fujitsu ID was 0004h).

In the CFI tables, lower and upper bytes are assigned to consecutive addresses whenever a definition can have a 16-bit data value. For example, the Manufacturer ID data value is 0002h. For the x8 case, the lower data byte is 02h at Address 13h and the upper data byte is 00h at Address 14h. For the x16 case, the data values are the same, but 00h has been added as the high byte to each data value.

Table 3.2 Primary Vendor Command Set and Control Interface ID Code

Address	Data (x8)	Data (x16)	Definition
13h	02h	0002h	Manufacturer ID Lower Byte
14h	00h	0000h	Manufacturer ID Upper Byte

Addresses 15h and 16h define the starting address of the “Primary Vendor-Specific Extended Query” table. The starting address for the “Primary Vendor-Specific Extended Query” table starts at address 40h for Spansion products, whereas it may start at address 31h for other manufacturers.

Table 3.3 Primary Vendor-Specific Extended Query

Address	Data (x8)	Data (x16)	Definition
15h	40h	0040h	Starting Address for “Primary Vendor-Specific Extended Query” table Lower Byte
16h	00h	0000h	Starting Address for “Primary Vendor-Specific Extended Query” table Upper Byte

Addresses 17h and 18h define the alternate Flash manufacturer identification number, or the “Alternate Vendor Command Set and Control Interface ID Code”. Spansion does not currently implement this feature.

Table 3.4 Alternate Vendor Command Set and Control Interface ID Code

Address	Data	Definition
17h	00h	Alternate Manufacturer ID Lower Byte
18h	00h	Alternate Manufacturer ID Upper Byte

Addresses 19h and 1Ah define the starting address of the “Alternate Vendor-Specific Extended Query” table. Spansion does not currently implement this feature.

Table 3.5 Alternate Vendor-Specific Extended Query

Address	Data	Definition
19h	00h	Starting Address for “Alternate Vendor-Specific Extended Query” table Lower Byte
1Ah	00h	Starting Address for “Alternate Vendor-Specific Extended Query” table Upper Byte

3.2 System Interface String

The “System Interface String” table starts from Flash device physical address 1Bh and ends at 26h.

Addresses 1Bh and 1Ch define the Power Supply Voltage (V_{CC}) minimum and maximum limits. Please note that when rounding the V_{CC}, the lower limit (address 1Bh) should always be rounded up and the higher limit (address 1Ch) should always be rounded down.

Table 3.6 Power Supply Voltage

Address	Data	Definition
1Bh	27h	27 / 10 = 2.7 volts V_{CC} lower limit (D7-D4: volts, D3-D0: 100 millivolts)
1Ch	36h	36 / 10 = 3.6 volts V_{CC} upper limit (D7-D4: volts, D3-D0: 100 millivolts)

Addresses 1Dh and 1Eh define the Dual Supply Programming Voltage (V_{PP}) minimum and maximum limits. This is only available on legacy devices since newer devices have migrated to single supply programming.

Table 3.7 Dual Supply Programming Voltage

Address	Data	Definition
1Dh	00h	V_{PP} lower limit (00h = no V_{PP} pin present)
1Eh	00h	V_{PP} upper limit (00h = no V_{PP} pin present)

Addresses 1Fh and 23h define the single byte/word programming typical and maximum timeout values in microseconds. Typical time = 2^N µs and maximum time = 2^N times typical.

.

Table 3.8 Single Byte/Word Programming

Address	Data	Definition
1Fh	07h	2^7 = 128 µs typical word programming time from Erase and Programming Performance table in data sheet
23h	01h	2^1 = 2 -> 2*128 µs = 256 µs maximum word programming time, which is the maximum programming time expected before a timeout is generated (rounded up)

Addresses 20h and 24h define the entire buffer programming typical and maximum timeout values in microseconds. Typical time = 2^N µs and maximum time = 2^N times typical.

Table 3.9 Buffer Programming Timeout Values

Address	Data	Definition
20h	07h	2^7 = 128 µs typical buffer programming time
24h	05h	2^5 = 32 -> 32*128 µs = 4096 µs maximum buffer programming time (rounded up)

Addresses 21h and 25h define the sector erase typical and maximum timeout values in milliseconds. Typical time = 2^N ms and maximum time = 2^N times typical.

Sector and block are equivalent names for the smallest erasable size in Spansion Flash memory. Boot sector Flash memory contains multiple sector sizes, but the Address 21h definition corresponds to the time to erase the largest sector size of the device.

Table 3.10 Sector Erase Timeout Values

Address	Data	Definition
21h	0Ah	2^{10} = 1024 ms typical sector erase time
25h	04h	2^4 = 16 -> 16*1024 ms = 16,384 ms maximum sector erase time (rounded up)

Addresses 22h and 26h define the chip erase typical and maximum timeout values in milliseconds. Typical time = 2^N ms and maximum time = 2^N times typical.

Table 3.11 Chip Erase Timeout Values

Address	Data	Definition
22h	4Fh	2^N ms typical chip erase time
26h	04h	2^N = N * typical chip erase time maximum chip erase time (rounded up)

3.3 Device Geometry Definition

The “Device Geometry Definition” table starts from Flash device physical address 27h and ends at 3Ch.

Address 27h defines the device density in bytes.

Table 3.12 Device Density

Address	Data	Definition
27h	17h	17h = 23 -> 2^{23} = 8 Mbytes

Addresses 28h and 29h define the Flash device data bus interface. It defines parallel NOR and SPI Flash interfaces. For parallel NOR, bits 0, 1, and 2 correspond to the bitwise switch used to define devices having a x8, x16 or x32 interface, as follows:

Bit0 – represents x8

Bit1 – represents x16

Bit2 – represents x32

For x8/x16 capable devices, Bit0 and Bit1 must be set. For parallel NOR interfaces, take the binary value minus one to obtain the actual CFI entry. For example, the bitwise pattern for x8/x16 is '011', subtracting 1 gives '010' (or 02h).

00h = x8 only interface

01h = x16 only interface

02h = x8/x16 interface

03h = x32 interface

Table 3.13 Data Bus Interface — Parallel NOR

Address	Data	Definition
28h	02h	x8/x16 interface Lower Byte
29h	00h	x8/x16 interface Upper Byte

For SPI serial Flash devices 04h = Single I/O SPI, 3-byte address

05h = Multi I/O SPI, 3-byte address

Table 3.14 Data Bus Interface — SPI Flash

Address	Data	Definition
28h	04h	SPI Flash interface Lower Byte
29h	00h	SPI Flash interface Upper Byte

Addresses 2Ah and 2Bh define the maximum number of bytes in a multi-byte write, which is equal to 2^N. 00h is indicated if multi-byte write feature not supported.

Table 3.15 Maximum Number of Bytes

Address	Data	Definition
2Ah	05h	2^5 = 32 bytes / Buffer Length Lower Byte
2Bh	00h	Buffer Length Upper Byte

Addresses 2Ch through 3Ch define the “Erase Block” regions of the Flash device. The information stored at these address locations indicate how the Flash memory map is organized.

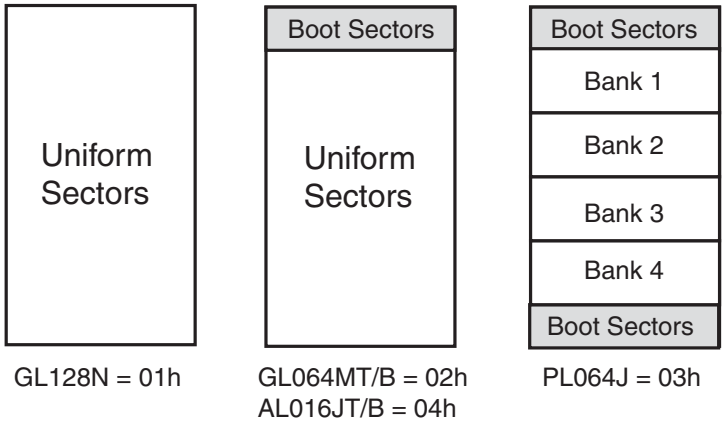
Address 2Ch defines the number of “Erase Block” regions within the Flash device.

Table 3.16 Number of Erase Block Regions

Address	Data	Definition
2Ch	01h	number of Erase Block regions

Figure 3.1 shows some examples of defining the number of erase block regions within Spansion Flash.

Figure 3.1 Examples of Erase Block Regions



Since the GL128N has only 128 Kbyte sectors in its memory array, there is only one “Erase Block” region. In the GL064MT/B, there are uniform 8 Kbyte boot sectors at the top or the bottom of the memory map with 64 Mbyte uniform sectors elsewhere. Thus we have two “Erase Block” regions. The AL016JT/B has four “Erase Block” regions, counted as one region of Uniform Sectors plus three regions in the Boot Sectors, due to mixed sector sizes among the Boot Sectors. The mixed sector regions, each counting as one “Erase Block” region, are:

- One 16 KW boot block sector region
- Two 4 KW boot block sector regions (count as one because the same size sector regions are contiguous)
- One 8 KW boot block sector region

In the PL064J, uniform 4 Kbyte boot sectors are located at both the top and bottom of the memory map, with uniform sectors in between. Thus we have three “Erase Block” regions.

Address 2Dh through 30h, 31h through 34h, 35h through 28h, and 39h through 3Ch defines the:

1. number of sectors and
2. sector density inside each “Erase Block” regions.

The lower two addresses specify the number of sectors and the upper two addresses specify its density.

For PL064J, the memory is configured into four banks: banks A through D. At both ends of the memory map, there are eight 8 Kbyte boot sectors. Besides the boot sectors located at the two ends of the memory map, there are 64 Kbyte uniform sectors sandwiched between the boot sectors through out the memory. The boot sectors at each end of the memory map can be classified as individual regions, while all uniform sections are another region. Therefore we end up with three regions, which include the first eight boot sectors, all of the uniform sectors, and then the second eight boot sectors.

Table 3.17 Region 1

Address	Data	Definition
2Dh	07h	07h = 07h + 01h = 8 / number of sectors Lower Byte
2Eh	00h	number of sectors Upper Byte
2Fh	20h	20h = 32 * 256 bytes = 8KB / density Lower Byte
30h	00h	density Upper Byte

Table 3.18 Region 2

Address	Data	Definition
31h	FDh	FDh = FDh + 01h = FEh = 254/ number of sectors Lower Byte
32h	00h	number of sectors Upper Byte
33h	00h	100h = 256 * 256 bytes = 64KB / density Lower Byte
34h	01h	density Upper Byte

Table 3.19 Region 3

Address	Data	Definition
35h	07h	07h = 07h + 01h = 8 / number of sectors Lower Byte
36h	00h	number of sectors Upper Byte
37h	20h	20h = 32 * 256 bytes = 8KB / density Lower Byte
38h	00h	density Upper Byte

The unused erase block regions, address 39h through 3Ch, will be left empty at 00h.

3.4 Primary Vendor-Specific Extended Query

Address 40h to 42h defines the ASCII string “PRI”. The string “PRI” indicates the beginning of the “Primary Vendor-Specific Extended Query” table.

Table 3.20 Primary Vendor-Specific Extended Query

Address	Data	Definition
40h	50h	'P' in ASCII
41h	52h	'R' in ASCII
42h	49h	'I' in ASCII

Address 43h and 44h defines the Major and Minor version number of the Spansion CFI version implemented.

Table 3.21 Spansion CFI Version

Address	Data	Definition
43h	31h	Version 1.4 major version number '1' in ASCII
44h	34h	Version 1.4 minor version number '4' in ASCII

Address 45h defines if the Flash device has the “Address Sensitive Unlock” functionality and indicates the “Process Technology” of the Flash device.

The “Address Sensitive Unlock” functionality shows that the addresses during command cycles are “don't cares”. An example of a device implementing the “Address Sensitive Unlock” functionality is the

Am29LV065M Flash device. Take a look at the command definition table in the Am29LV065M and identify the differences versus other Flash devices.

The “Process Technology” defines the transistor size.

DQ7-DQ6 are reserved

DQ5-DQ2 defines the “Process Technology”

DQ1-DQ0 defines the “Address Sensitive Unlock” -> 0 = Supported, 1 = Not Supported

Table 3.22 Address Sensitive Lock

Address	Data	Definition
45h	08h	08h = 00001000b
		DQ1-DQ0 -> 00b -> Address Sensitive Unlock supported
		DQ5-DQ2 -> 0000b -> 230 nm Floating Gate technology 0001b -> 170 nm Floating Gate technology 0010b -> 230 nm MirrorBit® technology 0011b -> 130 nm Floating Gate technology 0100b -> 110 nm MirrorBit® technology 0101b -> 90 nm MirrorBit® technology 0110b -> 90 nm Floating Gate technology 1000b -> 65 nm MirrorBit® technology 1001b -> 45 nm MirrorBit® technology
		DQ7-DQ6 -> 00b -> Reserved

Address 46h defines “Erase Suspend” and indicates 00h if Erase Suspend is not supported, 01h if support for “Read Only” or 02h if support for both “Read and Write”.

Table 3.23 Erase Suspend

Address	Data	Definition
46h	02h	Erase Suspend supports both “Read and Write” operations

Address 47h defines the smallest “Sector Group” protected in the Flash device. For Flash devices with Boot Sectors, the smallest Sector Group consists of one sector. For Flash devices with Uniform Sectors, Sector Groups consist of four Uniform Sectors each.

Table 3.24 Sector Group

Address	Data	Definition
47h	04h	4 Sectors within a Sector Group in an Uniform Flash device

Address 48h defines the “Temporary Sector Unprotect” functionality. Temporary Sector Unprotect is a functionality that unlocks protected sectors by applying high voltage V_{ID} to the RESET# pin.

Table 3.25 Temporary Sector Unprotect

Address	Data	Definition
48h	01h	Temporary Sector Unprotect 00 = Not Supported 01 = Supported

Address 49h defines the “Sector Protection Scheme”.

Table 3.26 Sector Protection Scheme

Address	Data	Definition
49h	04h	AM29LV800 mode

Table 3.27 provides the different data code and definition mode options for Address 49h, shown in Table 3.26.

Table 3.27 Address 49h Data and Definition Table

Data Code	Definition Mode	Description
03h	AM29F400	(a) Temporary Sector Unprotect -> VID on RESET# (b) Programmer Protect -> VID on A9 and OE#
04h	AM29LV800	(a) AM29F400 (b) Sector Protect -> VID on RESET#, A6=L, A1=H, A0=L (c) Sector Unprotect -> VID on RESET#, A6=H, A1=H, A0=L
05h	AM29BDS640	(a) Sector Lock and Sector Unlock software commands Software Command Locking (SCL)
06h	AM29BDD160	(a) New Sector Protection Scheme
07h	AM29PDL128	(a) AM29LV800 (b) New Sector Protection Scheme
08h		Advanced Sector Protection

Address 4Ah defines the number of sectors in a simultaneous operation Flash device outside of Bank 1. For PDL128, there are four banks. The number of sectors outside of Bank 1, or the bank where the Flash device is to boot from during power up sequence, is 231, or E7h.

Table 3.28 Number of Sectors Outside Bank 1

Address	Data	Definition
4Ah	E7h	Simultaneous Operation 00 = Not Supported X = Number of Sectors outside Bank 1 which are Supported

Address 4Bh defines if the Flash device supports burst mode.

Table 3.29 Burst Mode

Address	Data	Definition
4Bh	00h	Burst Mode 00 = Not Supported 01 = Supported

Address 4Ch defines if the Flash device supports page mode. Page size of 4 Words or 8 Words is indicated by 46h being 01h or 02h respectively.

Table 3.30 Page Mode

Address	Data	Definition
4Ch	01h	4-Word Page Supported
	02h	8-Word Page Supported
	03h	16-Word Page Supported

Addresses 4Dh and 4Eh define the Acceleration Power Supply Voltage (A_{CC}) minimum and maximum limits. Bits 7-4 represent the volts in hex, while bits 3-0 represent the BCD equivalent value in 100 millivolt increments.

Table 3.31 Acceleration Power Supply Voltage

Address	Data	Definition
4Dh	B5h	11.5 volts (Bits 7-4: 1011 and Bits 3-0: 0101) A_{CC} lower limit
4Eh	C5h	12.5 volts (Bits 7-4: 1100 and Bits 3-0: 0101) A_{CC} higher limit

Address 4Fh defines if the Flash device consists of uniform sectors, uniform sectors mixed with boot sectors, and the write protect function from the WP# pin.

00 = Flash device without WP Protect

01 = Eight 8KB Sectors at TOP and Bottom with WP Protect

02 = Bottom Boot Device with WP Protect

03 = Top Boot Device with WP Protect

04 = Uniform, Bottom WP Protect

05 = Uniform, Top WP protect

06 = WP protect for all sectors

07 = Uniform, Top or Bottom WP protect (user selected)

Table 3.32 Sector and WP# Pin Protection Scheme

Address	Data	Definition
4Fh	02h	Bottom Boot with WP#

Address 50h defines “Program Suspend”.

Table 3.33 Program Suspend

Address	Data	Definition
50h	01h	Program Suspend 00 = Not Supported 01 = Supported

Address 57h defines “Bank Organization”. If data at Address 4Ah is 00h, indicating that Simultaneous Operation is not supported, Address 57h will also indicate 00h. For PDL128, there are four banks within the memory map.

Table 3.34 Bank Organization

Address	Data	Definition
57h	04h	04h = 04 = Number of Banks

Addresses 58h to 5Bh define the “Bank Region Information” for Banks A, B, C, and D.

For PDL128, there are four banks. The number of sectors inside Bank A, B, C, and D are 39, 96, 96, and 39 respectively

Table 3.35 Bank Region Information

Address	Data	Definition
58h	27h	Bank A Region Information: 27h = 39 = Number of sectors in Bank A
59h	60h	Bank B Region Information: 60h = 96 = Number of sectors in Bank B
5Ah	60h	Bank C Region Information: 60h = 96 = Number of sectors in Bank C
5Bh	27h	Bank D Region Information: 27h = 39 = Number of sectors in Bank D

4. Conclusion

This application note provides the user an understanding of how to derive the CFI table data, which are listed in Spansion NOR Flash data sheets.

Spansion supports the CFI tables in all parallel NOR Flash families.

Currently, the CFI standard does not support SPI Flash memories (such as the Spansion FL Family), or Spansion ORNAND™ Flash. Spansion does expect the CFI standard to support SPI Flash memory in the future.

5. Revision History

Section	Description
Revision 01 (March 28, 2008)	
	Initial Release
Revision 02 (June 5, 2008)	
	Minor update to Section 3.3; Changes to Table 3.22

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion. Spansion reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion assumes no liability for any damages of any kind arising out of the use of the information in this document.