Preliminary Information
This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

MINDSPEED™

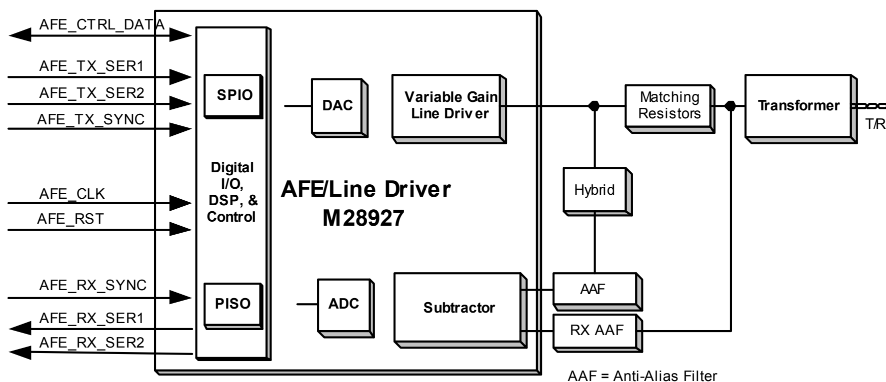
M28927

G.shdsl Multimode AFE/Line Driver

The M28927 is a companion device to Mindspeed's ZipWirePlus and ZipWireMulti family of G.shdsl DSP/Framers. Offered as single-port devices, the designer is granted maximum flexibility for PCB layout and routing. This typically results in superior performance, less heat concentration, and higher density than would be achievable with multi-port packages.

The M28927 AFE/Line Driver supports most modes of symmetrical DSL operation including G.shdsl, G.shdsl.bis, HDSL4, HDSL2, IDSL, HDSL, and SDSL/2B1Q. All of these modes are selectable via software with no changes to external components.

Functional Block Diagram



Distinguishing Features

- Operates with the entire family of ZipWirePlus™ and ZipWireMulti™ devices including:
  - M28945
  - M28946
  - M28947
  - M28950
  - M28985
- Supports multimode operation including:
  - ITU-T G.shdsl including EPAP modes (ITU-T G.991.2)
  - ITU-T G.handshake (ITU-T G.994.1)
  - HDSL2/4 (ANSI T1.418)
  - SDSL/2B1Q
  - IDSL (T1.601)
  - Proprietary/Extended Reach (ANSI spectrum management for loop transmission systems)
  - Proprietary/High-Speed (ANSI spectrum management for loop transmission systems)
- Low power consumption
- Packaging in 48-pin 6x6 mm ETQFP
- Support data rates from 192 kbps to 4.64 Mbps in 8 kbps increments
- Central office (COT) and remote (RT) operation
- +3.3 V and +12.0 V power supplies
- JTAG boundary scan
- Operation over full industrial temperature range (-40 to +85 °C)

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Ordering Information

Product Number	Description	Package	Ambient Temperature Range
M28927-29	AFE/Line Driver	6 x 6 mm 48-pin TQFP	-40 °C to 85 °C

Revision History

Document Number	Level	Date	Comments
28927-DSH-001-A	Preliminary	July 2003	Initial release.

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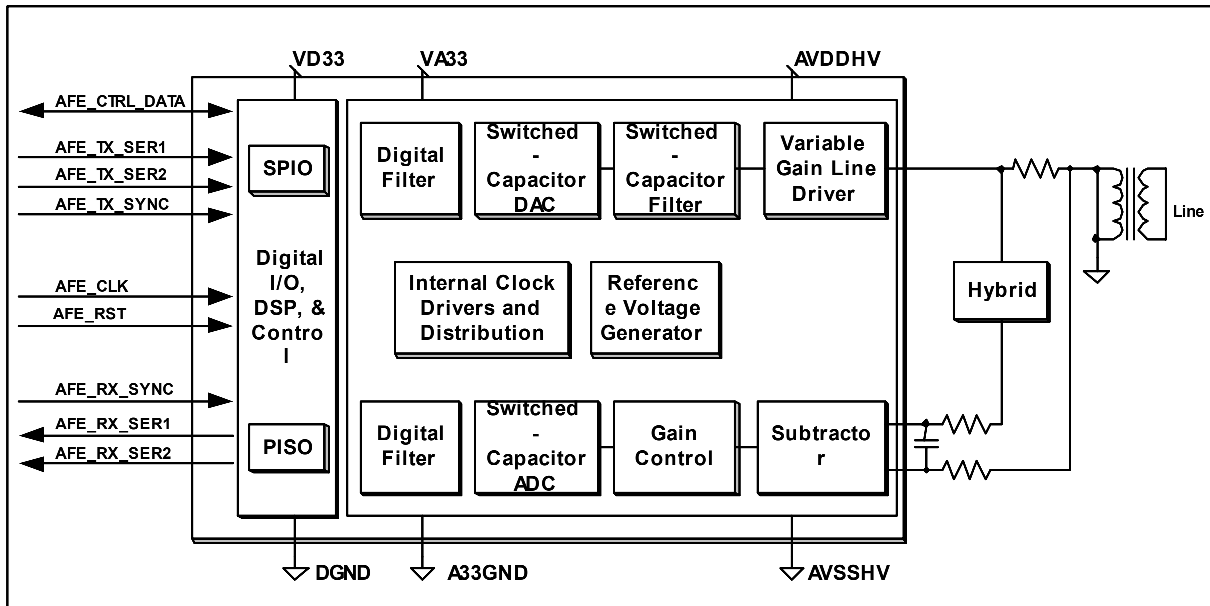
1.0 Hardware Interfaces

1.1 M28927 AFE/Line Driver Functional Summary

Figure 1-1 illustrates the M28927 AFE/Line Driver. The M28927 AFE/Line Driver performs the analog functions required for transmission and reception of G.shdsl, EPAP, OPTIS, or 2B1Q line-coded signals. The M28927 AFE/Line Driver includes the Digital-to-Analog (D/A) and Analog-to-Digital (A/D) data converters, anti-aliasing and post filtering circuitry, gain control blocks, and line drivers.

The M28927 AFE/Line Driver serial digital interface connects to the DSP/Framer transceiver. The serial interface protocol is proprietary. The DSP/Framer transceiver indirectly controls the AFE. The AFE interface consists of the line driver, impedance-matching resistors, external hybrid, and transformer.

Figure 1-1. M28927 AFE/Line Driver Block Diagram

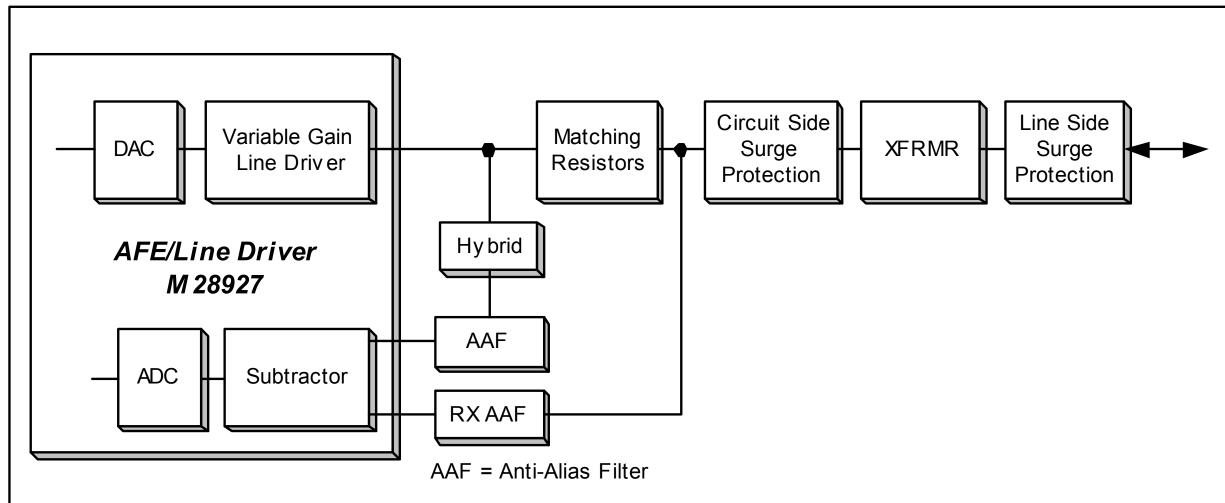


1.2 Transmission Line Interface

Figure 1-2 illustrates a block diagram of the DSL transmission line interface. The DSL interface consists of the continuous time filter, line drive feedback resistors, impedance matching resistors, compromise hybrid, transformer, and surge protection. All signals are differential pairs. Only NPO-type capacitors should be used in the DSL transmission line interface except for the surge protection blocks. The NPO capacitors

are selected because of their high degree of linearity characteristics. All capacitors should have a tolerance of 5% while the resistors should have a tolerance of 1%.

Figure 1-2. DSL Transmission Line Interface



1.2.1 Compromise Hybrid

The purpose of the compromise hybrid is to model the impedance of the transmission line. This model generates an approximation of the transmitted signal's echo. The echo replica is then subtracted from the signal on the line transformer to generate a first-order approximation of the received signal. Although the DSP/Framer device contains a digital echo canceller (EC), the hybrid is needed to reduce the signal-level input to the Analog-to-Digital Converter (ADC). This eliminates ADC overflow on short loops and increases the resolution of the digitized received signal for better digital signal processing performance.

1.2.2 Line Driver Compensation

The LD_PH/LD_PL and LD_MH/LD_ML signal pairs require that capacitors be placed between them. The LDOP/LDAOP and LDON/LDAON signal pairs require that inductors be placed between them. These components should be placed as close as possible to the device.

1.2.3 Impedance Matching Resistors

Impedance matching resistors are placed in the transmit path so the output impedance of the line interface more closely matches the impedance of the transmission line and load. This maximizes the power transferred to the receiver on the other end of the line. The load is assumed to be 135 W.

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1.2.4 Transformer

The line transformer provides DC isolation from the transmission line by creating a high-pass filter. The winding ratio of the transformer must be 2.0:1 (line side:circuit side) to generate the appropriate voltage level on the line. The primary inductance (L) of the line side transformer is a very critical parameter. If the inductance is too high, the cutoff frequency of the filter will be too low and the DSP+AFE echo canceller and equalizer will not be able to cancel out the low frequency components of the echo and inter-symbol interference (ISI). If L is too low, part of the information in the signal will be filtered out, thereby decreasing the Signal-to-Noise (SNR) ratio. In addition, the line transformer must meet certain return loss requirements to maximize system performance.

1.2.5 Anti-alias Filters

Anti-aliasing filters are needed to filter out high frequencies that would be aliased back into the passband as noise. These filters are made of all passive components. The cutoff frequency (fc) is designed to be as low as possible to achieve maximum attenuation of aliasing frequencies without filtering out the desired signal.

1.2.6 Surge Protection

Mindspeed uses the SIDACtor®, fuses, and diodes for surge protection on our EVM. Teccor Electronics (http://www.teccor.com) has an application note (Digital Line Card Circuit Protection) that is useful in designing surge protection.

1.2.7 Voltage Reference and Compensation Circuitry

Compensation capacitors must be connected between all M28927 voltage reference pins and analog ground.

In addition to compensation capacitors, external passive components are needed to set the bias current used in the M28927. Refer to the latest M28927 EVM schematics for these components.

1.2.8 Test and Diagnostic Interface (JTAG)

The Test and Diagnostic Interface comprises a test access port and two Serial Test Ports (STP). The test access port conforms to IEEE Std. 1149.1-1993 (IEEE Standard Test Access Port and Boundary Scan Architecture). Also referred to as the Joint Test Action Group (JTAG), this interface provides direct serial access to each of the transceiver's I/O pins. This capability can be used during an in-circuit board test to increase the testability and reduce the cost of the in-circuit test process.

The serial test ports function as a real-time virtual probe for looking at the transceiver's internal signals. A majority of the receiver's signal path is accessible through these outputs.

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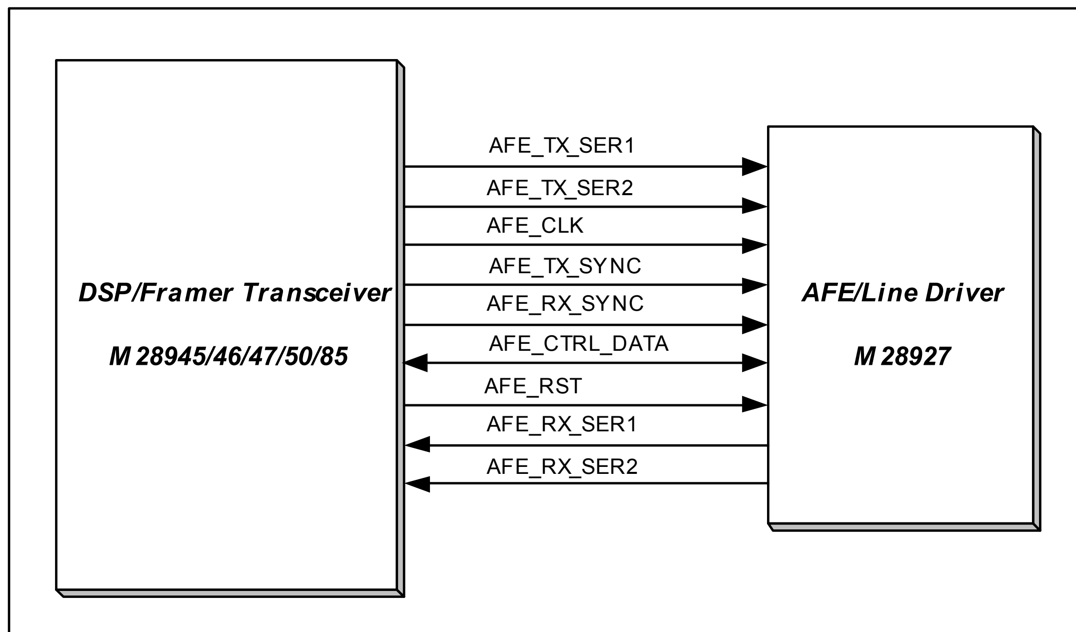
1.3 DSP/Framer Transceiver to M28927 AFE/Liner Driver Interface

Figure 1-3. DSP/Framer to AFE Interface



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2.0 Pin Descriptions

2.1 Pin Assignments

This section provides the pin assignments for the AFE device. The AFE/Line Driver is packaged as a 48-pin exposed thin Quad Flat Pack (ETFP). The pin list is shown in Table 2-1.

Table 2-1. Pin Assignments

ETQFP Pin Number	Signal Name
2	A12GND
43	A12GND
10	A33GND
12	A33GND
35	AFE_CLK
31	AFE_CTRL_DATA
36	AFE_RST
26	AFE_RX_SER1
25	AFE_RX_SER2
27	AFE_RX_SYNC
29	AFE_TX_SER1
30	AFE_TX_SER2
28	AFE_TX_SYNC
9	AVBIAS
32	DGND
40	LD_MH
39	LD_ML
46	LD_PH
47	LD_PL
42	LDAON
44	LDAOP
48	LDON
1	LDOP

Table 2-1. Pin Assignments

ETQFP Pin Number	Signal Name
24	No connect
37	No connect
8	RBIAS
4	RCDRVN
5	RCDRVP
34	SCAN_EN
3	VA12
41	VA12
45	VA12
11	VA33
13	VA33
38	VA33
16	VBGN
17	VBGP
14	VCMI
15	VCMO
23	VHN
22	VHP
33	VD33
18	VRNRX
6	VRNTX
19	VRPRX
7	VRPTX
21	VXN
20	VXP

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2.2 Signal Descriptions

Table 2-2 lists the AFE/Line Driver signal (pin) descriptions.

Table 2-2. M28927 AFE/Line Driver Signal Descriptions

Signal Name	I/O	Description
Power and Ground		
VA12	—	+12 V analog supply
A12GND	—	Analog ground for +12 V analog supply
VA33	—	+3.3 V analog supply
A33GND	—	Analog ground for +3.3 V analog supply
VD33	—	+3.3 V digital I/O supply
DGND	—	Digital I/O ground
Transmit Section		
LDOP	O	Transmit, positive (+) line driver output
LDON	O	Transmit, negative (–) line driver output
LDAOP	I	Transmit, auxiliary (+) line driver input
LDAON	I	Transmit, auxiliary (–) line driver input
RCDRVP	O	Transmit, positive (+) RC driver output
RCDRVN	O	Transmit, Negative (–) RC driver output
Transmit References		
VRPTX	REF	Transmit, positive (+) voltage reference
VRNTX	REF	Transmit, negative (–) voltage reference
Transmit Internal Signal		
LD_ML	—	Internal line driver signal
LD_MH	—	Internal line driver signal
LD_PH	—	Internal line driver signal
LD_PL	—	Internal line driver signal
Receive Section		
VXP	I	Receive, positive (+) transformer line input
VXN	I	Receive, negative (–) transformer line input
VHP	I	Receive, positive (+) hybrid analog input
VHN	I	Receive, negative (–) hybrid analog input
Receive References		
VRPRX	REF	Receive, Positive (+) Voltage Reference

Table 2-2. M28927 AFE/Line Driver Signal Descriptions

Signal Name	I/O	Description
VRNRX	REF	Receive, Negative (–) Voltage Reference
VBGP	REF	Reference, Positive (+) Band-gap Reference
VBGN	REF	Reference, Negative (–) Band-gap Reference
VCMO	REF	Reference, Output Common Mode Voltage
VCMI	REF	Reference, Input Common Mode Voltage
AVBIAS	REF	Reference, Compensation Capacitor
RBIAS	REF	Reference, Current Reference Resistor
DSP Interface		
AFE_CLK	I	19–27 MHz AFE clock (always running). Connects directly to DSP AFE_CLK.
AFE_RX_SYNC	I	Rxdata strobe. Connects directly to DSP AFE_RX_SYNC.
AFE_TX_SYNC	I	Txdata strobe. Connects directly to DSP AFE_TX_SYNC.
AFE_RST	I/O	Active-high input reset signal. Connects directly to DSP AFE_RST.
AFE_CTRL_DATA	I/O	Serial control data input/output. Connects directly to DSP AFE_CTRL_DATA.
AFE_RX_SER1	O	Serial RX data sample one (LSB). Connects directly to DSP AFE_RX_SER1.
AFE_RX_SER2	O	Serial RX data sample two (MSB). Connects directly to DSP AFE_RX_SER2.
AFE_TX_SER1	I	Serial TX data sample one (LSB). Connects directly to DSP AFE_TX_SER1.
AFE_TX_SER2	I	Serial TX data sample two (MSB). Connects directly to DSP AFE_TX_SER2.
Miscellaneous and Test		
SCAN_EN	I	ASIC scan enable input, connect to logic low (GND).

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3.0 Electrical and Mechanical Specifications

3.1 Recommended Operating Conditions

The recommended operating conditions are shown in Table 3-1 below.

Table 3-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
AFE 12.0 V Analog Supply	VA12	11.4	12.0	12.6	V
AFE 3.3 V Analog Supply	VA33	3.15	3.30	3.45	V
AFE 3.3 V Digital Supply	VD33	3.15	3.30	3.45	V
GENERAL NOTE: A12GND = A33GND = GND = DGND = 0 V; other voltages with respect to 0 V.					

3.2 Recommended Power Sequencing

Power up sequencing involves the order of powering up the IO and core supplies and the period of time between powering up these supplies.

The recommended sequence for the DSP/Framer and AFE is as follows:

5.0 V (VGNN)

3.3 V (VDDO, VD33 and VA33)

1.8 V (VDD)

There is no minimum or maximum time between supplies.

The sequencing of the 12.0 V (VA12) is not critical.

If the above power sequence is not followed, there will be potentially a large forward bias current drawn until the IO supply (3.3 V) is powered up. This can cause a reliability issue.

3.3 Absolute Maximum Ratings

The absolute maximum ratings are shown in Table 3-2 below.

Table 3-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VA12	VA12	—	12.0	—	V
VA33	VA33	–0.3	3.30	3.45	—

Table 3-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VD33	VD33	–0.3	3.30	3.45	—
Voltage on any Signal Pin	—	GND–0.3	—	VIO + 0.3	V
Input Current, any pin except supplies	IMAX	—	—	±10	mA
Analog Input Voltage	—	–0.3	—	VAA + 0.3	V
Digital Input Voltage for AFE	—	–0.3	—	3.45	V
Ambient Operating Temperature	T_A	–40	25	+85	°C
Junction Temperature	T_J	—	—	125	°C
Storage Temperature (ambient)	T_{SA}	–65	—	150	°C
Soldering Temperature	TSOL	–65	—	260	°C
Vapor Phase Soldering	TVSOL	–65	—	220	°C
Air Flow	0	—	0	—	L.F.P.M.
GENERAL NOTE: Operation beyond these limits may cause permanent damage to the device. Normal operation is not guaranteed at these extreme conditions.					

3.4 Thermal Characteristics

For the 48-pin ETQFP AFE Line Driver device with 0 m/s of airflow, qJA~ 27 °C/W.

3.5 Power Consumption

Table 3-3 below shows the breakdown for the M28927 AFE power consumption for 1,552 kbps G.shdsl Enhanced Performance Asymmetric PSD (EPAP) and 2,320 kbps G.shdsl Symmetric PSD mode.

These power values assume normal operating modes of random (scrambled) data with a 10 Kft. 26 AWG line

The maximum values are for worst case temperature, voltage, and silicon process.

The power consumption includes the power delivered to the DSL line. In EPAP mode, the power delivered to the load is ~100 mW. In symmetric PSD mode, the power delivered to the load is ~50 mW.

Table 3-3. AFE Power Dissipation

Parameter	Condition	Symbol	Min	Typ	Max	Units
AFE, +12.0 V	EPAP	$PD_{AFE\ 12.0}$	—	420	—	mW
	Sym PSD		—	350	—	mW
AFE, +3.3 V	—	$PD_{AFE\ 3.30}$	—	410	—	mW

The following tables detail the M28927 power consumption at different modes, distances, and rates.

Table 3-4. Power Consumption of the M28927 in Idle Mode/Reset Stage

MODE	Current (mA)		AFE
	3.3V AFE	12VAA AFE	Power/Port (W)
Idle	118.50	22.58	0.662
Hold Reset	87.30	0.17	0.290

Table 3-5. Power Consumption of the M28927 in HDSL2 Mode at 9 kft (26 AWG) Loop

DSL Line Rate (Kbps)	Current (mA)		AFE Power/Port (W)
	3.3V AFE	12VAA AFE	
1552	115.20	33.85	0.786

Table 3-6. Power Consumption of M28927 in G.hsdsl Mode at 9 kft (26 AWG) Loop in Annex A Symmetric Mode

DSL Line Rate (Kbps)	Current (mA)		AFE Power/Port (W)
	3.3V AFE	12VAA AFE	
200	113.00	30.01	0.733
208	113.10	29.85	0.731
272	113.20	29.01	0.722
392	113.20	28.44	0.715
400	113.10	28.40	0.714
528	113.30	28.17	0.712
776	113.40	28.16	0.712

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Table 3-6. Power Consumption of M28927 in G.hsdsl Mode at 9 kft (26 AWG) Loop in Annex A Symmetric Mode

784	113.70	28.21	0.714
1040	114.40	28.28	0.717
1168	114.10	28.32	0.716
1552	115.50	28.44	0.722
2056	115.30	28.62	0.724
2064	115.40	28.62	0.724
2312	118.50	28.62	0.734
2320	118.60	28.62	0.735

Table 3-7. CO, Annex A, Asymmetric, 9 Kft 26 AWG

DSL Line Rate (Kbps)	Current (mA)		AFE Power/Port (W)
	3.3V AFE	12VAA AFE	
1552	115.50	38.20	

Table 3-8. CO, Annex B, Asymmetric, 9 Kft 26 AWG

DSL Line Rate (Kbps)	Current (mA)		AFE Power/Port (W)
	3.3V AFE	12VAA AFE	
2056	116.50	35.26	0.808
2312	120.00	32.00	0.780

3.6 DC Characteristics

Table 3-9. AFE DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.50	-	3.45	V
Input Low Voltage	VIL	GND	-	0.4 V	V
Input Leakage Current	IIL/IIH	-10	-	10	mA
Input Capacitance	CIN	-	2.9	-	pF

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Table 3-9. AFE DC Characteristics

Digital Outputs					
Output High Voltage	VOH	0.9 VIO	-	VIO	V
Output Low Voltage	VOL	GND	-	0.1 VIO	V
Three-State Output Leakage	ILK	10	-	10	mA
Output Capacitance	CIN	-	3.1	-	pF
Digital Bidirectionals					
Three-State Output Leakage	ILK	-10	-	10	mA
Input/Output Capacitance	CINOUT	-	3.0	-	pF

3.7 Mechanical Specifications

Figure 3-1 illustrates the 48-pin ETQFP for the AFE/Line Driver.

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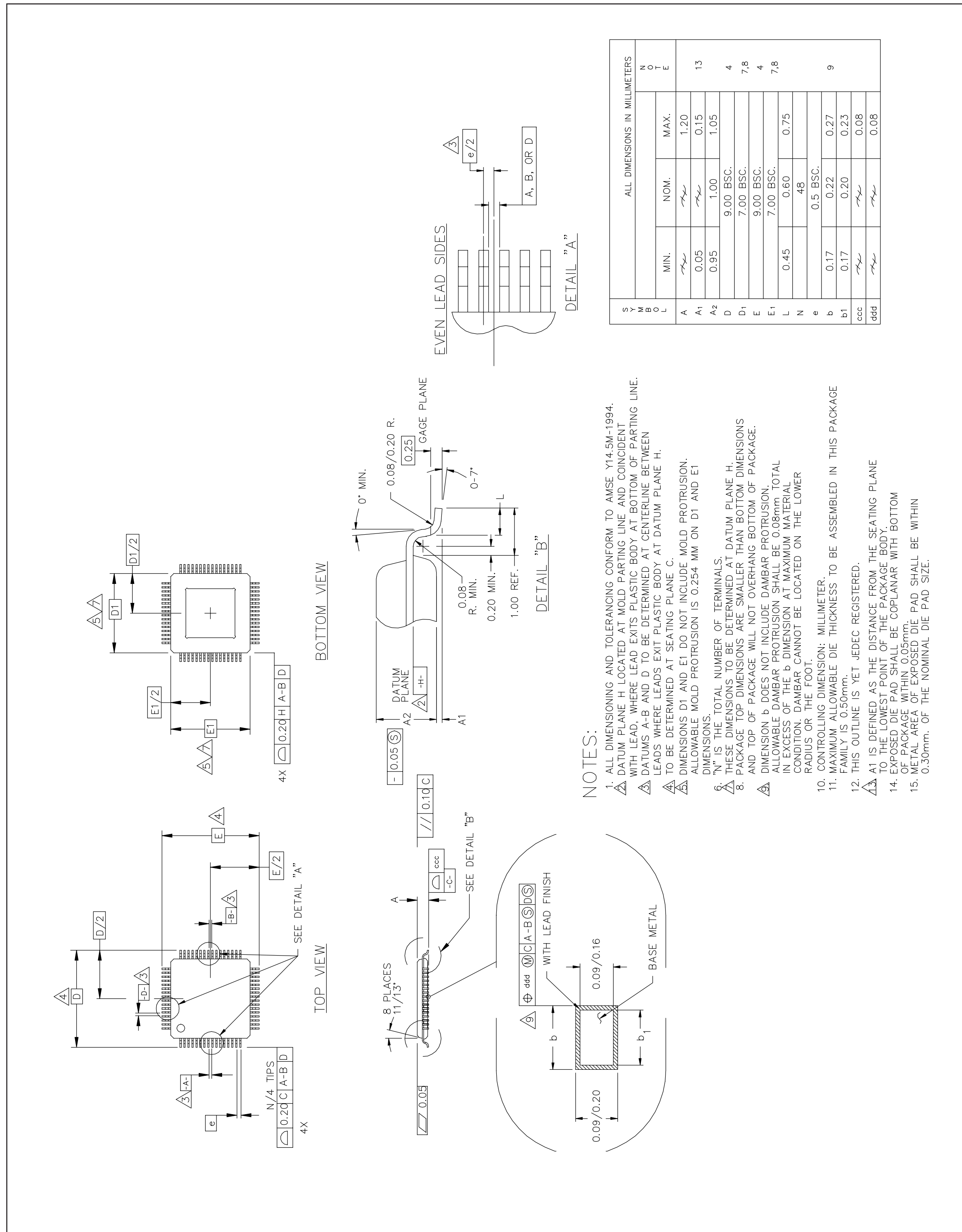
Figure 3-1. Top and Bottom View of a 6x6, 48-pin ETQFP



SYMBOL	ALL DIMENSIONS IN MILLIMETERS			
	MIN.	NOM.	MAX.	NOTE
A	~	~	1.20	
A_1	0.05	~	0.15	13
A_2	0.95	1.00	1.05	
D		9.00 BSC.		4
D_1		7.00 BSC.		7,8
E		9.00 BSC.		4
E_1		7.00 BSC.		7,8
L	0.45	0.60	0.75	
N		48		
e		0.5 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	~	~	0.08	
ddd	~	~	0.08	

4.0 Schematic, BOM, Layout Recommendations, and Diagnostic Test

4.1 Schematic and BOM

Figure 4-1 and Table 4-1 show the schematic and Bill of Material (BOM) respectively.

4.2 Layout Recommendations

4.2.1 AFE/Hybrid Placement

The AFE/hybrid should be placed in a quiet ara of the PCB away from all digitial and clock signals.

The botton of the M28927 (AFE) contains an exposed copper pad/heat sink and should be soldered to an exposed metal island on the top layer of the board. This island can be used as a quiet analog ground and all of the return pins from the AFE can be routed to it. See Appendix A, Exposed Pad Thin Quad Flat Pack (ETQFP), for the procedure for the proper layout and solder assembly of the ETQFP package. This procedure must be followed to ensure optimal performance of the AFE.

All of the decoupling capacitors for power and references should be placed as close to to the pins as possible.

4.2.2 Hybrid Layout and Routing

Lay out hybrid components symmetrically. The traces should be short, direct, equally wide and of the same length. They should flow symmetrically and be close together whenever possible. Mount the anti-alias filter components as close to the AFE as physically possible. The traces coming from pins 21 - 24 of the AFE should be kept very short. If this cannot be achieved, they must be routed as differential pairs and guarded on both sides with analog returns on an inside layer to increase noise immunity.

Figure 4-1. M28927 Hybrid Schematic

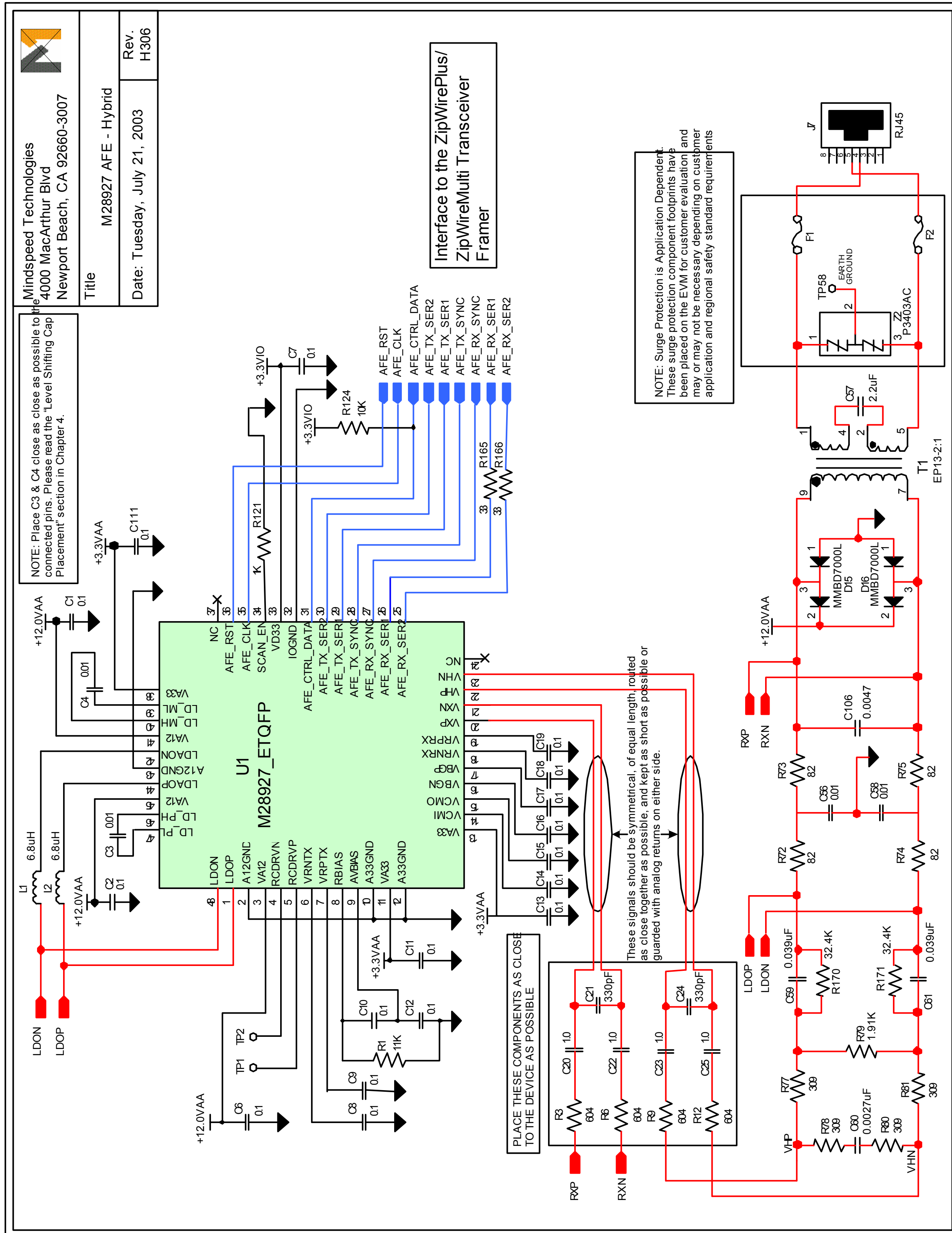


Table 4-1. M28927 Bill of Materials

M28927 HYBRID BILL OF MATERIALS REV. H306

Item	QTY	Reference	Manufacturer	Part Number	Description
1	17	C1,C2,C7,C6,C8,C9,C10,C11,C12	PANASONIC	ECJ-1VB1C104K	CAP, 0.1 UF, 16V, X7R, 0603, 20%
		C13,C14,C15,C16,C17,C18,C19,C111			
2	2	C3,C4	PANASONIC	ECJ-0EB1C103K	CAP, 0.01UF, 16V, X7R, 0402, 10%
3	4	C20,C22,C23,C25	TDK	C1608X5R1A105KT	CAP, 1.0 UF, 10V, X5R, 0603, 10%
4	2	C21,C24	PANASONIC	ECJ-1VC1H331J	CAP, 330 PF, 50V, NPO, 0603, 5%
5	1	C57	Taiyo Yuden	EMK316BJ225MC	CAP, 2.2 UF, 16V, X7R, 1206, 10%
6	2	C59,C61	TDK	C3225COG1H393J	CAP, 0.039 UF, 50V, COG, 0805, 5%
7	1	C60	TDK	C2012COG1H272J	CAP, 0.0027 UF, 50V, COG, 0805, 5%
8	2	C56,C58	TDK	C2012COG1E103J	Cap, 0.01UF, 50V, COG, 0805, 5%
9	1	C106	TDK	C2012COG2A472J	CAP, 0.0047UF, 25V, COG, 0805, 5%
10	2	D16,D15	MOTOROLA	MMBD70000LT1	Diode, Dual Switching, SOT 23
11	2	F1,F2	TECCOR	FUS60ASMD036	Fuse, TELELINK
12	1	J7	MOLEX	95040-2881	Conn, RJ45, Internal Shield, Right Angle
13	2	L1,L2	TOKO	FSLB2520-6RM8	Inductor, 6.8 uH, +/-20%, DCR 0.065, 0805
14	1	R1	KOA	RK73H1E1102F	Res, 11K OHM, 1%, 0402, 1/16 W
15	4	R3,R6,R9,R12	KOA	RK73H1E6040F	Res, 604 OHM, 0402, 1%
16	4	R72,R73,R74,R75	KOA	RK73H2A8R25F	Res, 8.25 OHM, 1%, 0805
17	1	R124	KOA	RJ73H1E1002F	Res, 10K, 5%, 0402, 1/16 W
18	4	R77,R78,R80,R81	KOA	RK73H1E3090F	Res, 309 OHM, 0402, 1%
19	1	R121	KOA	RK73H1E1001F	Res, 1K, 5%, 0402, 1/16 W
20	2	R165,R166	KOA	RK73H1E33R2F	Res, 33.2 OHM, 0402, 1%
21	1	R79	KOA	RK73H1E1911F	Res, 1.91K OHM, 0404, 1%
22	2	R170,R171	PHILIPS	2322-706-7-3243	Res, 32.4K OHM, 0402, 1%
23	1	U1	MINDSPEED	M28927-29	IC, AFE, 48 PIN ETQFP
24	1	Z2	TECCOR	P3403AC	Sidactor, TO-220, Balance Three Chip
25	1	T1	MIDCOM	50772	XFMR, 2:1, EP13, THROUGH HOLE

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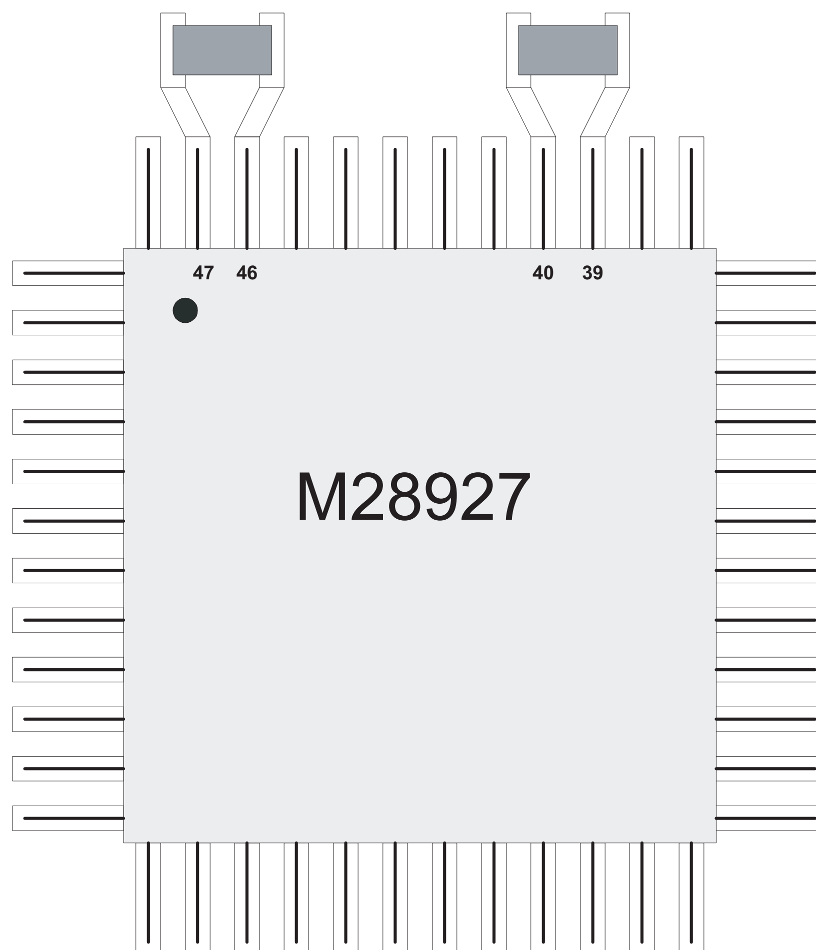
4.2.3 Level Shifting Capacitor Placement

The M28927-XX AFE/LD uses a push/pull class D amplifier to generate its line driver output. Level shifting capacitors are required to maintain the proper DC level at the inputs of the class D amplifier. Parasitic reactive elements at these inputs can shift the input signal, causing a signal overlap and excessive current draw from the Line Driver circuitry. This excessive current draw can lead to reduced life expectancy or, in extreme cases, eventual failure of the M28927-XX AFE/LD. To eliminate this effect, the Level Shifting capacitors must be mounted on the component side of the PCB as close to the M28927-XX AFE/LD level shifting pins (pins 39 and 40, and 46 and 47) as physically possible. The routed traces should be short (<2 mm, 0.08”) and as thick as the pin pads (~0.25 mm, 0.01”). Ideally, the capacitors should be mounted across the pin pair pads.

Level shiting caps must be mounted on the component side of the PCB as close to the M28927 as physically possible. Traces should be < 0.08 " long and ~0.010" thick.

Figure 4-2. Level Shifting Capacitors Example



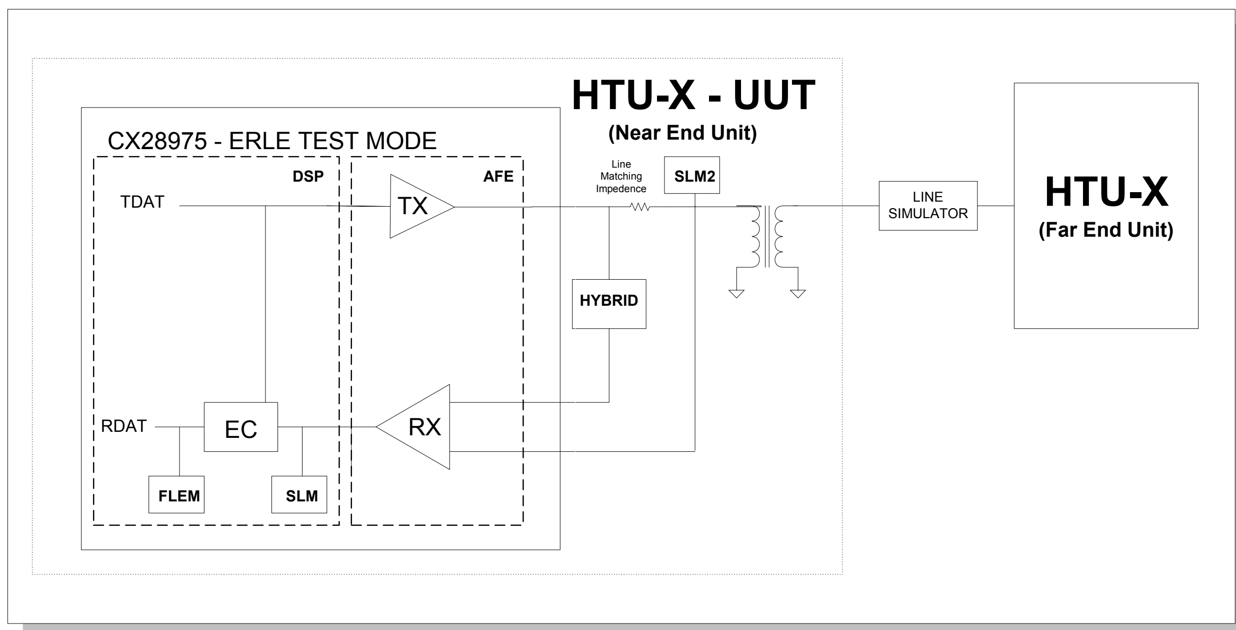
4.3 Diagnostic Test

Echo Return Loss Enhancement (ERLE) is a diagnostic tool to verify the integrity of the hardware's analog front end; transformer, surge protection, etc. The ERLE result determines the amount of echo canceled by the system. The echo is canceled initially by the external hybrid (Analog ERLE) and then by the linear digital echo canceler in the bitpump (Digital ERLE). This diagnostic tool can be used during development and manufacturing to identify problems with the AFE and Hybrid circuits.

4.3.1 Test Setup

Figure 4-3 shows the test setup needed for ERLE diagnostic mode. The Unit Under Test (UUT) is connected to a reference HTU-X (far end unit) via a line simulator. The line length is set to around 10K ft (24 or 26 AWG). The far end units transmitter may be disabled or powered down for ERLE testing. All configurtion for ERLE is done via Software API commands.

Figure 4-3. ERLE Test Setup



4.3.1.1 ERLE Test Modes

There are two major steps to the ERLE test modes:

- Background Noise Test—Transmitter OFF
- ERLE Test—Transmitter ON

Background Noise Test—Transmitter OFF

The background test measures the Signal Level Meter (SLM) while the transmitter is turned off. This effectively gives the amount of noise present at the input of the A/D. The noise result should be very small. A large noise result with the transmitter off usually indicates a DSL connection to a remote unit that is transmitting.

ERLE Test—Transmitter ON

The ERLE result determines the amount of echo canceled. The echo is canceled initially by the external hybrid and then by the Linear Echo Canceler (LEC) in the bit pump. The Analog ERLE (AERLE) determines how much echo is canceled by the external hybrid. The SLM, FELM, and SLM2 measurements are important. The SLM measures the input to the A/D converter. The FELM measures the output of the Digital Echo Canceler (DEC). The FELM value should be small because there is no far-end transmitter. The SLM/FELM ratio gives a quality measurement of the digital echo cancellation; the larger the ratio, the better the performance of the digital echo cancellation. A large SLM or FELM with the transmitter on could indicate that the DSL is not properly terminated. The SLM2 measures the TX signal power when bypassing the analog hybrid. The SLM2/SLM ratio gives a quality measurement of the analog echo cancellation. The following equations show how DERLE and AERLE is computed from SLM, SLM2 and FELM.

$$\mathbf{DERLE = 20 * \log (SLM / FELM)}$$

$$\mathbf{AERLE = 20 * \log (SLM2 / SLM)}$$

4.3.1.2 ERLE API Command Summary

Table 4-2 lists API commands that will be used for configuring the M28927 device for ERLE test modes.

Table 4-2. ERLE API Command Summary

Command	OPCode	Description
_BP_ERLE_TEST_MODE	0x18	Activates the ERLE test mode.
_BP_ERLE_RESULTS	0x93	Gets ERLE Test Mode Results.
_DSL_TEST_MODE	0x0D	Configures the device in special test modes. Use this command with the _EXIT_TEST_MODE option to abort a ERLE test before completion.

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4.3.2 ERLE Procedure

1. Connect your board under test via a line simulator of ~10k ft (24 or 26 gauge) and terminate the far-end with its transmitter turned off or the unit powered off.
2. Download and configure the modem as you would to run end-to-end except don't issue the _DSL_ACTIVATE (0x0B) command.
3. Issue the _BP_ERLE_TEST_MODE (0x18) with a parameter of 0x00
4. Wait for ERLE to complete by polling the _DSL_STATUS (Status 1 byte, upper 2 bits) until it reaches Normal Operation. ERLE takes ~1 seconds.
5. Get the ERLE results by issuing the _BP_ERLE_RESULTS (0x93) and apply the DERLE and AERLE formulas as specified in Section 4.3.1.1.
6. Compare the results with Table 4-3 below.

4.3.3 ERLE Results

Table 4-3 shows the minimum, typical and maximum values returned by _BP_ERLE_RESULTS API command for the NOISE, SLM, FLEM and SLM2 parameters. The ERLE and AERLE are calculated by the formulas described in Section 4.3.1.1. The ERLE results depend on the Hybrid, AFE, Transformer, Load, and software and may deviate from the below typical values.

Table 4-3. ERLE Results

ERLE RESULT	MINIMUM	TYPICAL	MAXIMUM
NOISE	5000	22000	30000
SLM	4,000,000	6,500,000	10,000,000
FLEM	100,000	150,000	200,000
SLM2	600,000,00	898,000,00	120,000,000
ERLE	28.0	32.0	38.0
AERLE	19.0	22.0	25.0

(1) ERLE RESULTS in Table 4-3 were measured on AFE labeled CX28927-11P.

Appendix A: Exposed Pad Thin Quad Flat Pack (ETQFP)

Abstract

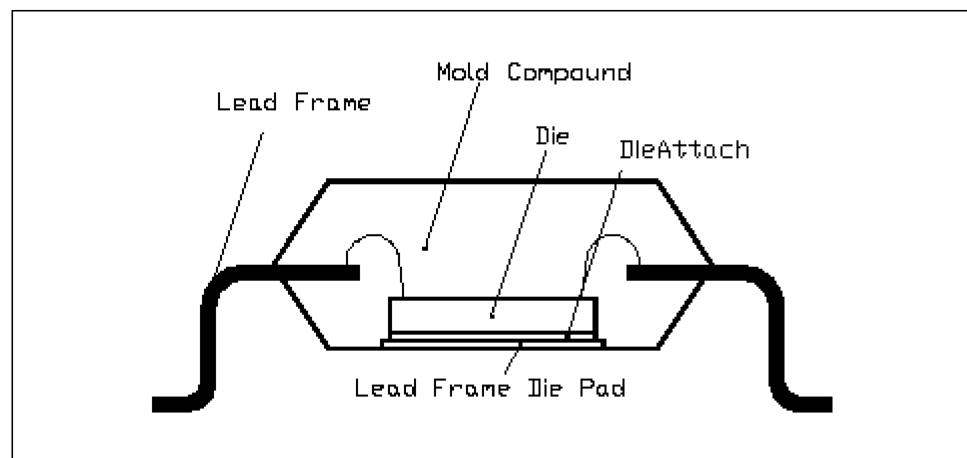
The Exposed Thin Quad Flat Pack (ETQFP) package provides greater design flexibility and increased thermal efficiency, while using a standard size IC Package. Exposed pad improved performance permits higher clock speeds, more compact systems, and more aggressive design criteria. ETQFP thermal performance is better than standard packages, however, to make optimum use of the thermal efficiencies designed into the ETQFP, the PCB must be designed with this package in mind. The following sections of this document provide more information regarding the thermal performance and PWB design for Mindspeed ETQFP's.

A.1 Introduction

The ETQFP is implemented using a standard epoxy-resin package mold compound. The integrated circuit die is attached to the lead-frame die pad using a thermally conductive epoxy. The leadframe is designed with a deep downset of the die attach pad so that it will be exposed on the bottom surface of the package after mold. This provides an extremely low thermal resistance between the IC junction and the exterior of the surface.

The external surface of the die pad can be attached to the PCB using standard solder re-flow techniques. This allows efficient attachment to the board, and permits the board structure to be used as a heat sink for the IC. Using thermal vias, the lead frame die pad can be attached to a ground plane or special heat sink structure designed into the PCB. Figure A-1 shows the schematic of the package components.

Figure A-1. Schematic Representation of the Package Components



A.2 Package Thermal Characterization

A.2.1 Heat Removal Path

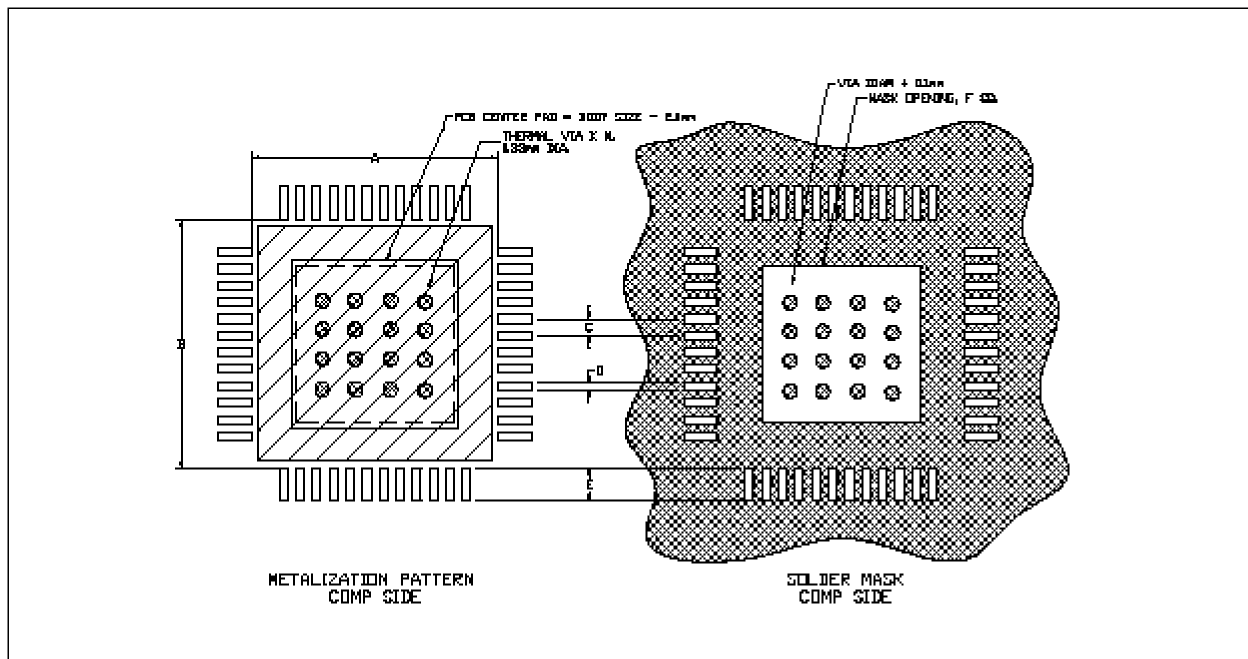
The internal heat removal path is designed to transfer heat from top surface of the die to the die pad and then directly to the Printed Circuit Board (PCB) through a center solder pad. The PCB must have features designed to remove heat from the package efficiently. At a minimum, there must be an area of solder-tinned-copper underneath the ETQFP, called a thermal land. Heat is transferred from the thermal land to the environment through thermal vias designed within the PCB structure.

A.2.2 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the exposed package. During normal surface mount re-fow the exposed pad on the underside of the package will be soldered to this thermal land creating an efficient thermal path. The size of thermal path is as large as needed to dissipate the required heat.

For simple double-sided PCBs, having no internal layers, the surface layers must be used to remove heat. Figure A-2 shows a sample package detail, including required solder mask and thermal land pattern for an EQTFP. The designer may consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member of other hardware convection.

Figure A-2. Package and PCB Land Configuration



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An array of 0.33 mm diameter thermal vias plated with 1 oz. copper must be placed on the pad and shorted to the ground plane of the PCB. If the plating thickness in the exposed region of the center pad is not sufficient to effectively plug the barrel of the via when plated, then solder mask should be used to cap the vias; the mask diameter should have a dimension equal to the via diameter + 0.1 mm minimum. This will prevent the solder from wicking through the thermal via, potentially creating a solder void in the region between the package bottom and the center pad on the surface of the PCB. Table A-1 shows the dimensions for the entire ETQFP package family.

Table A-1. Dimensional Parameters (mm)

Package Type	A	B	C	D	E	F	Recommended Array of Thermal Vias
48 pin ETQFP	7.40	7.40	0.50	0.25	1.00	25 sq.	5 x 5

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A.3 PCB Design

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sinks. The number of vias, the size of the vias used, and the construction of the vias is important in obtaining the best package thermal performance and the package/PCB assembly. Thermal performance analysis shows that there is a point of diminishing returns where additional vias will not improve heat transfer through the board, which is a function of die size and the number of thermal through the use of analysis tools. The PCB internal structure plays a very important role in package thermal performance. Figures A-3 and A-4 show the PCB structure for a 2 and a 6-layer design, respectively. PCB designs with more than 2 layers, should have all thermal vias connected to the ground plane.

Figure A-3. Internal Structure for a Two Layer PCB.

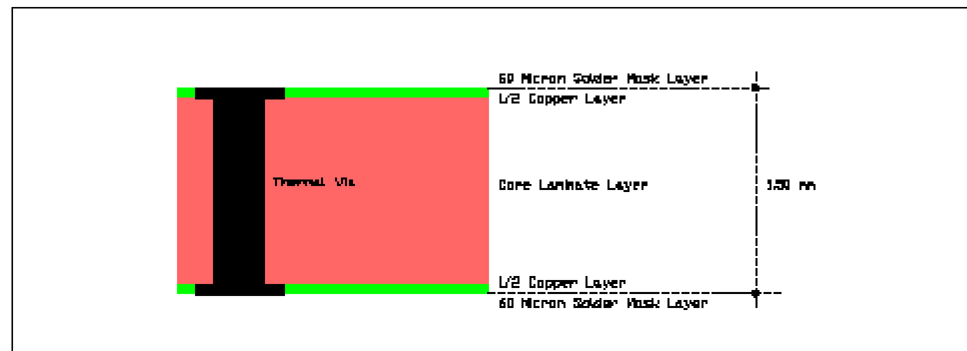
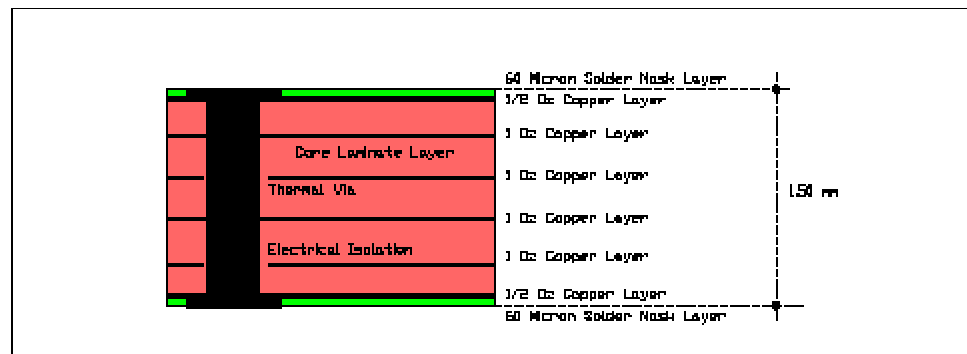


Figure A-4. Internal Structure for a Six Layer PCB

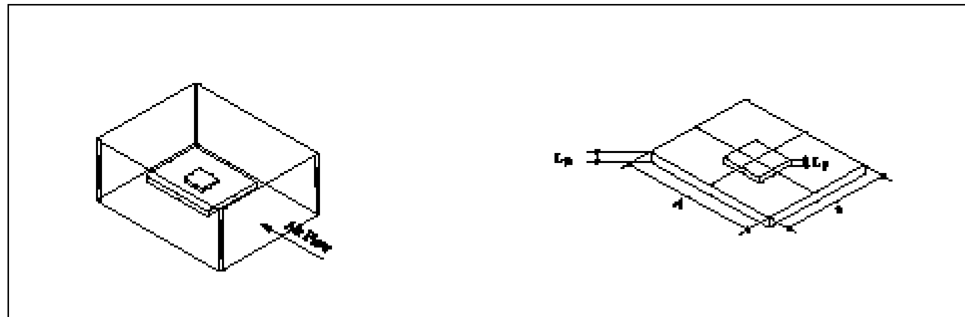


A.4 Thermal Test Structure

A.4.1 Test Environment

Package thermal performance has been tested following JEDEC standards. The ETQFP package is mounted at the center of a 100 mm – 100 mm six layer test- board and is tested under different air flow velocities. Figure A-5 shows the system configuration.

Figure A-5. Test Performance Structure (A = 100 mm, B = 100 mm, LP = 1.40 mm, LB = 1.60 mm)



A.4.2 Thermal Test Boards

Two different test boards have been used to evaluate package thermal performance for both worst and best conditions. Table A-1 shows specifications of these test boards.

Table A-1. Specification for a Two-layer Test Board

Drawing Number	TR03-T1
Substrate Material	FR-4
Thickness	1.6 mm
Stackup (# signal layers, # Cu planes)	1S0P
Cu Coverage (signal layer - top/bottom)	10%
Cu Coverage (power/gnd layer)	100%
Inner Cu Thickness (spec)	35 3.5

Table A-2. Specification for a Four-layer Test Board (1 of 2)

Drawing Number	TR03-T2
Substrate Material	FR-4
Thickness	1.6 mm
Stackup (# signal layers, # Cu planes)	1S2P
Cu Coverage (signal layer - top/bottom)	10%
Cu Coverage (power/gnd layer)	100%

Table A-2. Specification for a Four-layer Test Board (2 of 2)

Drawing Number	TR03-T2
Inner Cu Thickness (spec)	35 3.5

A.5 Package Thermal Performance

A.5.1 Calculation Guidelines

Maximum junction temperature can be calculated as:

$T_j = P \times \theta_{ja} + T_a$ (1)

Where:

θ_{ja} = Equivalent Package Thermal Resistance (C/W)

T_j = Maximum Junction Temperature (C)

T_a = Ambient Temperature (C)

P = Package Total Power Dissipation Value (W)

A.5.2 Package Thermal Resistance

Delco thermal test chips are used to estimate package thermal performance. Table A-3 shows thermal die specifications

Table A-3. Specification for Delco thermal test chips

Manufacturer	Delco	Delco	Delco
Dimensions	3.81 mm x 3.81 mm	6.35 mm x 6.35 mm	7.8 mm x 7.8 mm
Thickness	0.33 mm	0.45 mm	0.5 mm

Figure A-6 shows package thermal resistance as a function of airflow velocity for a 48 ETQFP package using two different test boards, specified in Tables A-2 and A-3, and a prediction for a 6 layer PCB design. Figures A-7 and A-8 show the similar information for a 64 and 80 ETQFP package. Table A-4 shows the test condition for each package type.

Table A-4. Test Conditions

Package Type	48 EQTFP	64 ETQFP	80 ETQFP
Body Size	7 mm x 7 mm	10 mm x 10 mm	14 mm x 14 mm
Die Size	3.81 mm x 3.81 mm	6.35 mm x 6.35 mm	7.8 mm x 7.8 mm
Die Pad Size	5 mm x 5 mm	7.50 mm x 7.50 mm	9.50 mm x 9.50 mm

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Figure A-6. Package Thermal Resistance as a Function of Airflow Velocity for a 48 ETQFP

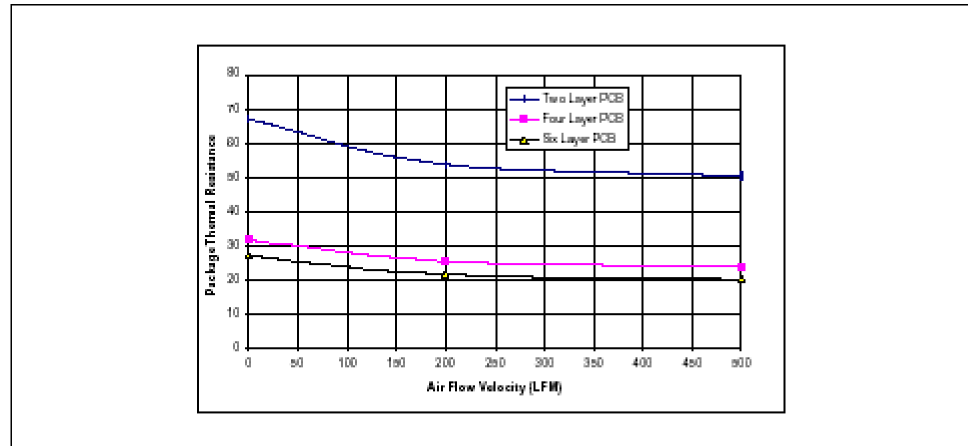


Figure A-7. Package Thermal Resistance as a Function of Airflow Velocity for a 64 ETQFP

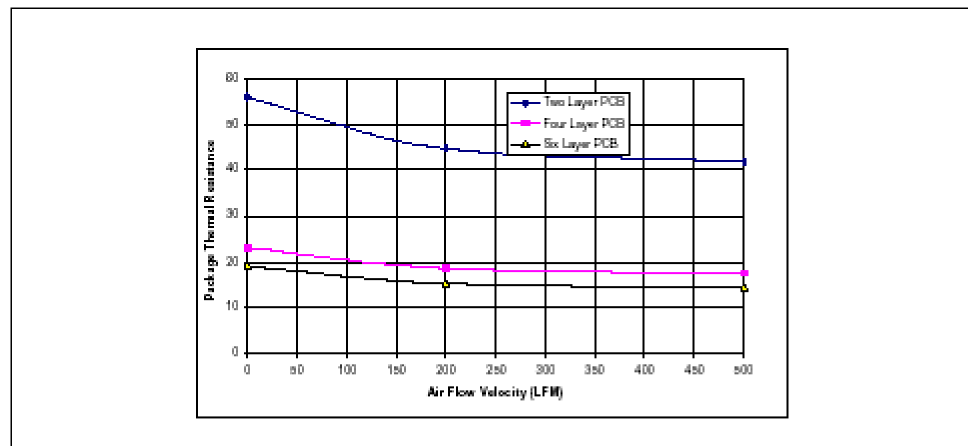
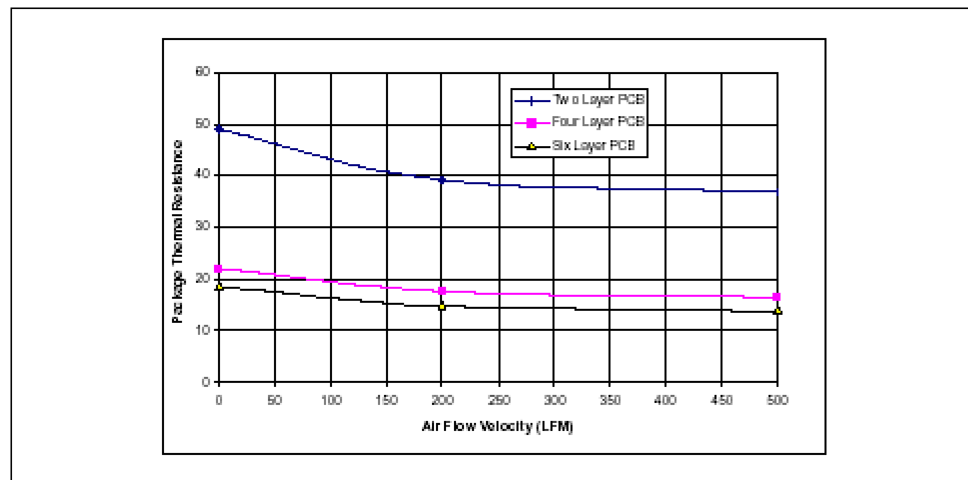


Figure A-8 illustrates the package thermal resistance as a function of airflow velocity for a 80 ETQFP. Package. Table A-4 5 shows the test conditions.

Figure A-8. Package Thermal Resistance as a Function of Airflow Velocity for a 80 ETQFP



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A.6 Solder Stencil Determination

The thickest possible solder mask, consistent with the components being assembled to the PWB and the with the PWB surface mount process, should be used. A standoff height of 2.0 to 4.2 mils provides good solder joints for both the leads and the center pad. This is achieved using a stencil thickness of 5, 6, or 7 mils.

A.7 Solder Re-flow Profile

The ETQFP uses the standard TQFP re-flow profile because the ETQFP package construction does not add thermal mass. There is minimal additional thermal load due to the increased solder area between the exposed die pad on the package and the center pad on the PCB. Figure A-9 and A-10 show typical IR re-flow profiles for Sn63:Pb37 solder in the cases of natural convection and forced convection ovens.

Figure A-9 illustrates the typical IR Reflow Profile for Eutectic Sn63:Pb37. Peak temperature should be approximately 220oC, and the exposure time should normally be less than 1.0 minutes at temperature above 183 ⁰C.

Figure A-9. IR Reflow Profile

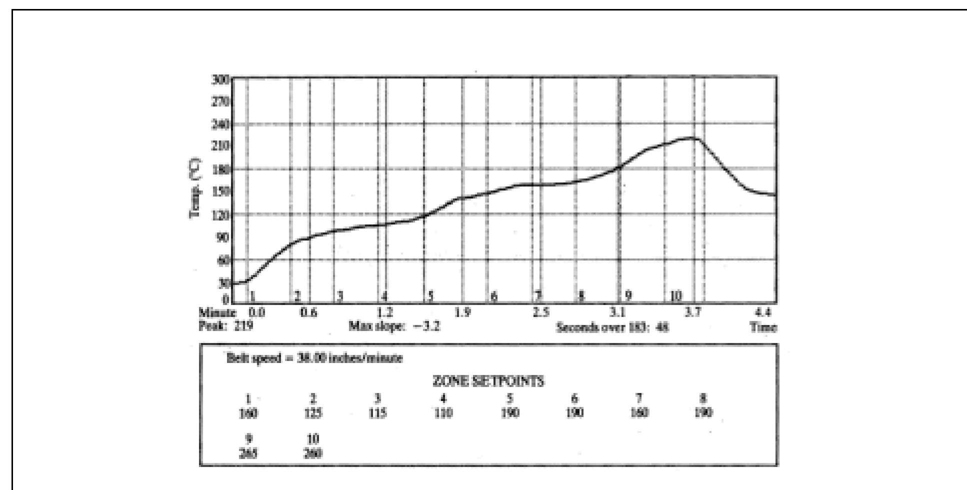
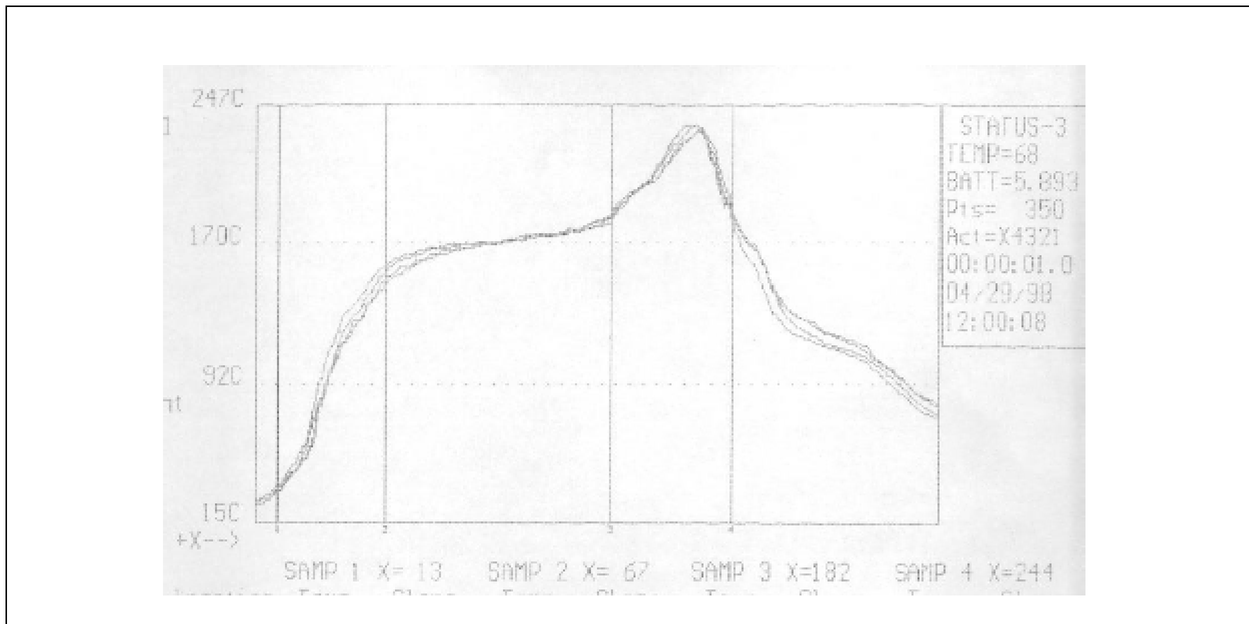


Figure A-10 illustrates the typical Forced Convection Reflow Profile for Eutectic Sn63:Pb37. Peak temperature should be approximately 235oC, and the exposure time should normally be less than 1.2 minutes at temperature above 183oC. Belt Speed = 30 Inches/minute (top and bottom setting), FANSPEED = 2500 RPM, NITROGEN LEVEL = 1200 SCFH

Figure A-10. Forced Convection Reflow Profile



NOTE:

ZONE 1 = 185°C ZONE 2 = 185°C ZONE 3 = 175°C ZONE 4 = 175°C
ZONE 5 = 180°C ZONE 6 = 190°C ZONE 7 = 230°C ZONE 8 = 270°C

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MINDSPEED™

www.mindspeed.com

(949) 579-3000 Headquarters
Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA. 92660