Enhanced EVM
ZipWirePlus™ G.shdsl/HDSL1/HDSL2/IDSL/SDSL Transceiver and Framer

User Guide

28945-EVMD-001-B
December 2004

MINDSPEED™

Revision History

Revision	Level	Date	Description
A	Advanced	December 2003	Initial release.
B	Advanced	December 2004	Added Unframed PCM 4-wire mode

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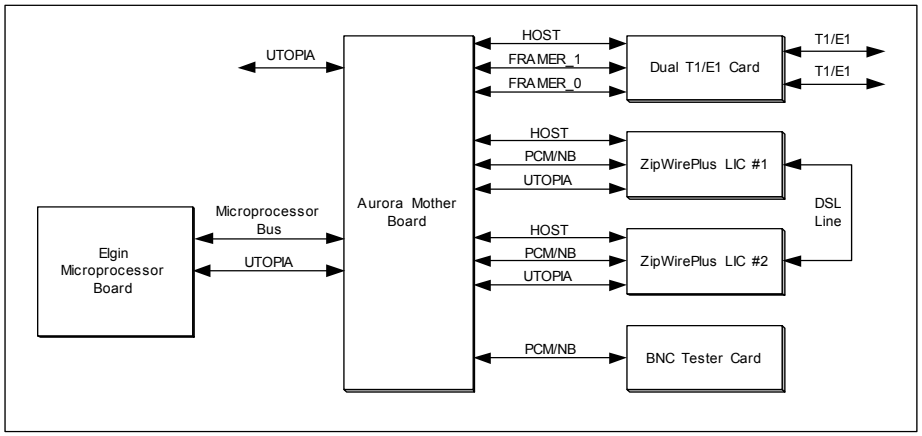
1.0 Introduction

Congratulations on your purchase of the Mindspeed ZipWirePlus™ High Bit-Rate Digital Subscriber Line (G.shdsl/HDSL1/HDSL2/IDSL/SDSL) evaluation system. You will find that it serves as an invaluable development platform to help get your product to market in the shortest possible time. The ZipWirePlus Enhanced Evaluation Module (EVM) facilitates the following:

- Demonstration/Evaluation—The ZipWirePlus Enhanced EVM allows you to demonstrate and evaluate the ZipWirePlus performance and features for standard G.shdsl, HDSL1, IDSL and HDSL2 configurations. In addition, the User Interface Program (UIP) enables you to exercise various configurations supported by the device.
- Customer System Debug and Trouble Shooting—The ZipWirePlus Enhanced EVM helps you to debug and troubleshoot your system. By using the ZipWirePlus Enhanced EVM as the far-end unit, you can debug your system against the known working ZipWirePlus Enhanced EVM system.
- Customer Host Processor Software Development—The Line Interface Card (LIC) allows you to connect the ZipWirePlus device's host bus or UIP interface to an external host processor to develop, test, and debug the software features (API commands) running on the external host processor.
- ZipWirePlus LIC—The ZipWirePlus LIC can be used in customer prototype development.

Figure 1-1 illustrates the architecture of the Enhanced EVM.

Figure 1-1. ZipWirePlus Enhanced EVM Architecture



1.1 Product Features

One complete Enhanced EVM kit and one ZipWirePlus kit allows you to evaluate the following applications:

- Single Pair application—G.shdsl, OPTIS 1T1, 2B1Q (Bt8973 mode), IDSL and HDSL1

Two complete Enhanced EVM kits and two ZipWirePlus kits allow you to evaluate the following applications:

- Multipair Applications—G.shdsl, PCM and Narrowband
- Single span Repeater Application—G.shdsl
- ATM Applications

The Enhanced EVM supports the following data rates for the different modes:

- G.shdsl frame structure: data rates from 192–4,640 kbps in 8 kbps steps
- RS8973 (2B1Q) Interoperability: data rates from 144–2,320 kbps in 8 kbps steps
- OPTIS 1T1 frame structure—1,552 kbps
- HDSL1 frame structure: standard and non-standard variable data rates over 1 loop

1.2 Ordering Information

The ZipWirePlus Enhanced EVM kit includes one Aurora motherboard, one Elgin Microprocessor board, one Dual T1/E1 card, one BNC Tester card and cables.

The individual ZipWirePlus line card (LIC) kits can be ordered separately. Each individual line card kit contains two line cards. The Table 1-1 shows the Mindspeed ordering part numbers for the Enhanced EVM and individual line card kits.

Table 1-1. Enhanced EVM System Contents

Description	Ordering Part Number
Enhanced EVM Kit	MH08-D260-001
M28945 Line Card Kit	BT02-D130-081 rev. N
M28946 Line Card Kit	BT02-D130-091 rev. A
M28947 Line Card Kit	BT02-D130-101 rev. A
M28950 Line Card Kit	BT02-D130-111 rev. A

Individual line cards can be used to:

- Evaluate the supported features
- Upgrade an existing evaluation board
- Replace a damage evaluation board
- Provide a spare evaluation board for performing hardware experiments
- Perform prototyping

2.0 Preparation and Setup

2.1 Enhanced EVM Contents

Please check the contents of the Enhanced EVM shipping carton to make sure you have received all of the items in Table 2-1. The system is already configured for optimal setup except for connections to the power supply, line simulator, BER tester, and host computer.

Table 2-1. Enhanced EVM System Contents

Qty	Description
Hardware	
1 each	Elgin Microprocessor Board
1 each	Aurora Mother board
1 each	Dual T1/E1 transceiver card
1 each	15V & 5V Dual Power Supply Brick
1 each	AC Power Cord
2 each	7-foot RJ-45 Twisted Pair Data Cables
1 each	6-foot RJ-11 to RJ-11 cable
1 each	DB9-F to RJ-11 Adapter (to configure IP address)
1 each	T1/E1 Cable Adapter (for Fireberd)
1 each	BNC Tester Card
Documentation	
1 each	Enhanced EVM Installation guide
CD-ROM Contents	
The Preliminary Enhanced EVM CD-ROM contains all the necessary documentation and software to operate the Enhanced EVM board.	

2.1.1 Enhanced EVM Software Contents

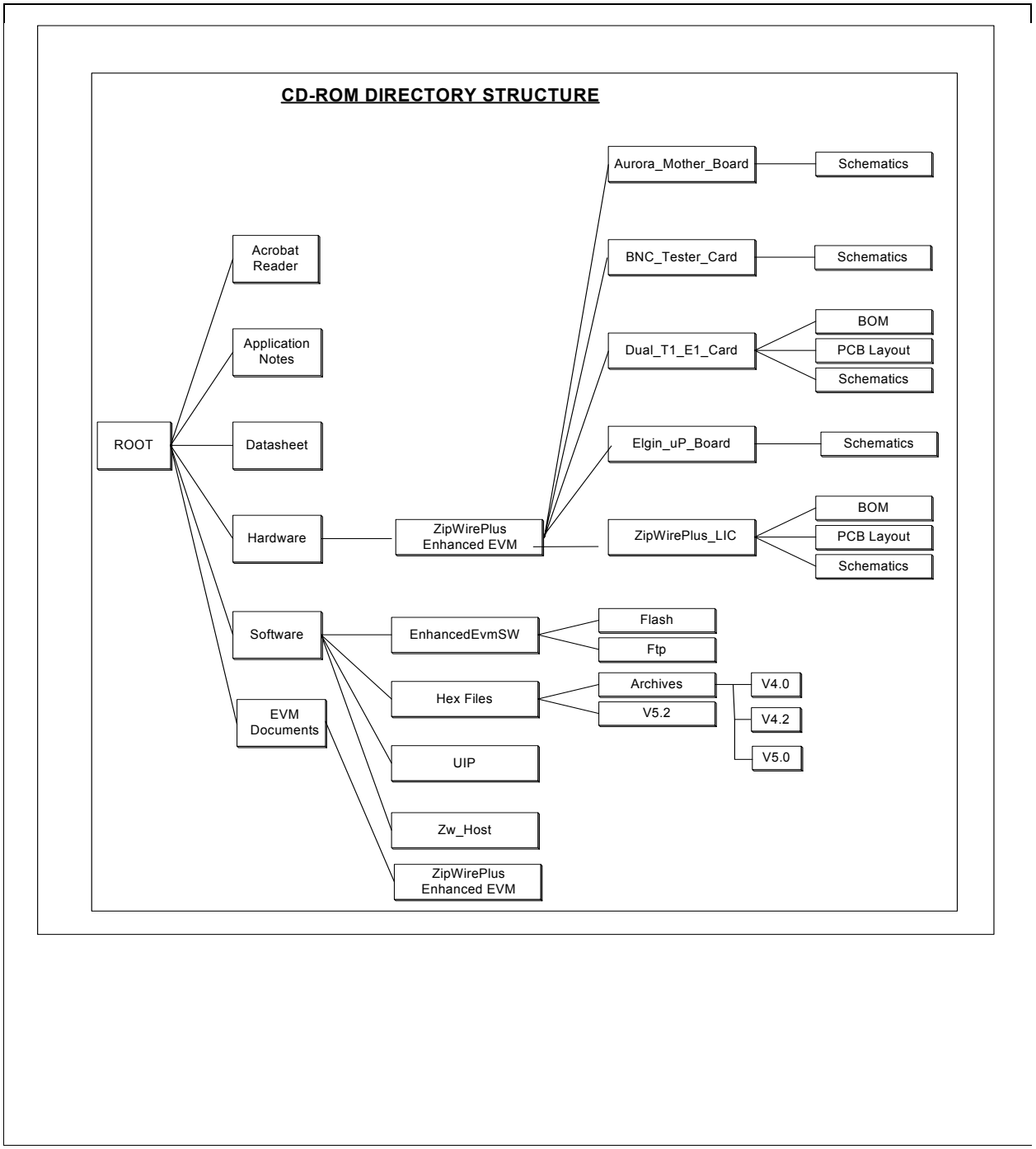
The Enhanced EVM Software is located at C:\Program Files\Mindspeed\ZipWirePlus Enhanced EVM\Software. It includes the following

- *Hex Files* - This software is executed inside the ZipWirePlus device. It is downloaded to the ZipWirePlus device.
- *UIP*- contains the TestExec Software. The TestExec(UIP) is a GUI based software which is used to control and monitor the Enhanced EVM platform.

- *EnhancedEvmSW* - contains the software which will be executed on the Host Microprocessor. This directory further consists of the subdirectory:
  - *ftp* - contains the FTP images for Host Microprocessor Software.
  - *flash* - contains the flash images for mcst microprocessor software. This option is currently not used.
- *FTPServer* - A sample FTP server has been included. The user can use any FTP server he wants to. Please consult the readme.txt file to use the sample ftp server.

Figure 2-1 shows the CD directory structure.

Figure 2-1. CD Directory Structure



2.2 Recommended Test and Measurement Setup

2.2.1 Line Simulators

Table 2-2 lists contact information for companies which support line simulators.

Table 2-2. Line Simulators

Manufacturer	Model	Emulation	Contact Information
Consultronics Spirent Communications	DLS–200H DLS–400H DLS–200HE DLS–400HE DLS–50 XPS–50	ANSI HDSL/ISDN ANSI HDSL/ISDN (partial) ETSI 1, 2 and 3 Pair, ISDN ETSI 1, 2 and 3 Pair, ISDN (partial) Straight Wire—no noise Straight Wire—no noise	1-800-227-3345 (US) 1-800-267-7235 (Canada) +44-2380-246-800 (UK) www.consultronics.com www.dlstestworks.com
Spirent Communications, formerly Telecom Analysis Systems (TAS)	TAS2270	Telcordia (formerly Bellcore)	1-732-544-8700 (voice) 1-732-544-8347 (fax) www.taskit.com
Acterna, formerly Wavetek, Wandel, and Goltermann	ILS–2	ETSI	1-800-729-9441 (US) http://www.acterna.com

2.2.2 Bit Error Rate (BER) Testers

Table 2-3 lists contact information for BER Testers.

Table 2-3. Bit Error Rate Testers

Manufacturer	Model	Contact Information
Acterna, formerly Telecommunications Technique Corp–(TTC) (see Table 2-4 for 6000A interface adapter modules)	Fireberd 6000A T-Berd 2209A	1-800-638-2049 (voice) 1-301-353-0234 (fax) http://www.acterna.com
International Data Services (IDS)	Model 77 Model 76B	1-800-IDS-DATA (voice) 1-401-737-9911 (fax) www.idsdata.com

Table 2-4 lists available models of Fireberd 6000A Interface Adapters.

Table 2-4. Fireberd 6000A Interface Adapters

Fireberd Adapter	Model	Used With
T1/FT1	41440	N/A
2MG704	30609	N/A
2M/Nx64 Kbps	41800	N/A
Lab (TTL) Data Interface	40204	Framer Bypass

.

NOTE: The T-Berd 2209A and IDS BER testers have not been verified with the Enhanced EVMs.

2.2.3 ATM Testers

lists the contact information for Cobalt ATM Testers.

Table 2-5. ATM Testers

Manufacturer	Model	Contact Information
Acterna	ATM UTIPIA Level 1+2 Emulator	1-800-638-2049 (voice) 1-301-353-0234 (fax) http://www.acterna.com

2.2.4 PC Controller

To use the ZipWirePlus UIP, a PC with the following configuration is required:

- Windows® 98, Windows NT® 5.0+, Windows 2000 or Windows XP
- One serial port (to configure boot parameters for the Enhanced EVM).

Two 9F–9F null-modem cables are required for most computers and are included.

NOTE: Mindspeed does not guarantee compatibility with Windows 95 and Windows Me.

2.2.5 User Interface Program (UIP)

A UIP is provided to perform more advanced ZipWirePlus Enhanced EVM monitoring and testing. This program runs on a standard IBM-compatible PC and interfaces from the PC to the ZipWirePlus Enhanced EVM through the 10/100 Base T Ethernet port. Please see the *UIP User Guide* for additional information.

3.0 Getting Started

This section describes the procedures for setting up and configuring the Mindspeed Enhanced EVM for various applications.

3.1 Enhanced EVM Overview

The Enhanced EVM comprises a Elgin Microprocessor board, 4 slots (on which LICs can be inserted). The LICs that can be inserted on to the slots are Dual T1/E1 Card, BNC Tester Card and ZipWirePlus device LICs. The following subsections will walk the user through the major blocks of the EVM.

3.1.1 Elgin Microprocessor Board

The Elgin Host Microprocessor Board comprises of system reset button, RJ11 port(for configuring the boot parameters of EVM) and RJ-45 ethernet port (for UIP communication and software download).

3.1.1.1 Serial Port

The Serial Port (J9) is used for configuring the boot parameters for the EVM like IP Address for the EVM, IP Address for the Host PC, path to the Code Image. The user shall connect the COM port of the PC to the Serial port using an RJ-11 cable and DB-9F to RJ-11 adapter.

3.1.1.2 Ethernet Port

The Ethernet Port (J8) is used for software download via FTP and communicating with the TestExec(UIP) Software. The user shall connect this port to the LAN by the RJ-45 Twister Pair Cable.

3.1.1.3 System Reset

The System Reset button(S1) is used for reseting the Elgin Microprocessor Board. Please note that currently reseting the Elgin Microprocessor Board does not reset the LICs. Therefore it is advisable to either power cycle the Enhanced EVM or alternatively reset the ZipWirePlus LICs as well as the Elgin Microprocessor Board.

3.1.2 Aurora Motherboard

The Aurora mother board supplies the necessary regulated voltages to the LICs, Dual T1/E1 Framer card, and Elgin Microprocessor board. It comprises of four slots. The

Dual T1/E1 Framer shall be inserted into Slot 0, the ZipWirePlus LIC onto Slots 1 and 2, and the BNC Tester Card shall be inserted into Slot 3.

The Dual Power Supply (5V and 15 V) Brick shall be plugged into the J9 plug.

3.1.3 Dual T1/E1 Framer Card

The Dual T1/E1 Framer comprises of two Bt8370 framer devices. This card is used for providing PCM data to the ZipWirePlus LICs. It has the RJ-45 ports (J1 and J2) which can be connected to any T1/E1 tester.

3.1.4 ZipWirePlus LIC

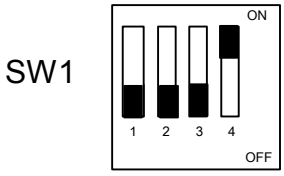
The ZipWirePlus LIC can be populated with the following four parts:

- M28945
- M28946
- M28947
- M28950

3.1.4.1 DIP Switch

The Motorola processor on the Elgin Microprocessor Board communicates to the ZipWirePlus devices through the Host Port. The DIP switch(SW1) should be configured for the Host Port Mode. Figure 3-1explains the DIP switch configuration.

Figure 3-1. DIP Switch Configuration for Communicating to the ZipWirePlus Device through the Host Port



3.1.4.2 DSL Line Port

The RJ-45 Port (J7) is used for connecting the LIC to the far end through a RJ-45 Twisted pair Cable.

3.1.4.3 System Reset

The System Reset button(SW3) is used for reseting the ZipWirePlus LIC. Please note that after pressing the Reset button, firmware would need to be downloaded to the ZipWirePlus device.

3.1.4.4 Master/Slave

All the ZipWirePlus LICs ship with the following two modifications.

- J22 (1,2 Shorted with a Jumper)
- J20 (5,6 Shorted with a Jumper)

Please check whether the following two modifications have been made on the ZipWirePlus LICs.

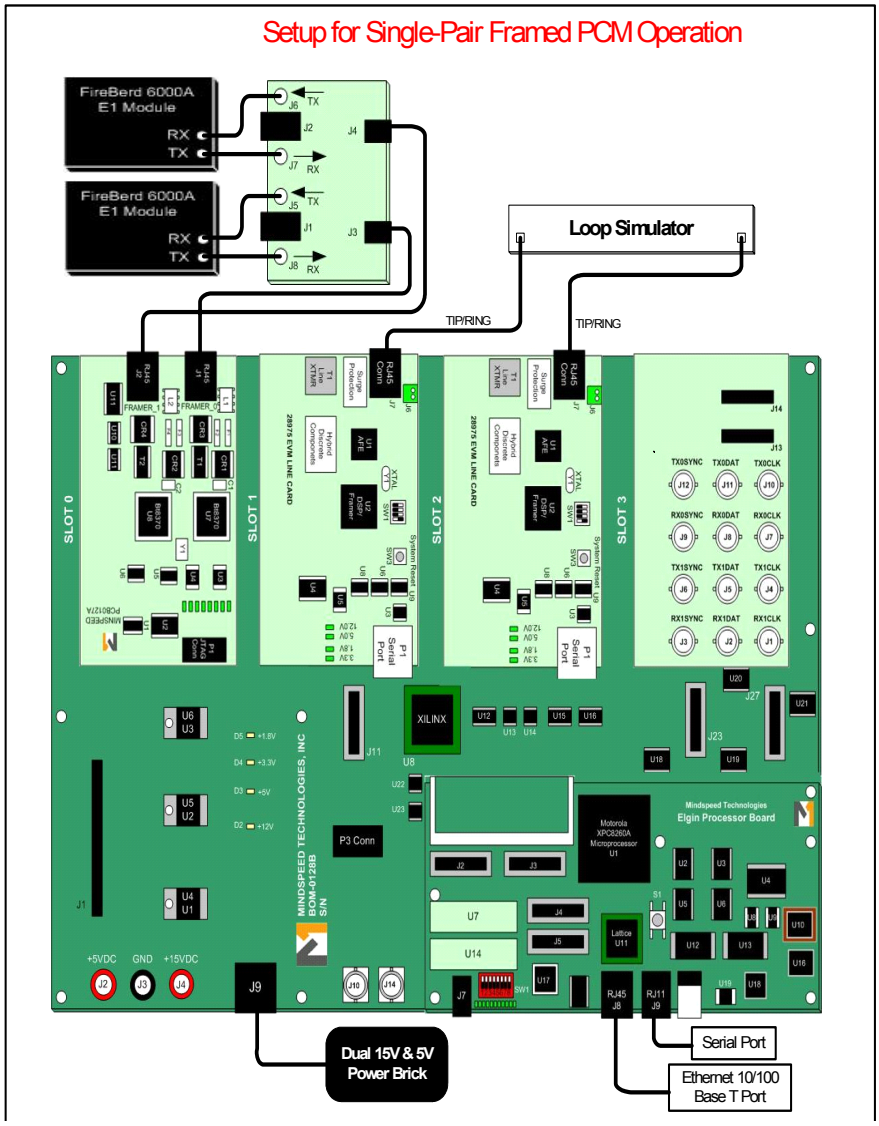
NOTE: The J20 Jumper should be removed from the Slave device for all the Multi-Pair Applications. The J20 Jumper should be present for all single pair applications and for the Master device of MultiPair Applications. The J22 Jumper should be present for all Applications.

3.2 Enhanced EVM Setup for Single Pair Framed PCM Operation

The following steps are required to set up the ZipWirePlus Enhanced EVM for Single Pair Framed PCM Operation. This setup needs only one Enhanced EVM.

NOTE: The Fireberd must be equipped with a 2M/ nX64 interface (E1 Module) to proceed with the setup described in this section. Figure 3-2 illustrates the required interconnections.

Figure 3-2. Enhanced EVM Setup for Single Pair Framed PCM Operation



3.2.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively. The BNC Tester Card is plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.

4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Set up for Zero Loop Length - Connect the RJ-45 cable (provided) from J7 of one ZipWirePlus LIC to J7 of the other ZipWirePlus LIC.
6. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
7. Fireberd Connections:

   a) Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-C card.

   b) Fireberd #2 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_1 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-R card.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into socket J9 of the Enhanced EVM.

3.2.2 Fireberd Setup

Configure the Fireberd #1 E1 Module front panel as follows:

- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kHz
- INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
- INTF SETUP: 2M/n64: MODE: FULL2M

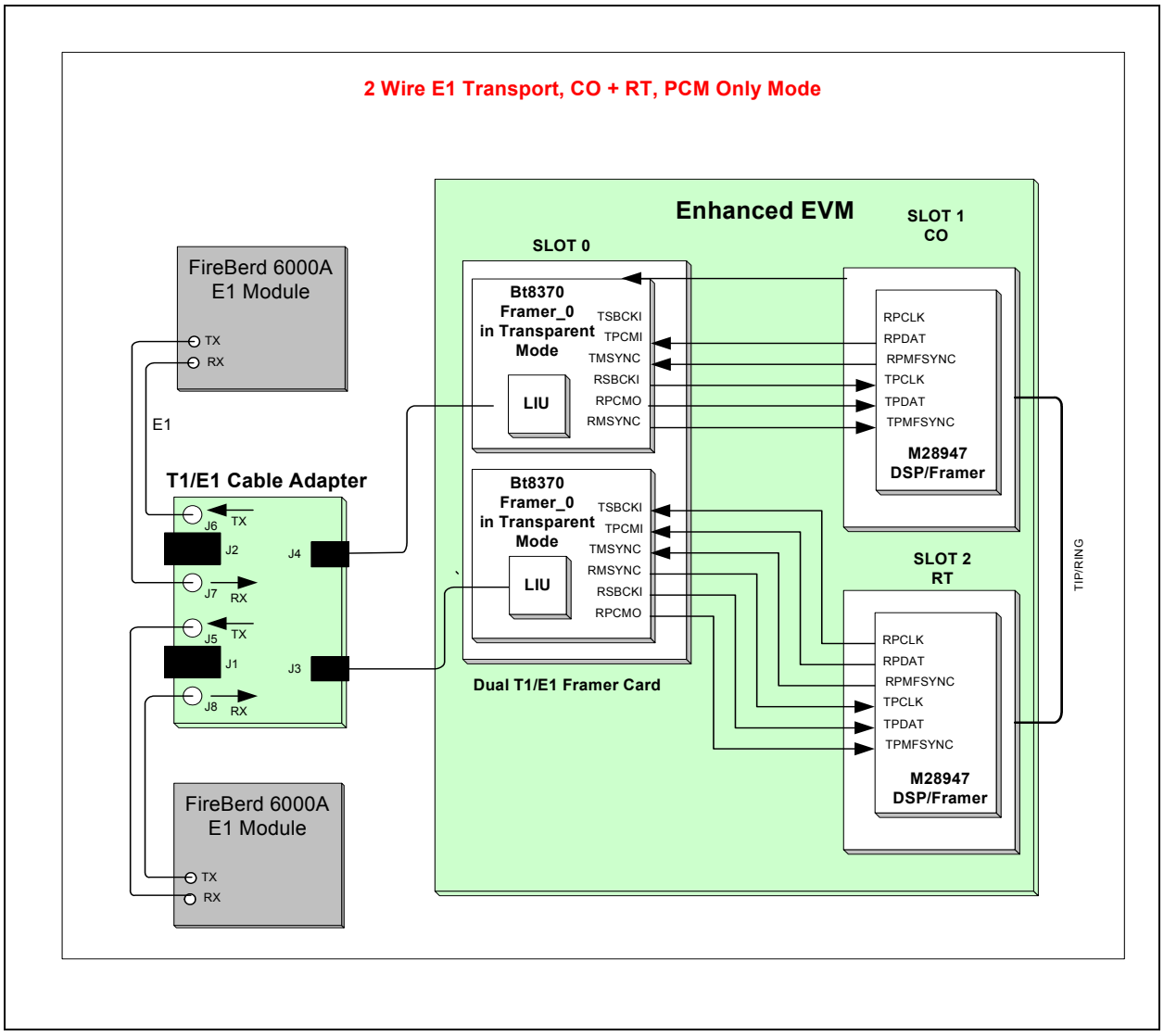
Configure the Fireberd #2 E1 Module front panel the same way as above.

3.2.3 FPGA Configuration

The Host Code configures FPGA(U8) into one of the many possible configurations through the TestExec (UIP) GUI.

This configuration will connect the PCM bus of the ZipWirePlus device (slot 1) to the Framer #0 (slot 0) and the PCM bus of the ZipWirePlus device (slot 2) to the Framer #1 (slot 0). Figure 3-3 explains the pin interconnections for this application.

Figure 3-3. Connections for Single Pair Framed PCM Application



3.2.4 Enhanced EVM Configuration

3.2.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

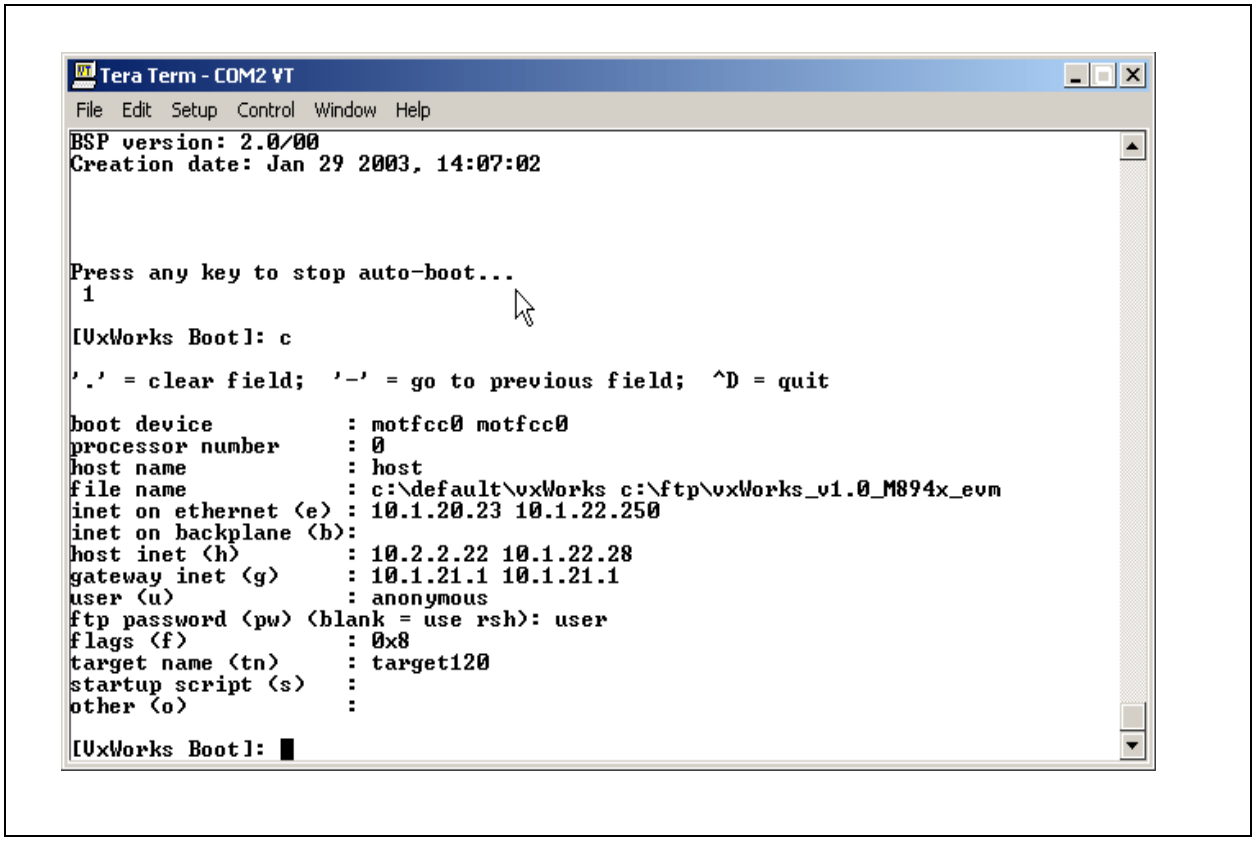
- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm)
- ZipWirePlus firmware image (VX_gshdsl_XXX_89XX.hex file) - Any of the G.shdsl hex files can be used for this configuration.

3.2.4.2 First Time Power Up

This section outlines the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

1. Power up the Enhanced EVM.
2. Monitor the output on the serial console on the PC.
3. When the board boots, you will be prompted with a boot countdown, press a key to terminate the countdown.
4. Type 'c' and enter the required boot parameters.

Figure 3-4. Serial Console - Configuring Boot Parameters



- *bootdevice* - enter it to be motfcc0
- *Processor number* - Skip the field by pressing the <Enter> Key.
- *host name* - Skip the field by pressing the <Enter> Key.
- *file name* - Enter the pathname of the EVM Elgin Microprocessor Software Image. The path to this image is <Root>\Program Files\Mindspeed\ZipWirePlus Enhanced EVM\Software\EnhancedEvmSW\ftp\vX_X_M289XX_eevm.

The maximum size of the path name is 80 characters. So move the file to a folder such that the file path will not exceed 80 characters.

- *inet on ethernet (e)* - Enter the IP Address for the Enhanced EVM.
- *inet on backplane (b*) - Skip the field by pressing the <Enter> Key.
- *host inet (h)* - Enter the IP Address for the PC where the EVM Elgin Microprocessor Software Image is located.
- *gateway inet (g)* - Enter the IP Address for the gateway for the Enhanced EVM
- *user (u)* - Enter the username for the FTP Server.
- *ftp password (pw)* - Enter the password for the FTP Server.

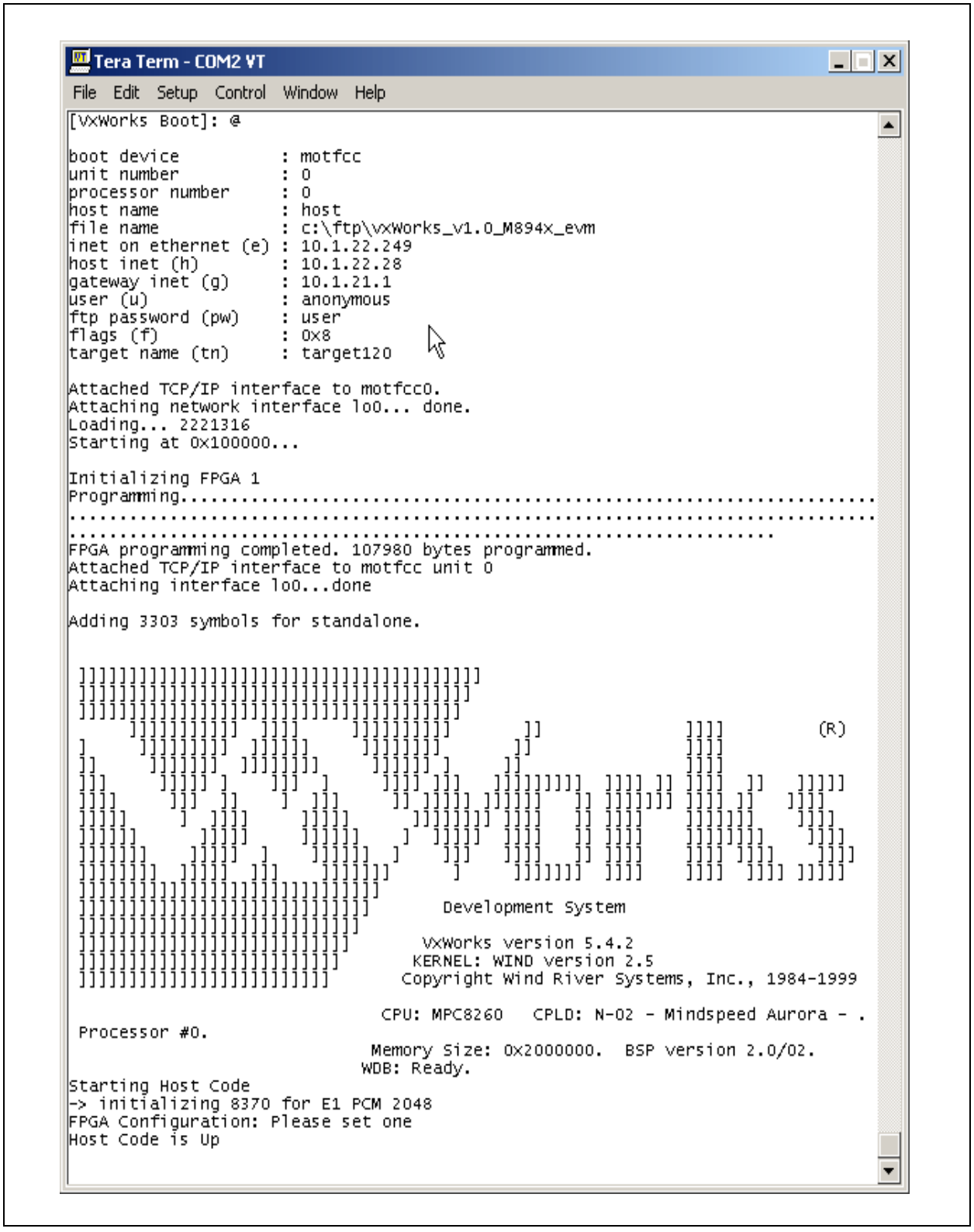
- *target name (tn)* - Skip the field by pressing the <Enter> Key.
- *startup_script (s)* - Skip the field by pressing the <Enter> Key.
- *other (o)* - Skip the field by pressing the <Enter> Key.

5. Start the FTP server.

If using the sample FTP Server, go to the folder <Root>\Program Files\Mindspeed\ZipWirePlus Enhanced EVM\Software\FTPServer.

6. Ensure the EVM Elgin Microprocessor Software Image (FTP image) and Hex file (ZipWirePlus Firmware Image) exist at the correct location. .
7. Type '@' and <Enter>
8. This will initiate the boot process. The EVM Elgin Microprocessor Software image will be fetched from the specified folder on the PC and shall be launched.
9. The following output shall be seen on the serial console.

Figure 3-5. Serial Console - Power up.



The software initializes the FPGA, initializes the Enhanced EVM and creates a socket for the TestExec/UIP Software.

10. Once the "`Host Code is Up`" message appears on the Serial Console, we are ready to start the TestExec Software.

3.2.4.3 Subsequent Power Ups

If the user has configured the boot parameters, the procedure defined in Section 3.2.4.2 can be skipped. Please follow the steps defined below:

1. Ensure the EVM Elgin Microprocessor Software Image (FTP image) and Hex file (ZipWirePlus Firmware Image) exist at the correct location. Any of the G.shdsl hex files can be used for this configuration.
2. Power up the Enhanced EVM.
3. Monitor the output on the serial console on the PC.
4. When the board boots, you will be prompted with a boot countdown, do not press a key.
5. The Enhanced EVM will boot up and fetch the EVM Elgin Microprocessor Software image will be fetched from the specified folder on the PC. The software shall be launched.
6. The following output will be displayed on the serial console.

Figure 3-6. Serial Console - Subsequent Powerups

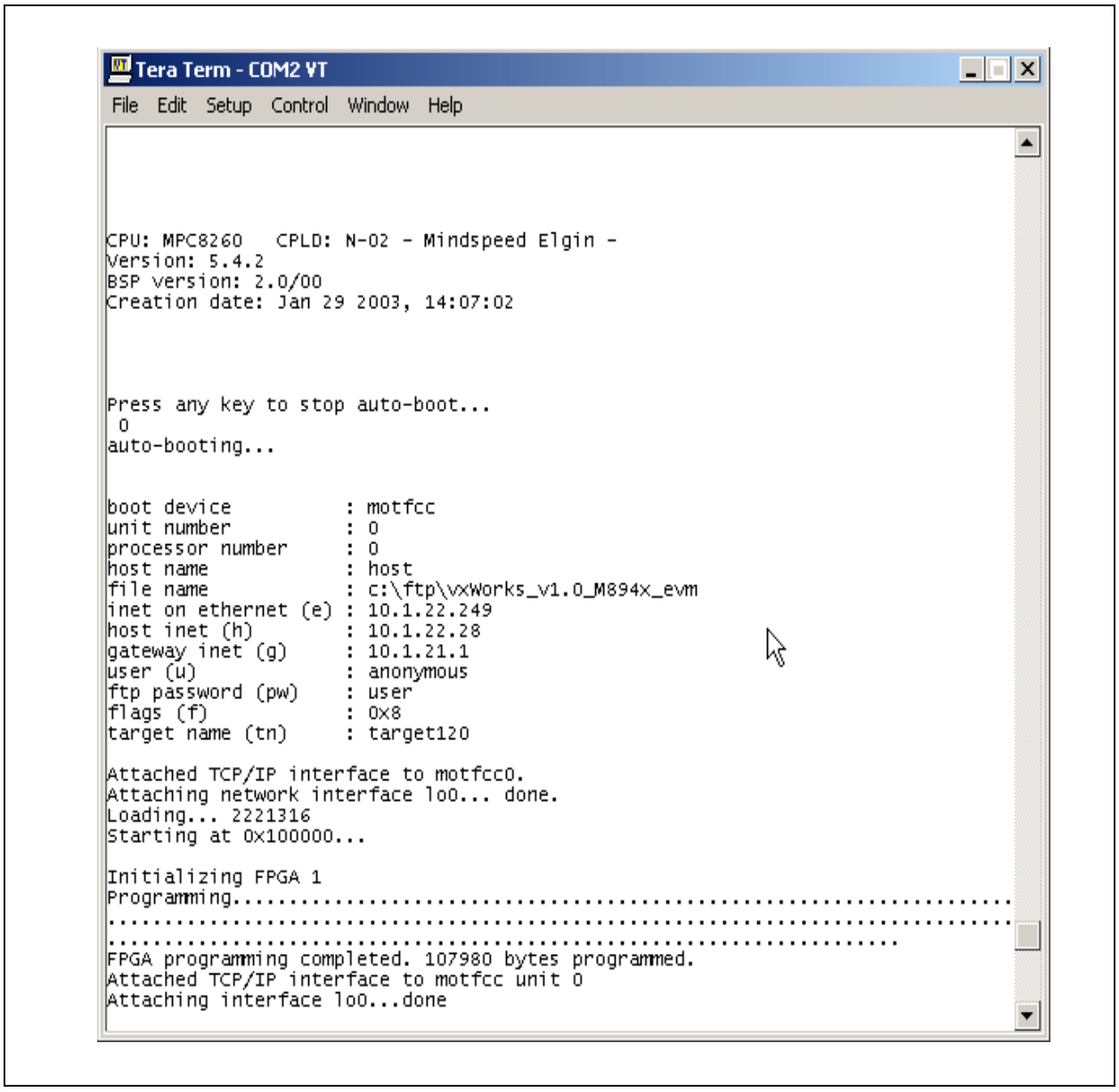
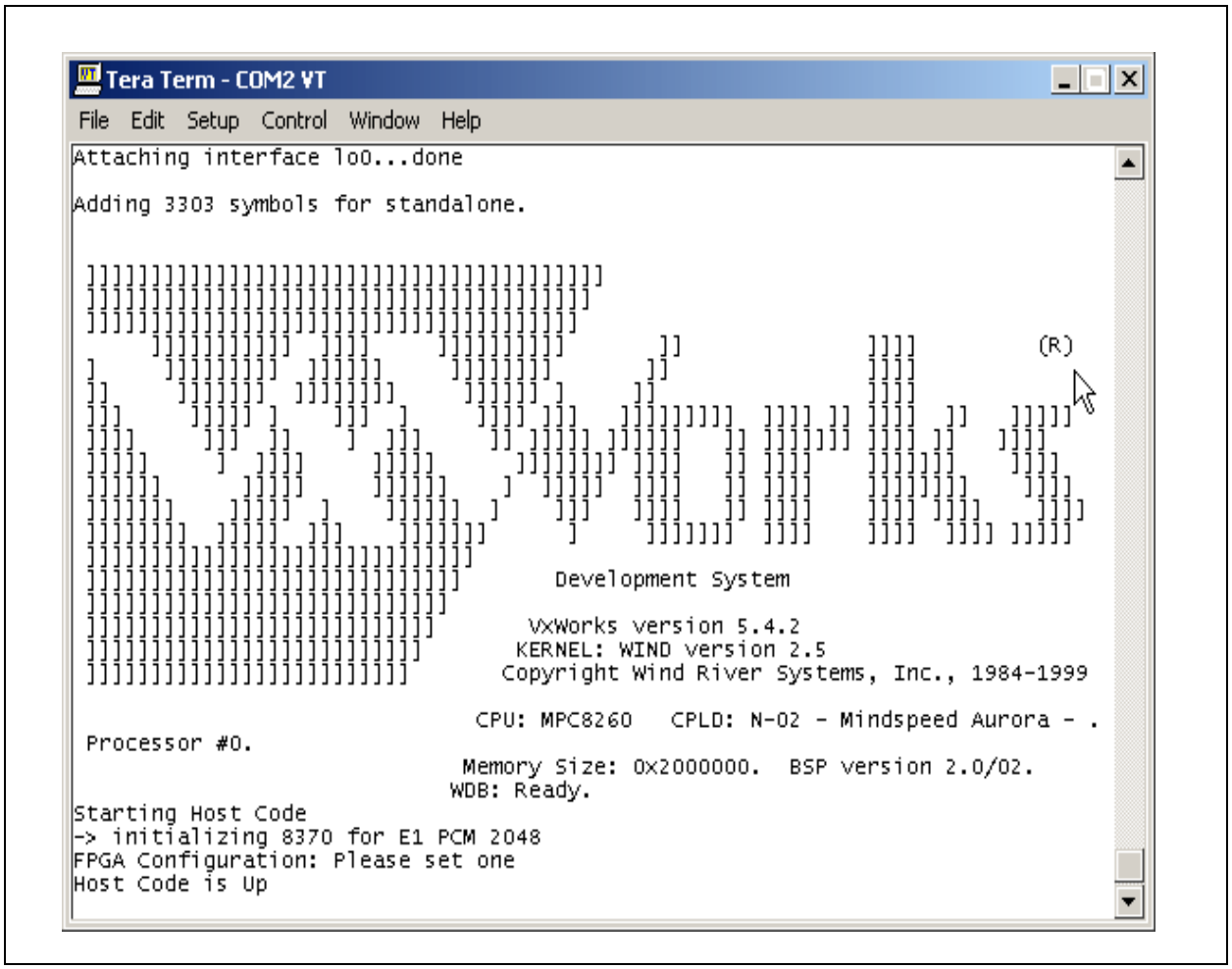


Figure 3-7. Serial Console - Subsequent Powerups - continued



7. The software initializes the FPGA, initializes the Enhanced EVM and creates a socket for the TestExec/UIP Software.
8. Once the "`Host Code is Up`" message appears on the Serial Console, we are ready to start the TestExec Software.

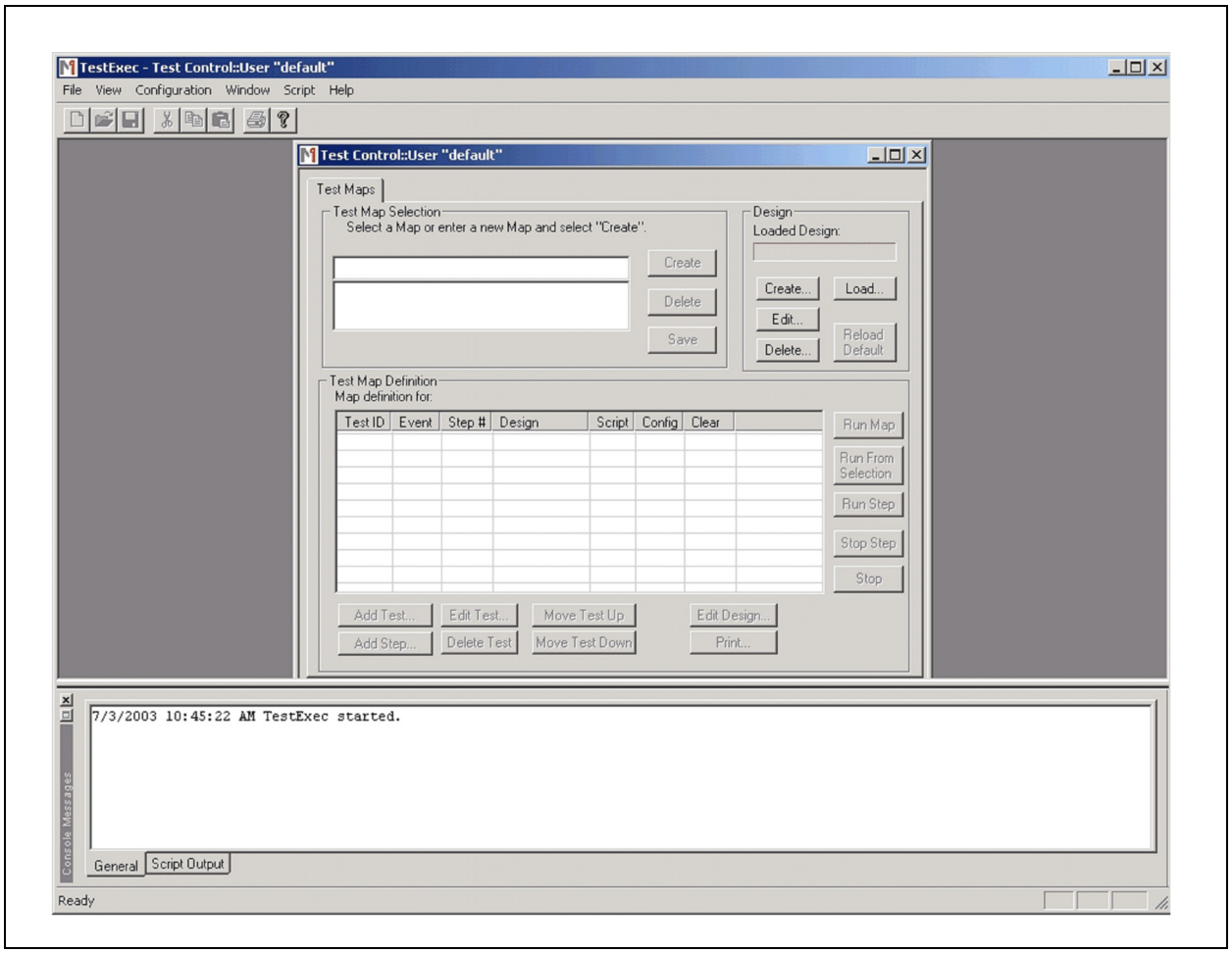
3.2.5 TestExec

3.2.5.1 Installation and Configuration

If this is the first time you are executing the TestExec please go through the following steps. Or else skip this section and go to Section 3.2.5.2.

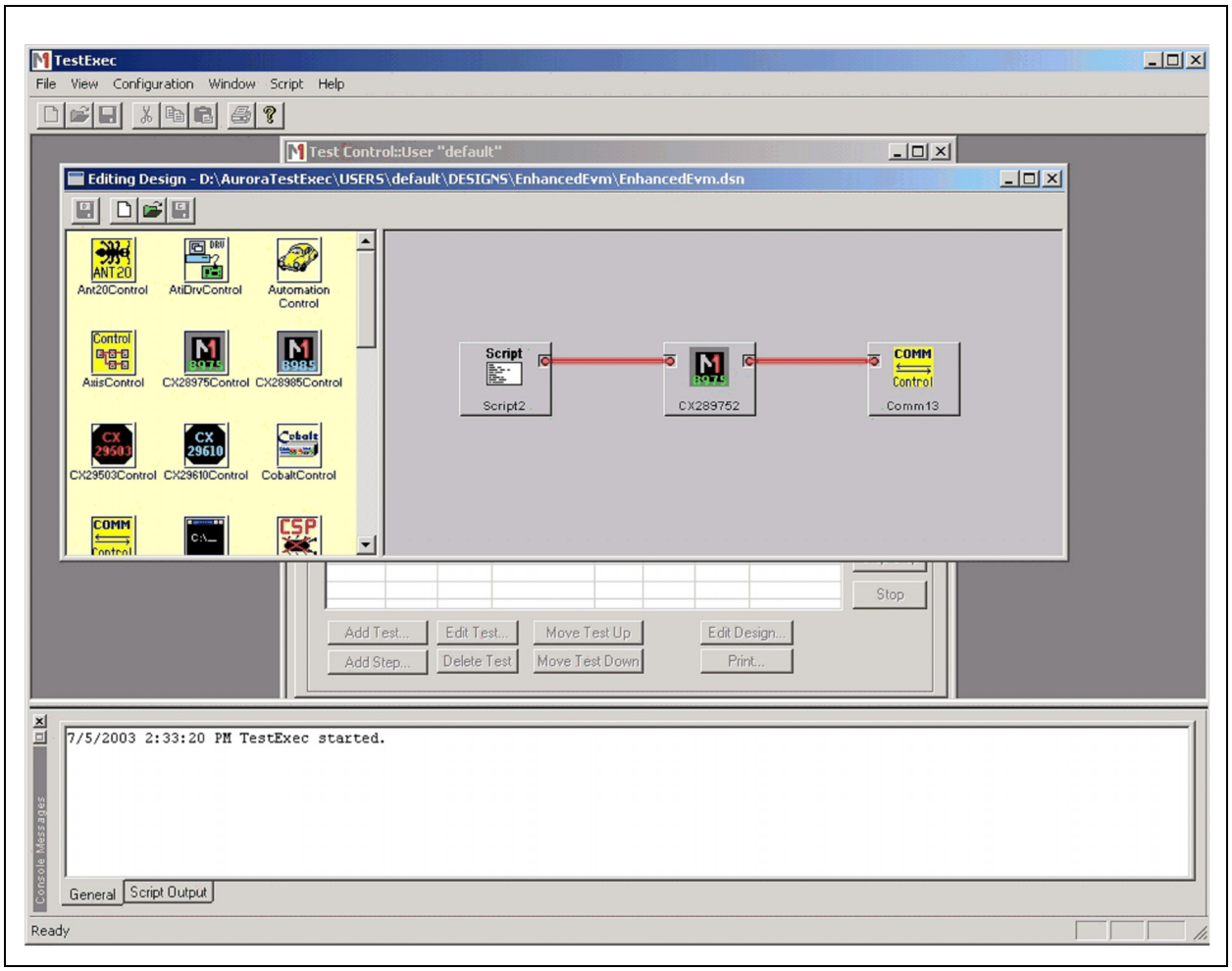
1. Install the ZipWirePlus TestExec (UIP) by installing the CD included in the Enhanced EVM Package into the host PC.
2. Run the Testexec.exe from the desktop.
3. The TestExec application will startup and displays the following screen.

Figure 3-8. TestExec Main GUI



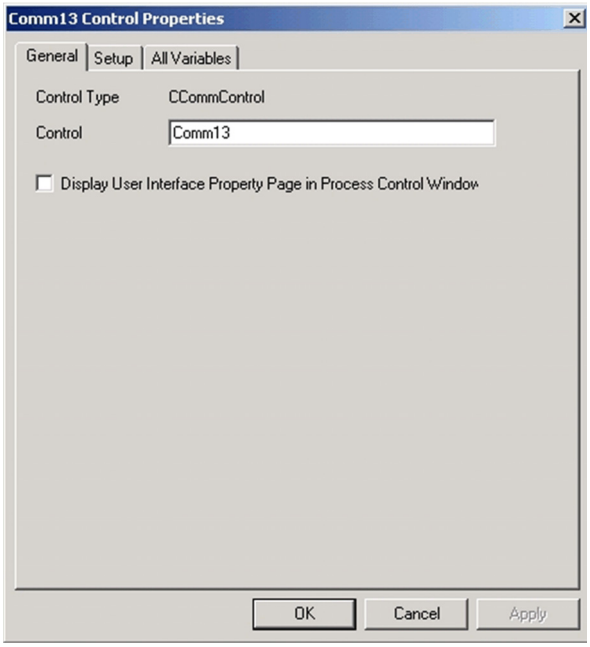
4. The TestExec requires a design file to communicate with the Enhanced EVM. The TestExec is shipped with sample design files (EnhancedEvm.dsn, EnhancedEvm2.dsn). Press on the **Edit** button.
5. The Test Exec will prompt you with a menu containing 3 design files
   - **EnhancedEvm**
   - **EnhancedEvm2**
   - **LegacyEvm**
6. Select the **EnhancedEvm** design file. The TestExec will load the chosen design configuration GUI.

Figure 3-9. Editing the Design File to configure the IP for the Enhanced EVM



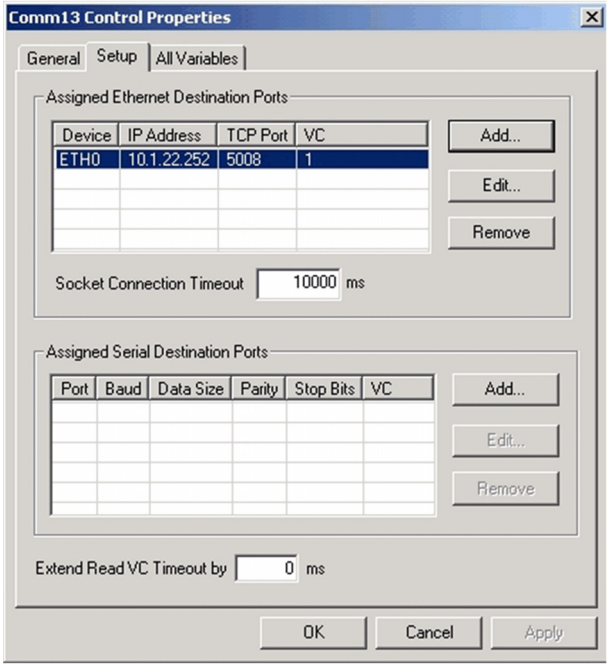
7. Right click the mouse on the **CommControl** Icon and choose **Properties**.
8. The TestExec will display the Control Properties for this icon.

Figure 3-10. Control Properties for CommControl Icon



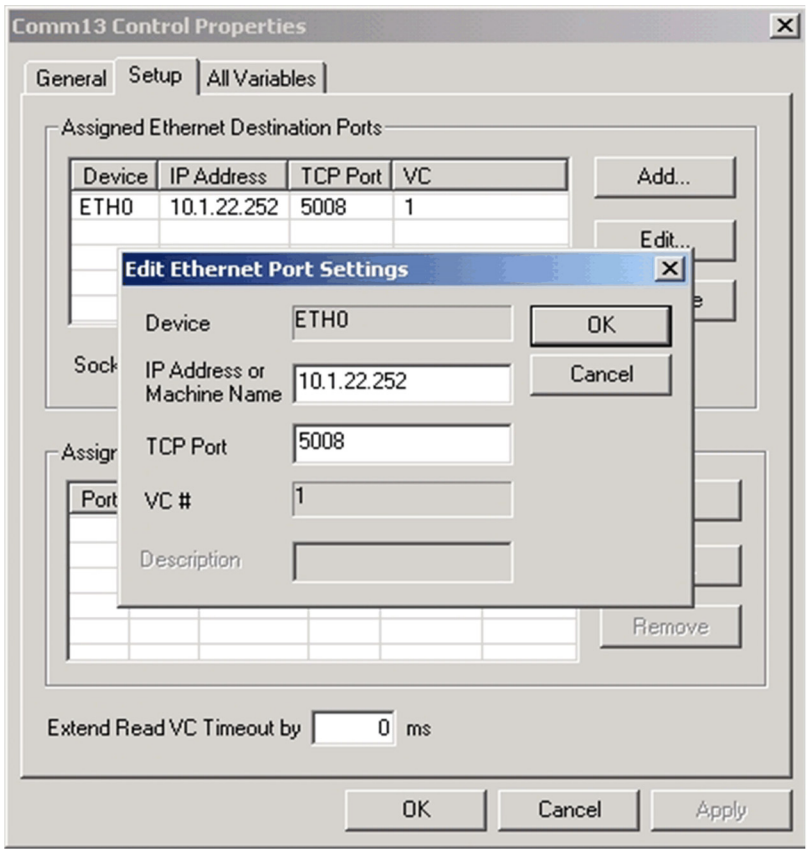
9. Click on the **Setup** Tab.

Figure 3-11. Setup Window for CommControl



10. Click on the **Edit** button.

Figure 3-12. Enter the IP Address for the Enhanced EVM

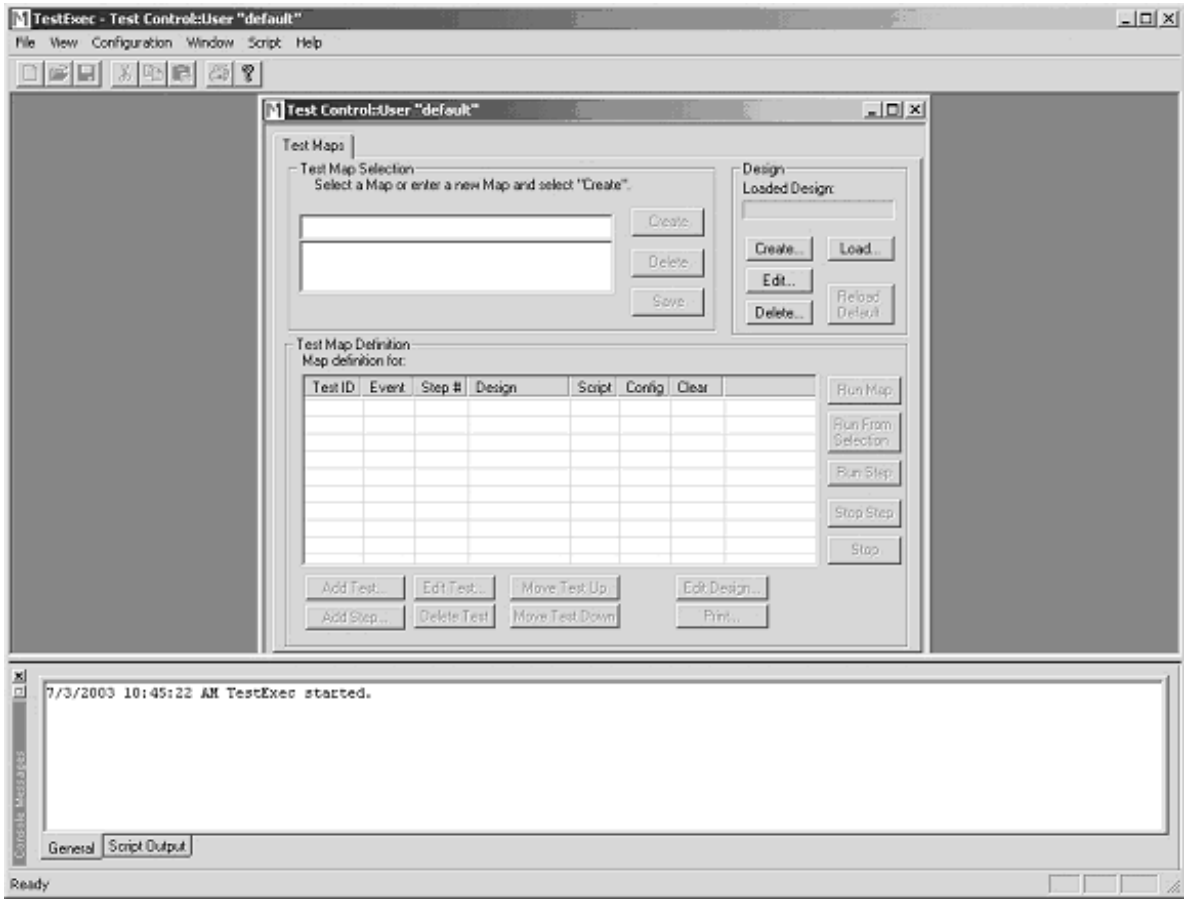


11. Edit the **IP Address** field and click OK.
12. Click **OK** on the Control Properties Window.
13. In the Main Design window, click on the **Save** icon to save the design file. The TestExec will prompt the user when the Design File is saved.
14. Close the Design File.

3.2.5.2 Enhanced EVM Configuration

1. Run **Testexec.exe** from the desktop.
2. The TestExec application will startup and displays the following screen.

Figure 3-13. Testexec Main GUI upon Launch



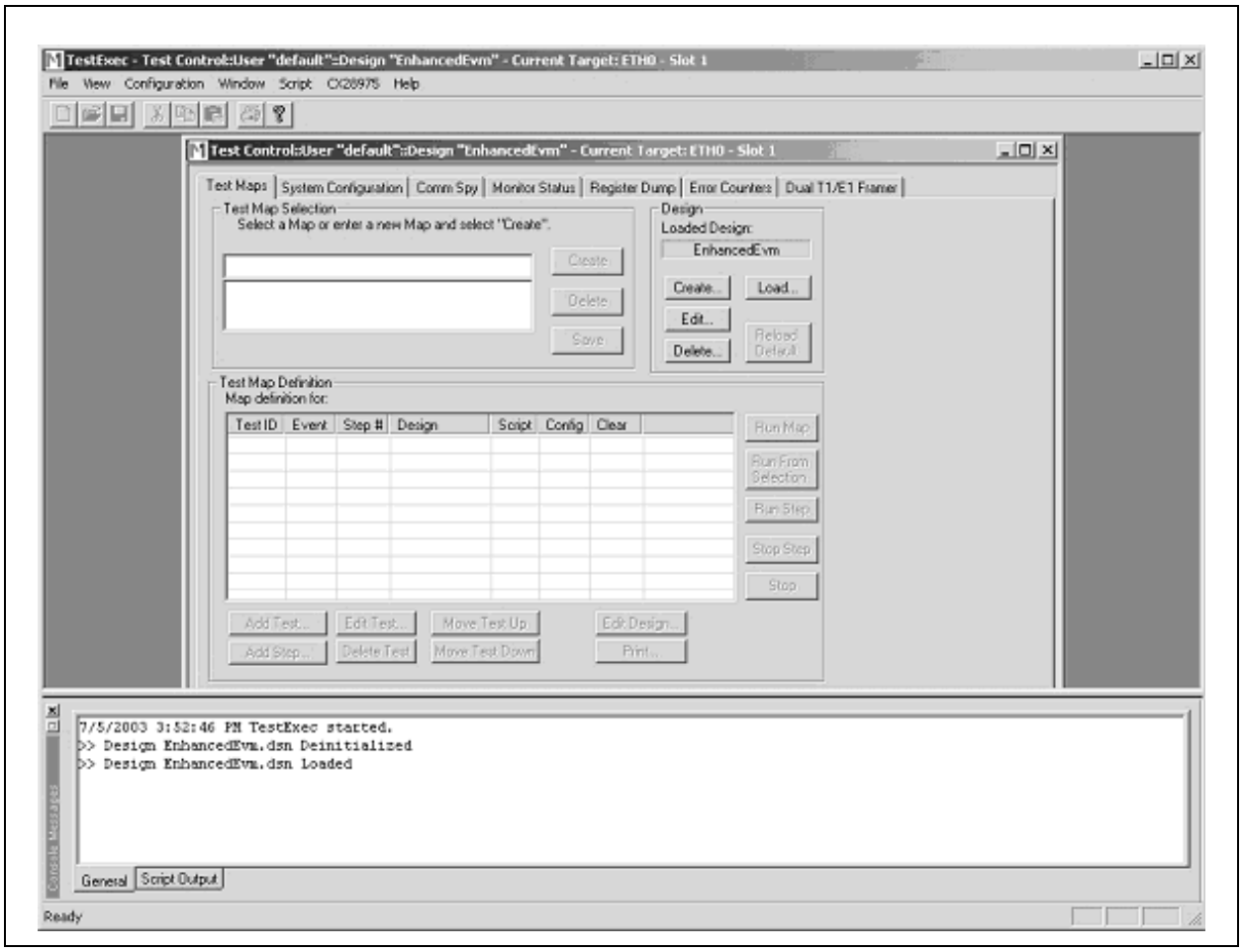
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

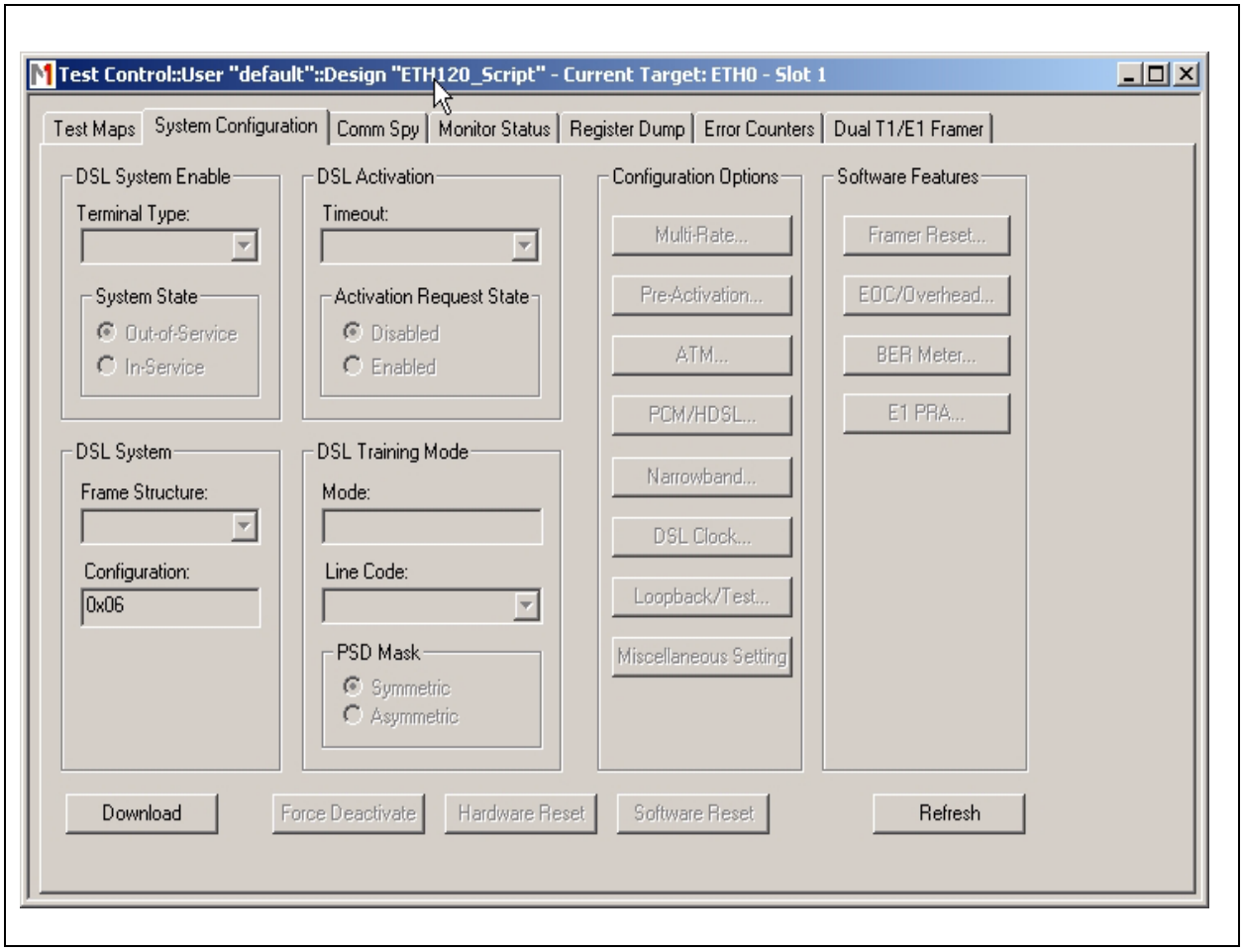
   c.**LegacyEvm**
5. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.

Figure 3-14. TestExec GUI after Design File is Loaded



6. Click on the **System Configuration** Tab.

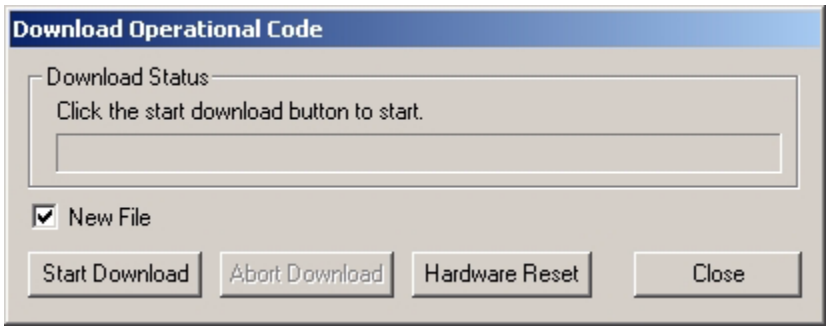
Figure 3-15. TestExec System Configuration Window



3.2.5.2.1 Code Download

1. Download the code to the ZipWireDevice device on Slot 1 by clicking on the **Download** button.

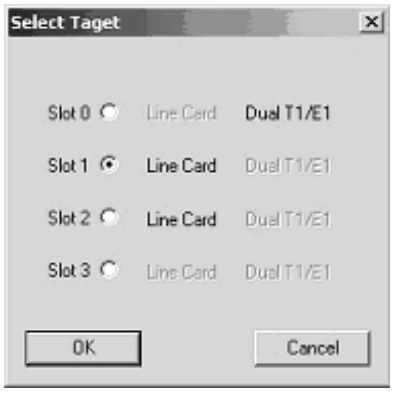
Figure 3-16. Downloading code to the ZipWirePlus device



2. Click on **New File** and specify the path to the hex file.
3. The Testexec will start the code download and prompt the user, once its done.

4. The Enhanced EVM has four slots - starting from zero. Select the slot to be configured by right clicking the mouse. The following menu appears.

Figure 3-17. Selecting the Slot

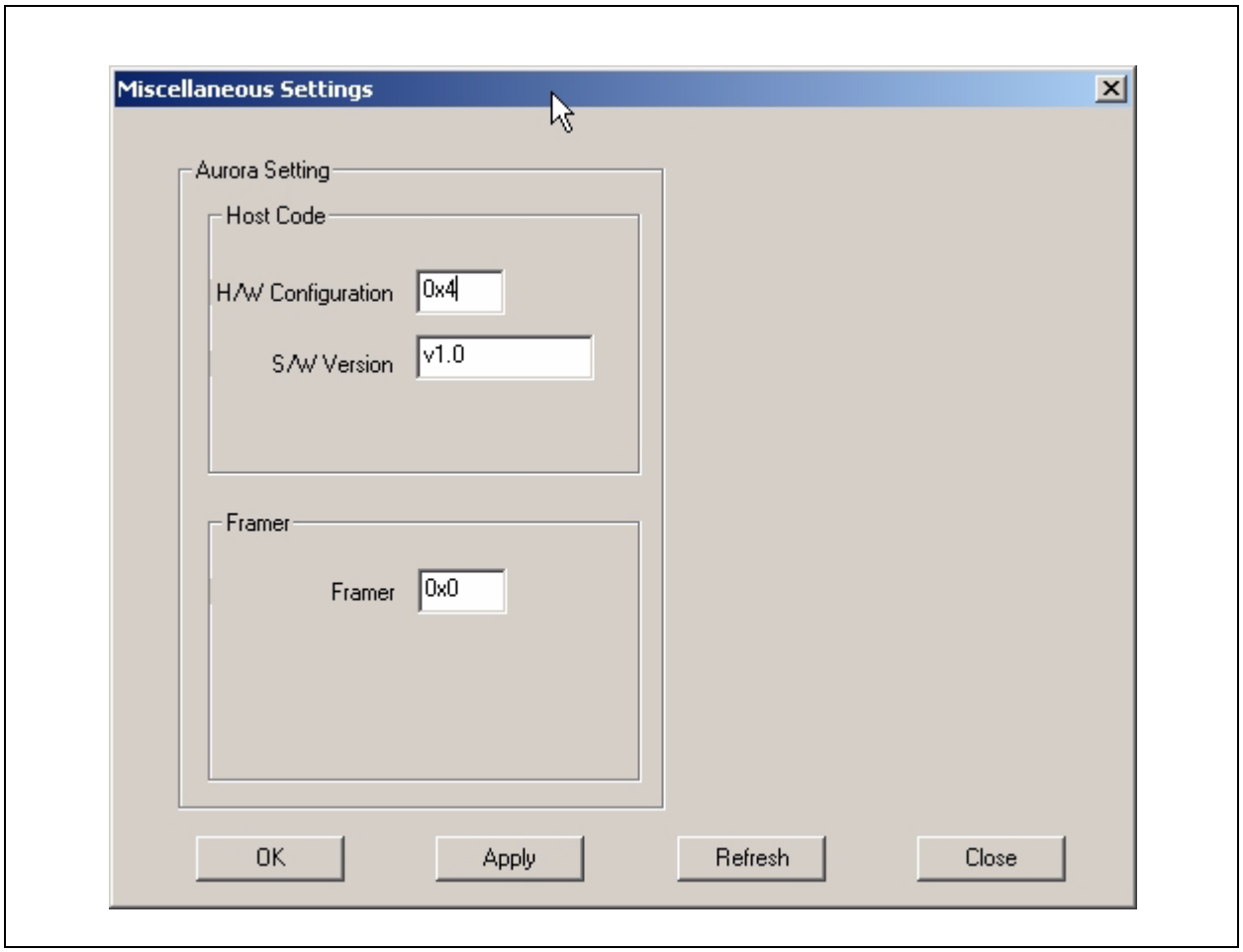


5. Select **Slot 2**.
6. Download the code to the ZipWireDevice device on Slot 2 by clicking on the **Download** button.
7. Click on **New File** and specify the path to the hex file.
8. The Testexec will start the code download and prompt the user once its done..

3.2.5.2.2 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0x4.
4. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-18. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

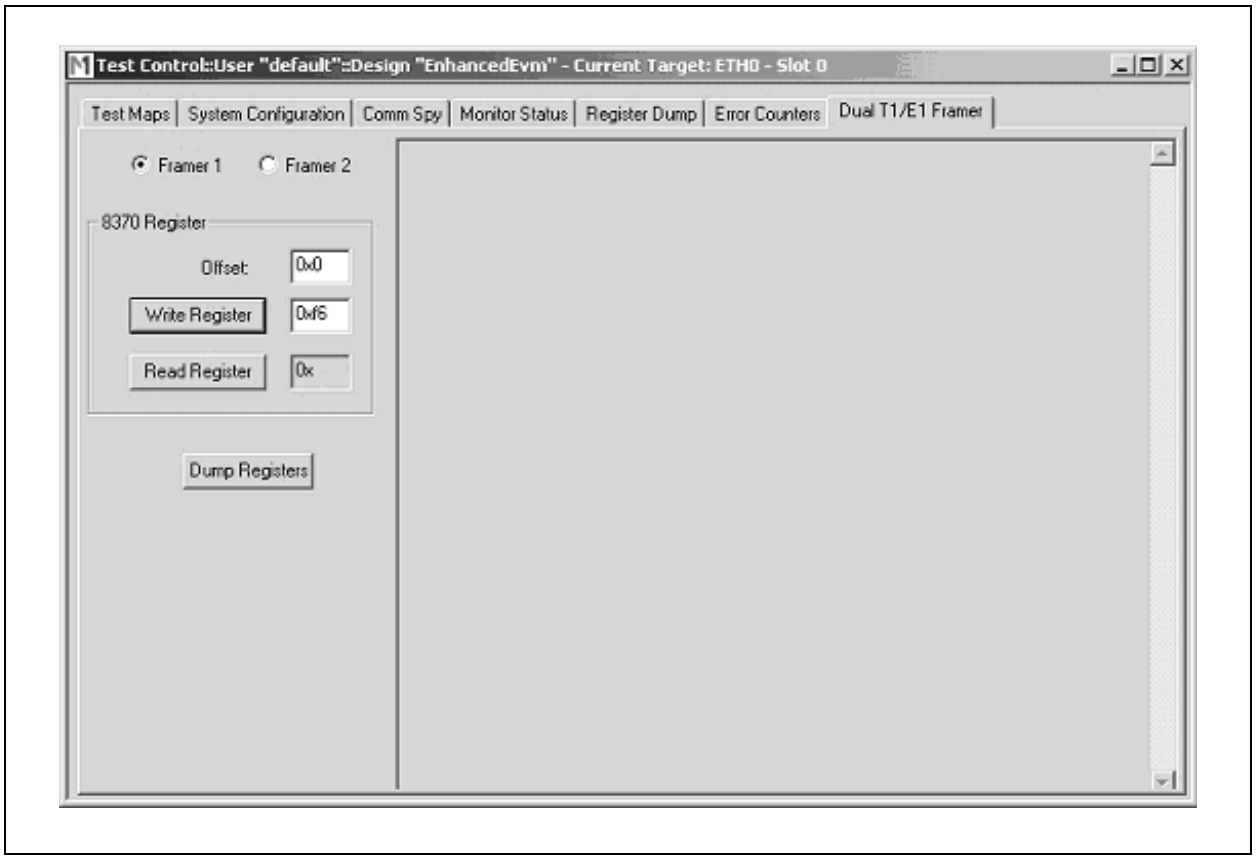


5. Select **Slot 0** i.e. Dual T1/E1 Framer card.

3.2.5.2.3 Slot 0 (Dual T1/E1 Framer card)

1. Click on the **Dual T1/E1 Framer** tab.
2. This window is used to read and write registers of the Bt8370 device.

Figure 3-19. TestExec Dual T1/E1 Framer Window



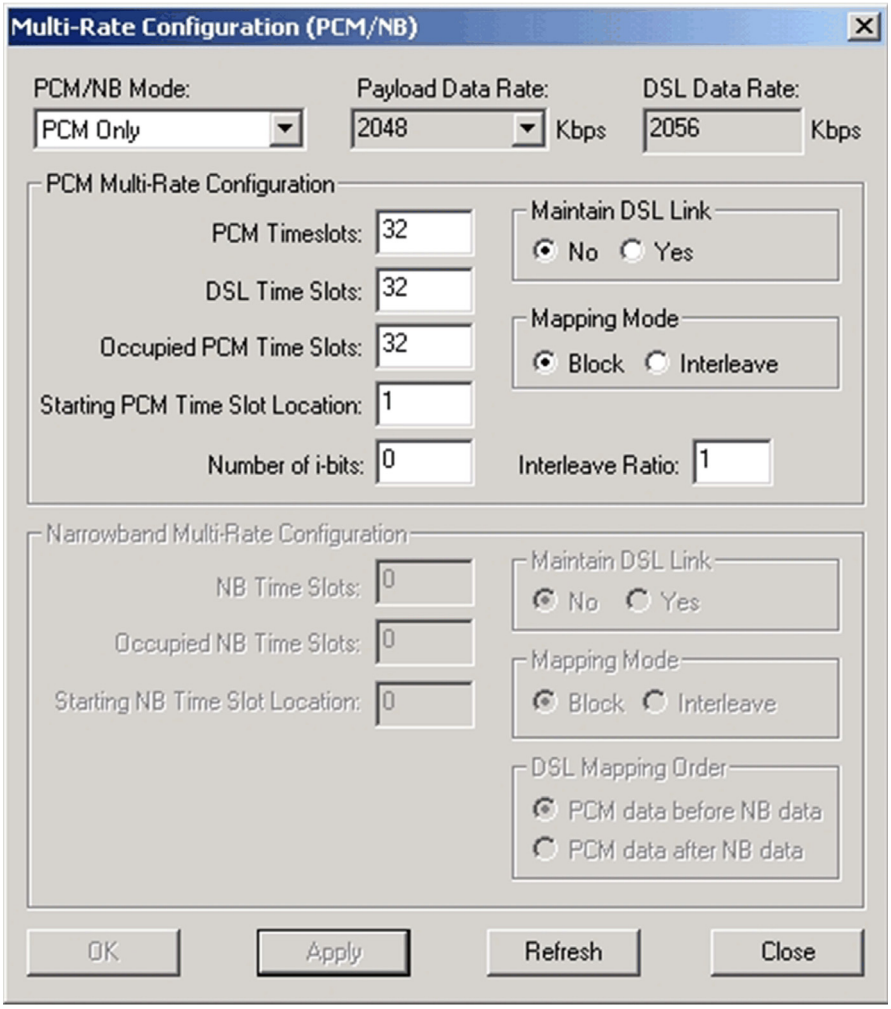
3. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.

3.2.5.2.4 Slot 1 (HTU-C Side)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the Values:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

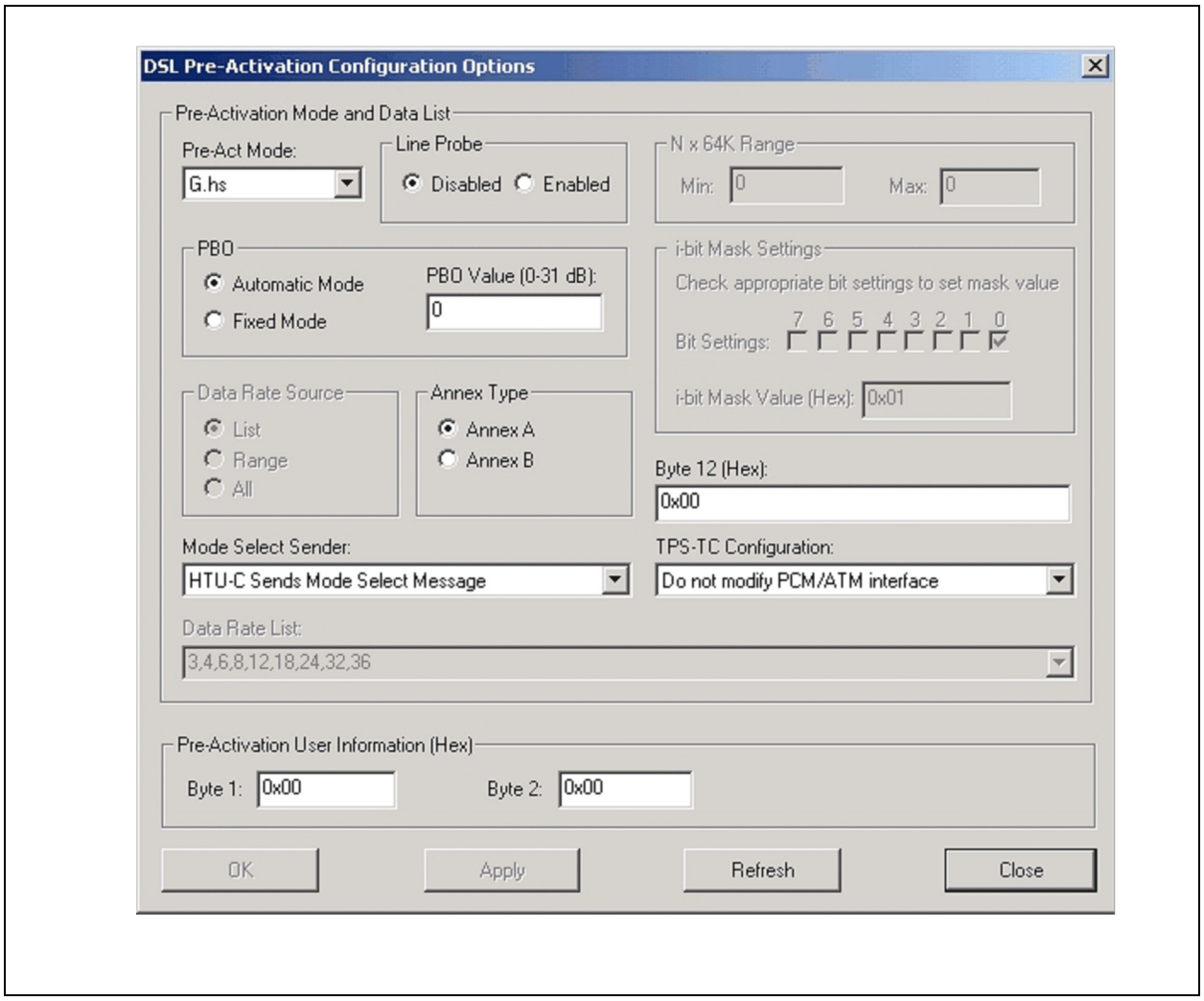
Figure 3-20. TestExec Multi-Rate Configuration for CO



Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.

5. Click on the **Pre-Activation** button.

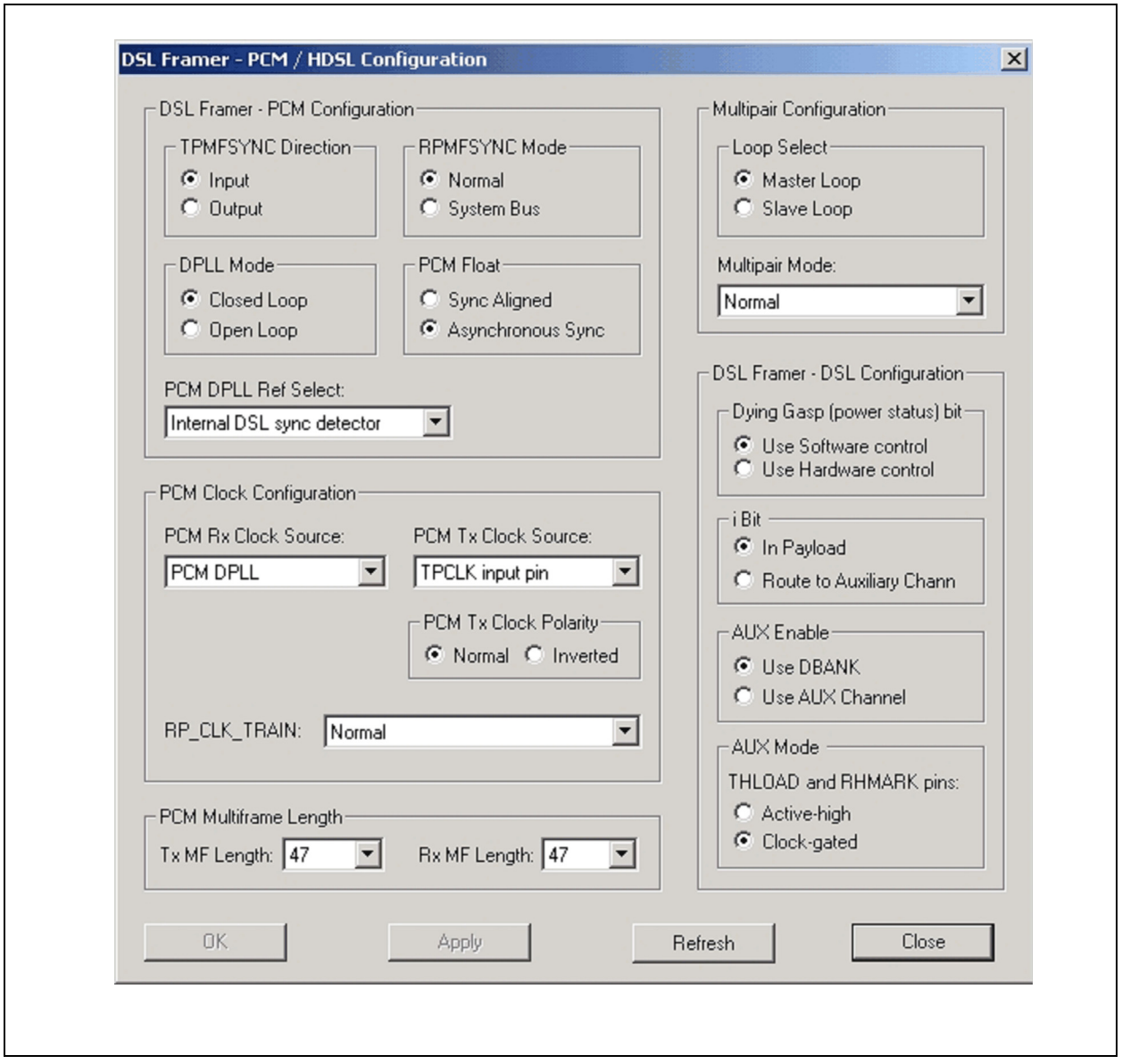
Figure 3-21. TestExec Preactivation Configuration for CO



6. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
7. Click on the **Apply** button and then click on the **Close** button.
8. Click on the **PCM/HDSL** button. Enter the following values:
   - DSL framer - PCM Configuration
     - TPMFSYNC Direction - **Input**
     - RPMFSYNC Mode - **Normal**
     - DPLL Mode - **Closed Loop**
     - PCM Float - **Asynchronous Sync**
     - PCM DPLL Ref Select - **Internal DSL Sync Detector**
   - PCM Clock Configuration
     - PCM Rx Clock Source - **PCM DPLL**
     - PCM Tx Clock Source - **TPCLK Input**
     - PCM Tx Clock Polarity - **Normal**
     - RP_CLK_TRAIN - **Normal**
   - PCM Multiframe Length

  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

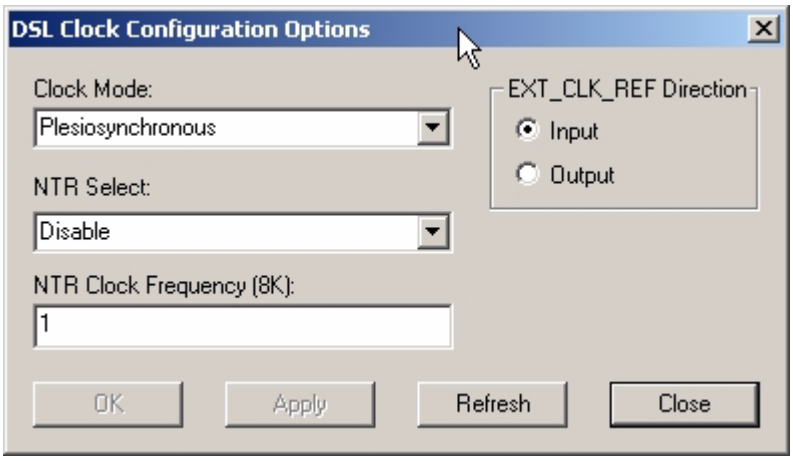
Figure 3-22. TestExec PCM/HDSL Configuration for CO



9. Click on the **Apply** button and then click on the **Close** button.

10. Click on the **DSL Clock** Button.
11. Enter the following values:

Figure 3-23. TextExec DSL Clock Configuration for CO



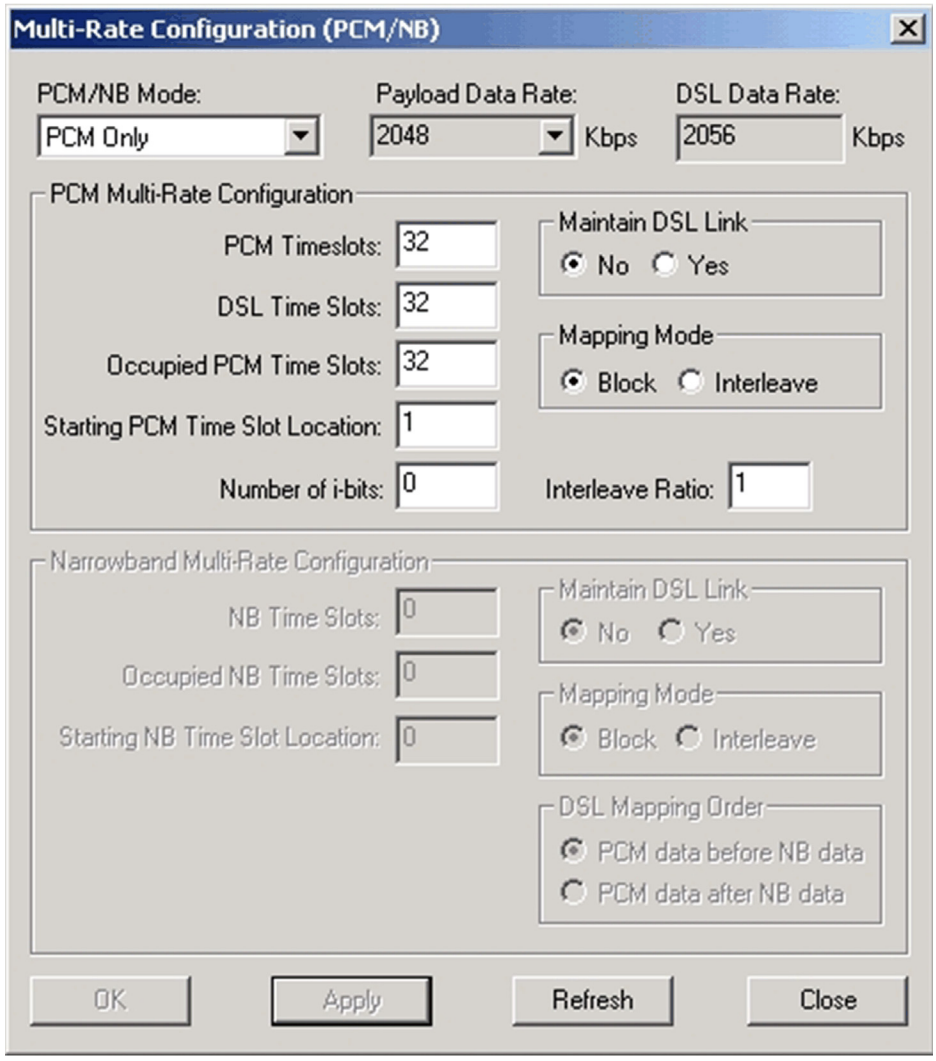
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
13. Change to Slot 2 by right clicking the mouse button and selecting **Slot 2.**

3.2.5.2.5 Slot 2 (HTU-R Side)

1. Click on the **System Configuration** tab.
2. Set the **Terminal Type** to **HTU-R**.
3. Set the **System State** to **In-Service**.
4. Click on **Multi-Rate Button**.
5. Enter the values:

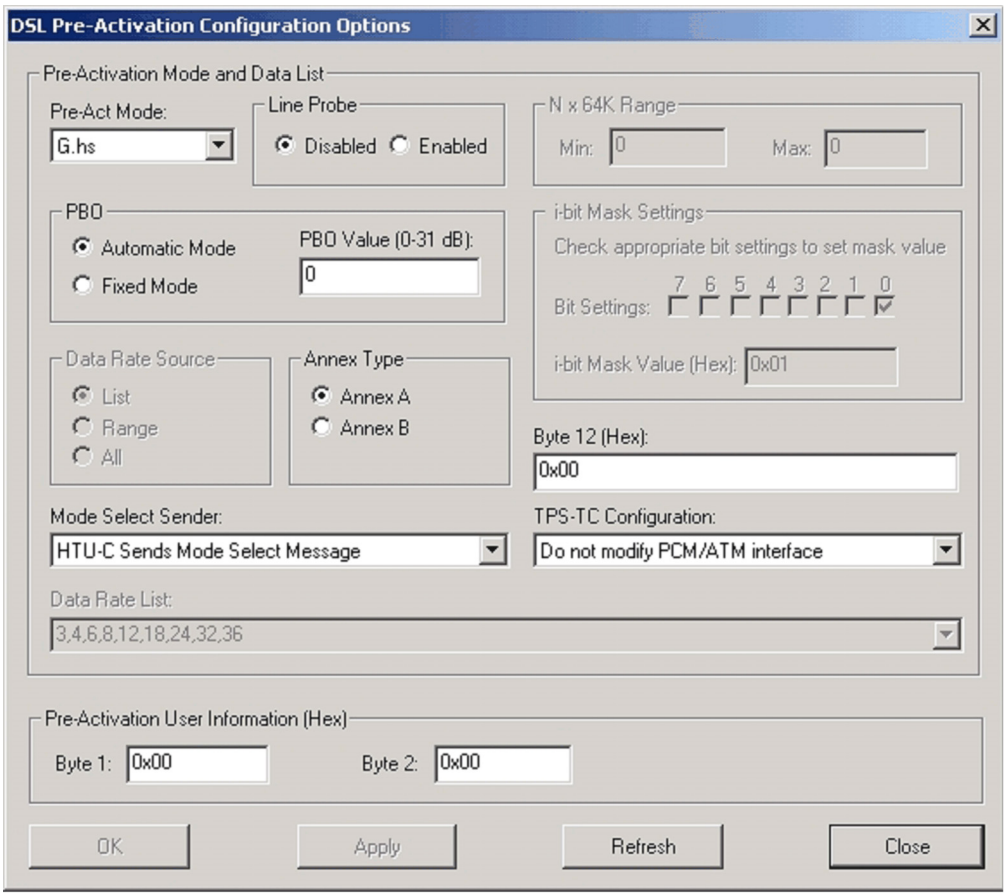
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-24. TestExec Multi Rate Configuration for RT



6. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

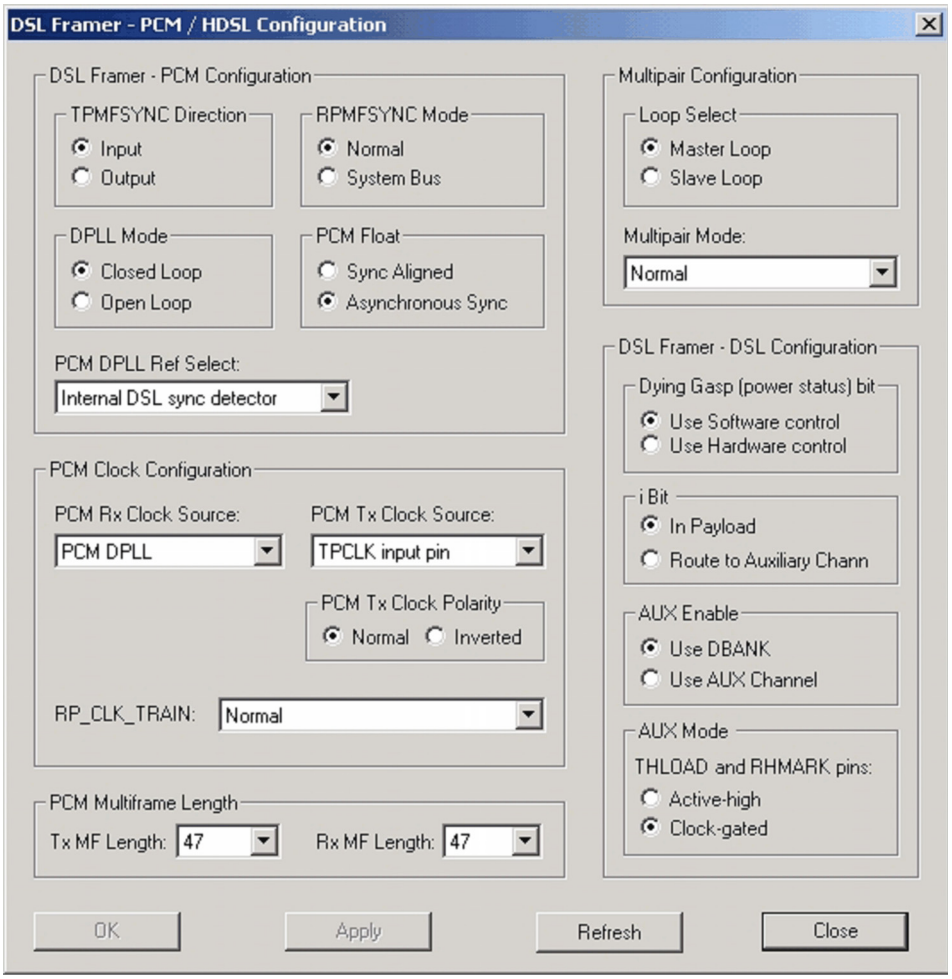
Figure 3-25. TestExec Preactivation Configuration for RT



8. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      - TPMFSYNC Direction - **Input**
      - RPMFSYNC Mode - **Normal**
      - DPLL Mode - **Closed Loop**
      - PCM Float - **Asynchronous Sync**
      - PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      - PCM Rx Clock Source - **PCM DPLL**
      - PCM Tx Clock Source - **TPCLK Input**
      - PCM Tx Clock Polarity - **Normal**
      - RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length
      - Tx MF Length - **47**

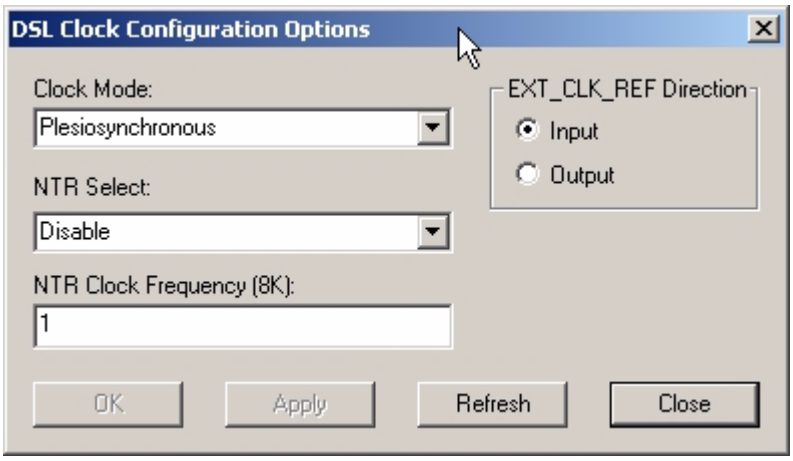
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-26. TestExec PCM/HDSL Configuration for RT



11. Click the **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-27. TextExec DSL Clock Configuration for RT

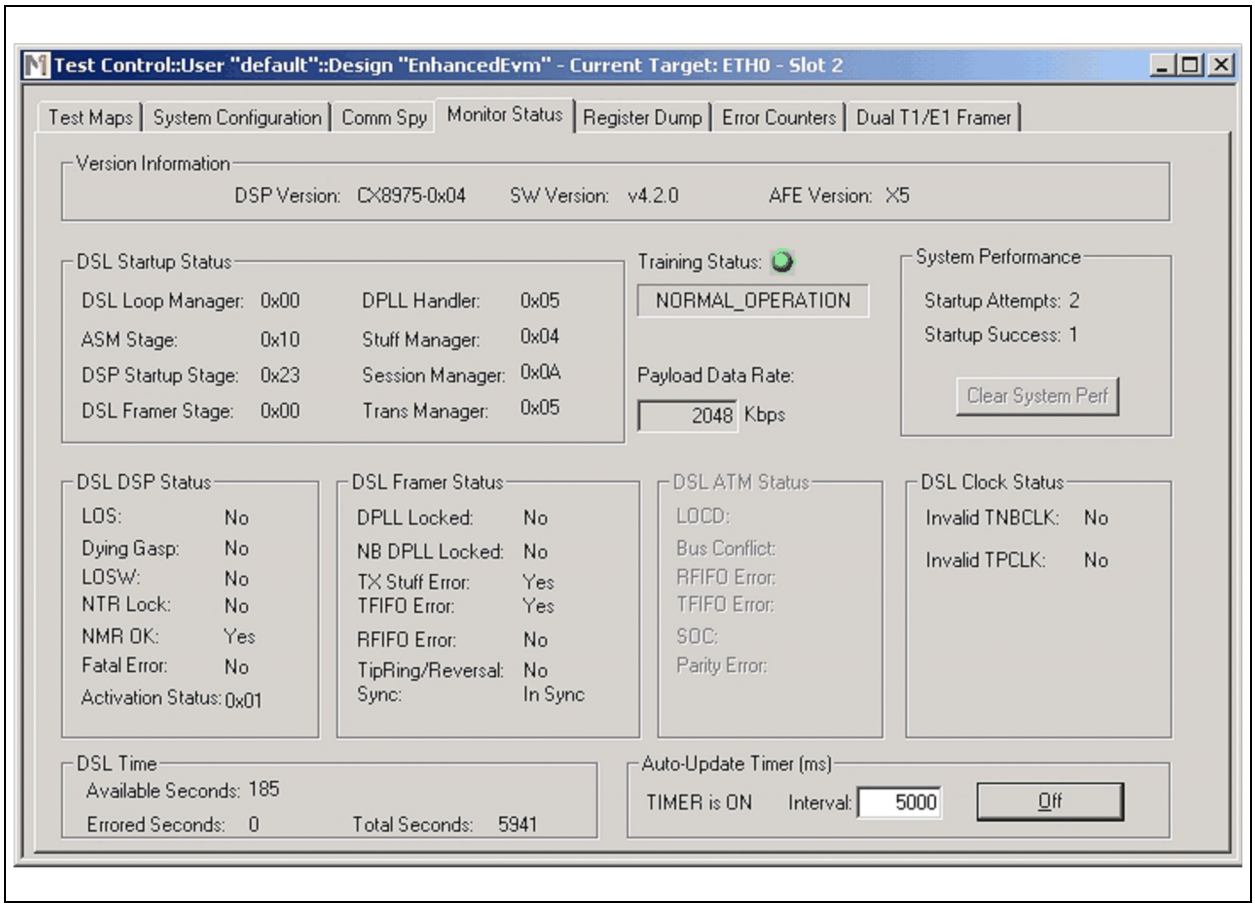


14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.2.5.2.6 Monitor the Link

1. Click on the **Monitor Status** tab for Slot 1 or Slot 2.
2. Click the **Set** button in the **Auto Update Timer** box.
3. The following output shall appear on the screen indicating the status of the Enhanced EVM.
4. Verify that the Fireberd is in sync and it has zero bit errors.

Figure 3-28. Monitoring the DSL Link



3.2.6 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM system. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulator using RJ-45 cables (provided) as shown in the Figure 3-2. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

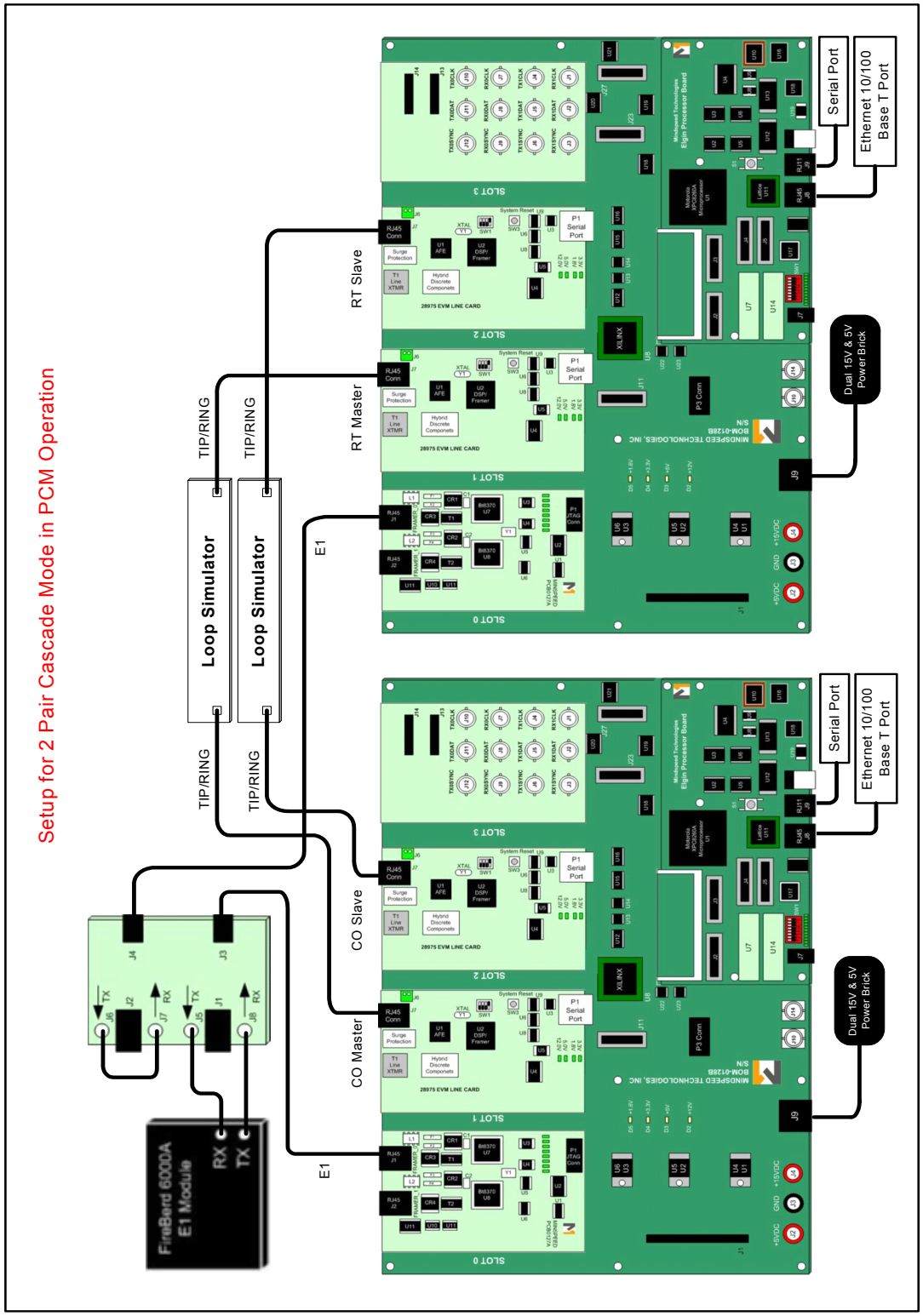
3.3 Enhanced EVM Setup for Multi-pair Cascade Mode in Framed PCM Operation

The following steps are required for running the ZipWirePlus Enhanced EVM in Multi-Pair Cascade Mode Framed PCM Operation. This setup needs two enhanced EVMs.

First, we shall use only the HTU-C EVM and put the DSL side is put into loopback. Then we shall perform end to end testing with two enhanced EVMs. The Hardware setup for this application is shown in Figure 3-29.

NOTE: The Fireberd must be equipped with a 2M/ nX64 interface (E1 Module) to proceed with the setup described in this section. Figure 3-29 illustrates the required interconnections.

Figure 3-29. Enhanced EVM Setup for Two-Pair Framed PCM Operation



3.3.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -
7. Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-C Master and HTU-C Slave cards.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.3.2 Fireberd Setup

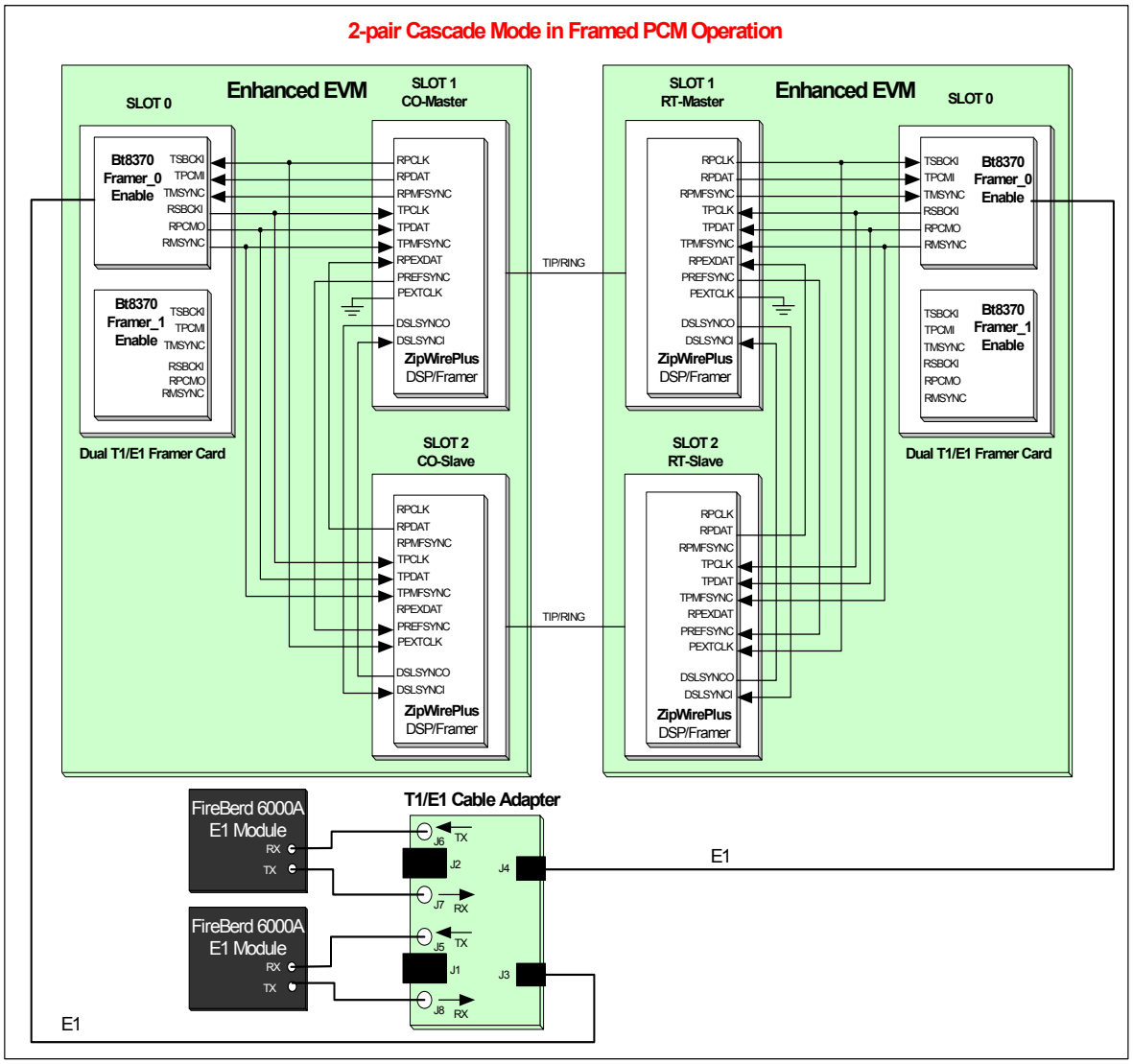
Configure the Fireberd #1 E1 Module front panel as follows:

- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kHz
- INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
- INTF SETUP: 2M/n64: MODE: FULL2M

3.3.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Framer #0 (slot 0). The Figure 3-30 explains the pin interconnections for this application.

Figure 3-30. Connections for Two-Pair Framed PCM Application in Cascade Mode



3.3.4 Enhanced EVM Configuration

3.3.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- ZipWirePlus firmware image

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.3.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.3.5 TestExec

3.3.5.1 Installation and Configuration

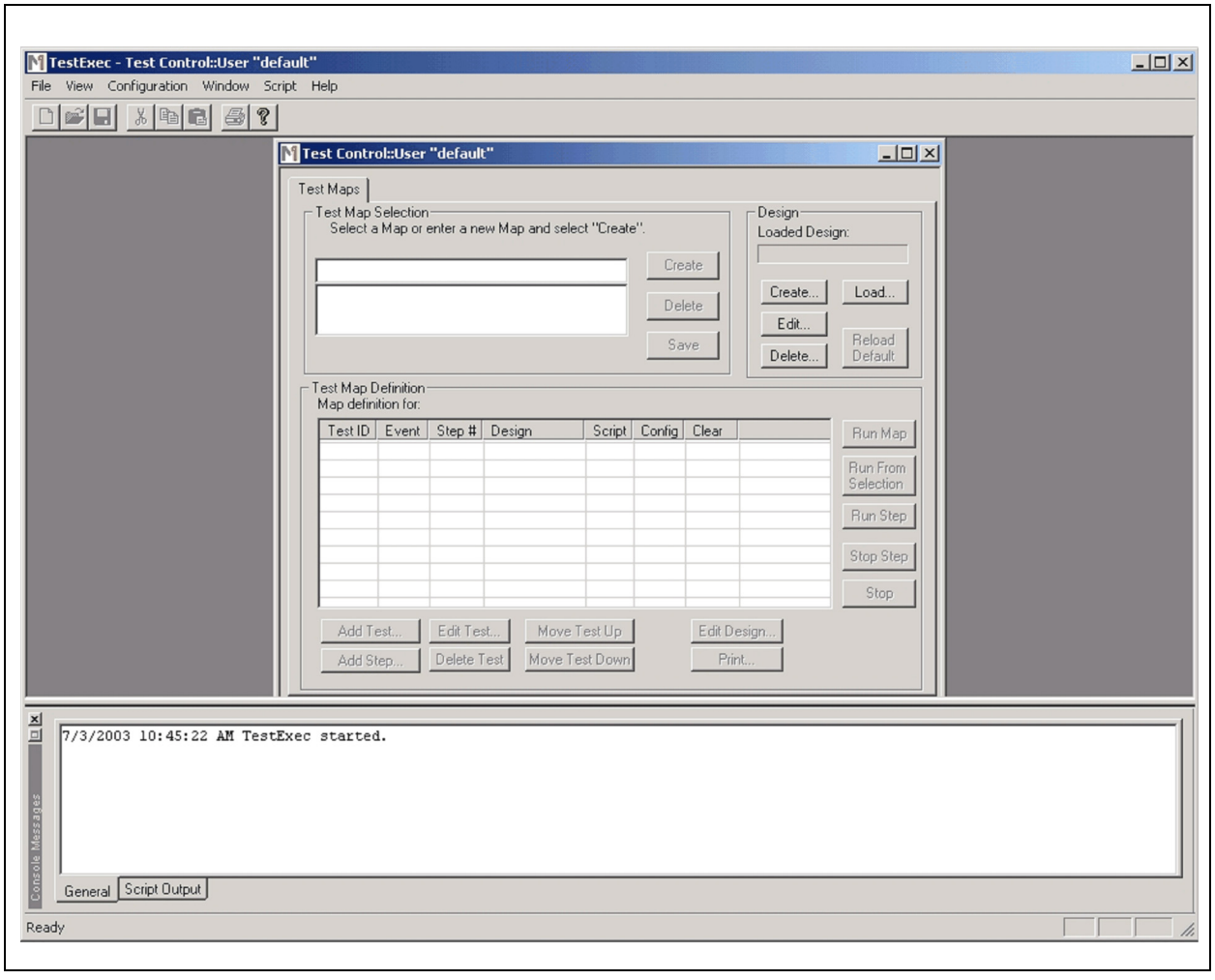
Please refer to Section 3.2.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software.

We will use the **EnhancedEvm** design file for the HTU-C Enhanced EVM.

3.3.5.2 Enhanced EVM Configuration

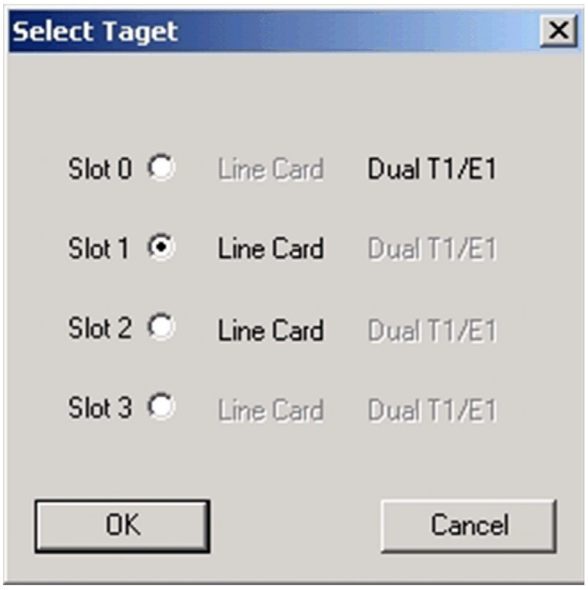
1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup and displays the following screen.

Figure 3-31. TestExec Main GUI



3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files
   a. **EnhancedEvm**
   b. **EnhancedEvm2**
   c. **LegacyEvm**
5. Select the **EnhancedEvm** design file. The TestExec will load the selected design file. Please note that for the HTU-C (CO) side EVM please select **EnhancedEvm** design file. For HTU-R (RT) side EVM please select the **EnhancedEvm2** design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. The Enhanced EVM has four slots - starting from zero. Select the slot to be configured by right clicking the mouse. The following menu appears.

Figure 3-32. Selecting the Slot



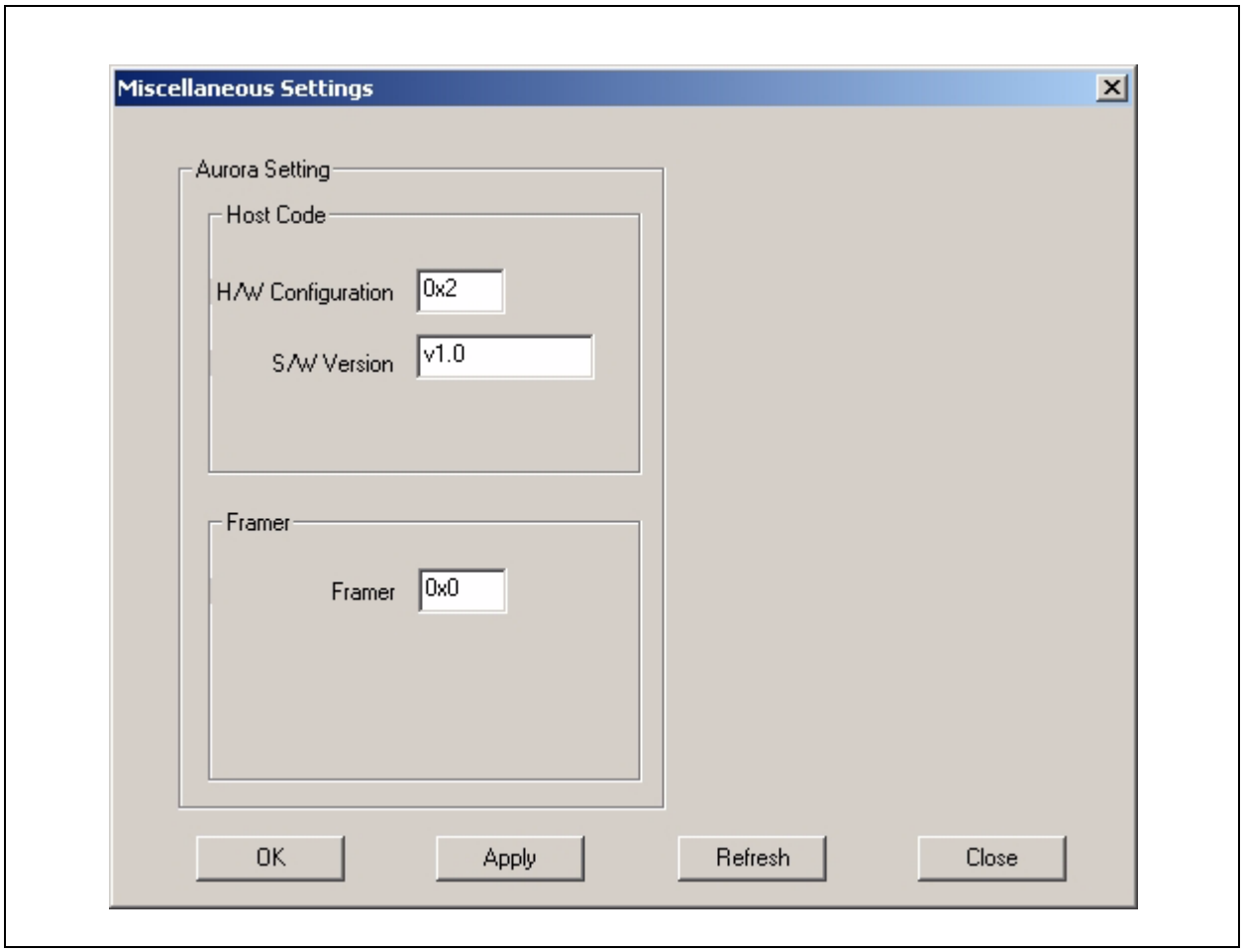
9. Select **Slot 1**.

3.3.5.2.1 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0x2.

4. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-33. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

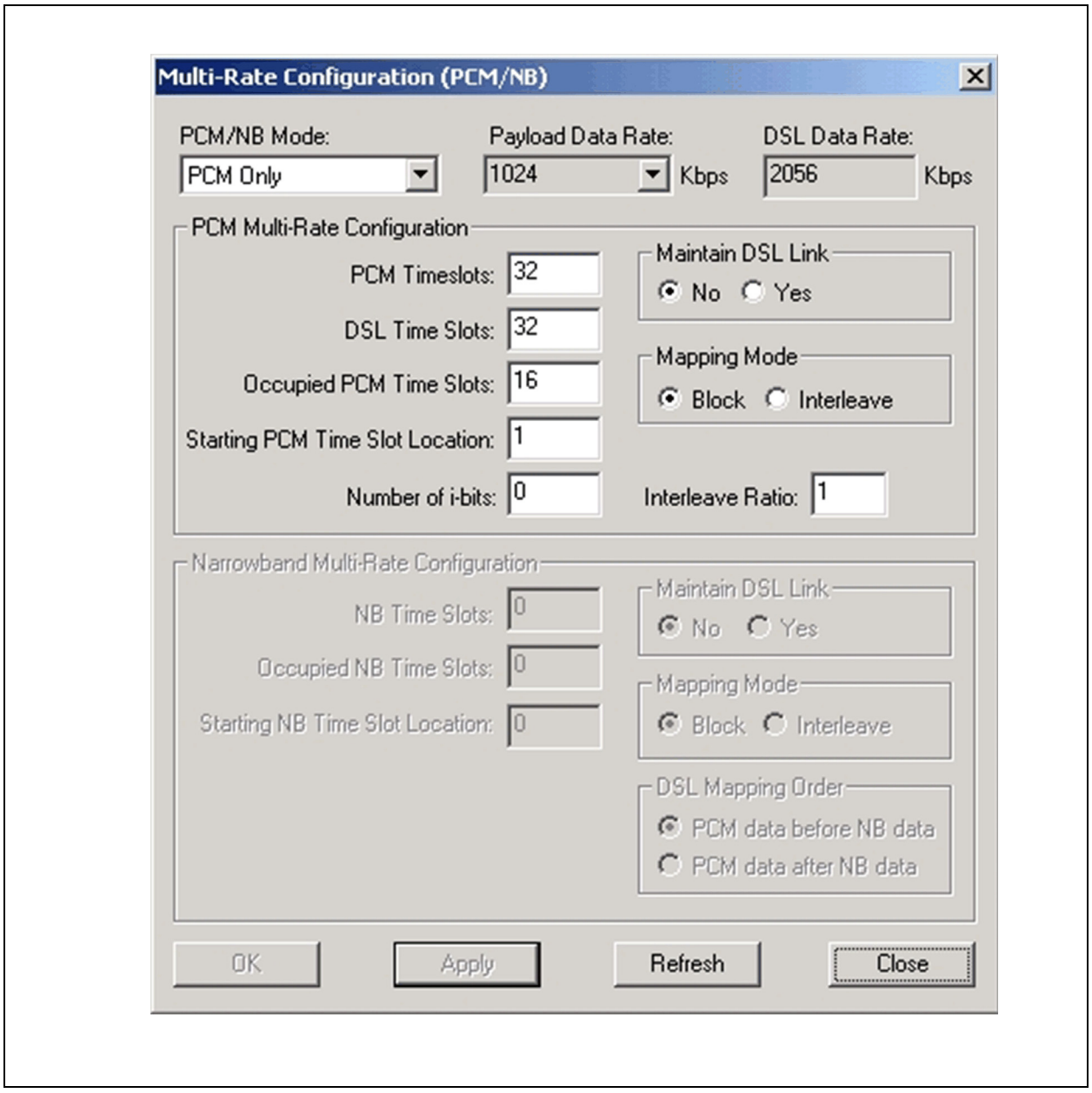


3.3.5.2.2 Slot 1 (HTU-C Master)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

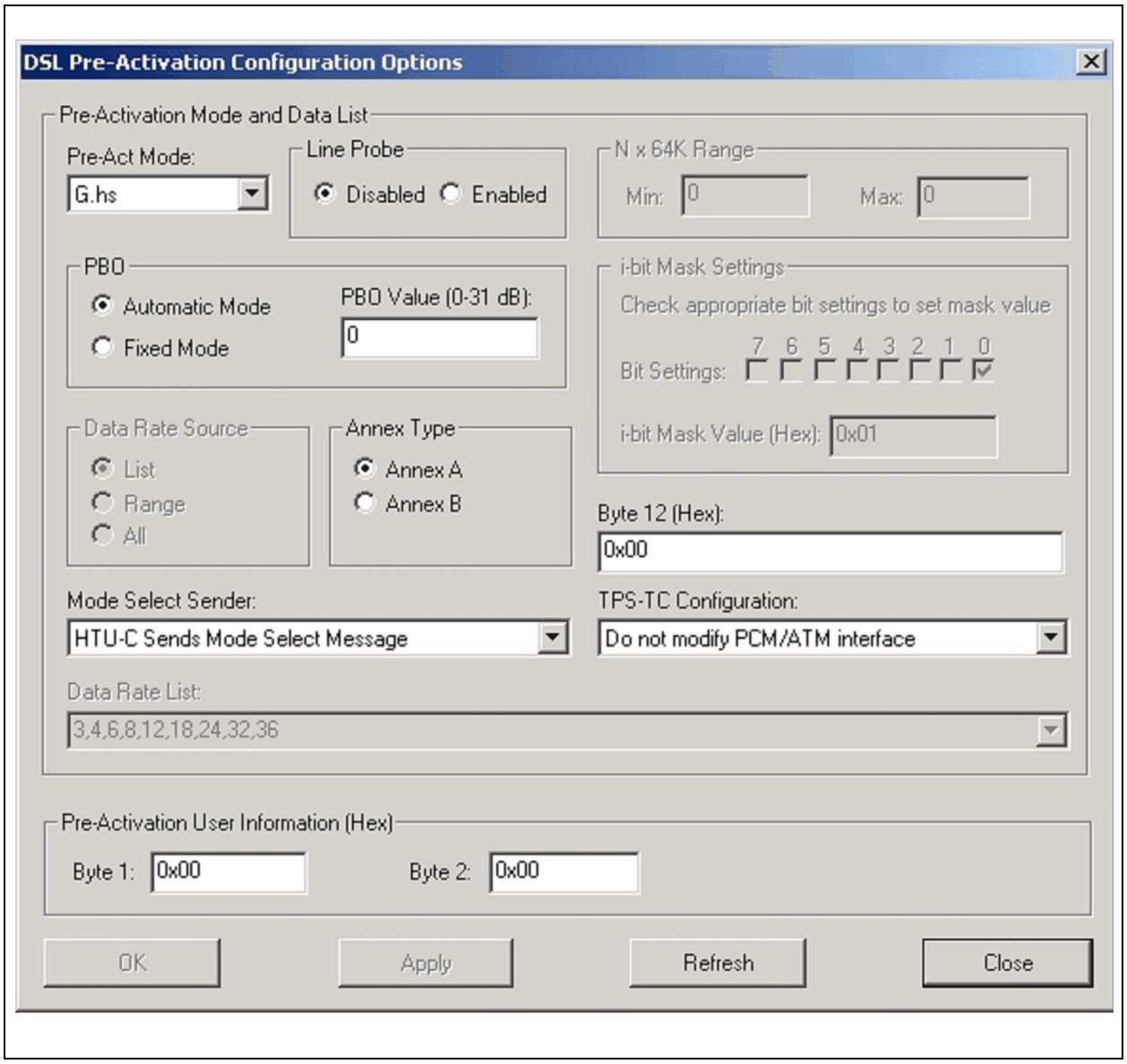
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-34. TestExec Multi-Rate Configuration for Master



5. Click the **Apply** button. The **Payload Data Rate** will change to 1024 Kbps and the **DSL Data Rate** will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-35. TestExec Preactivation Configuration for Master

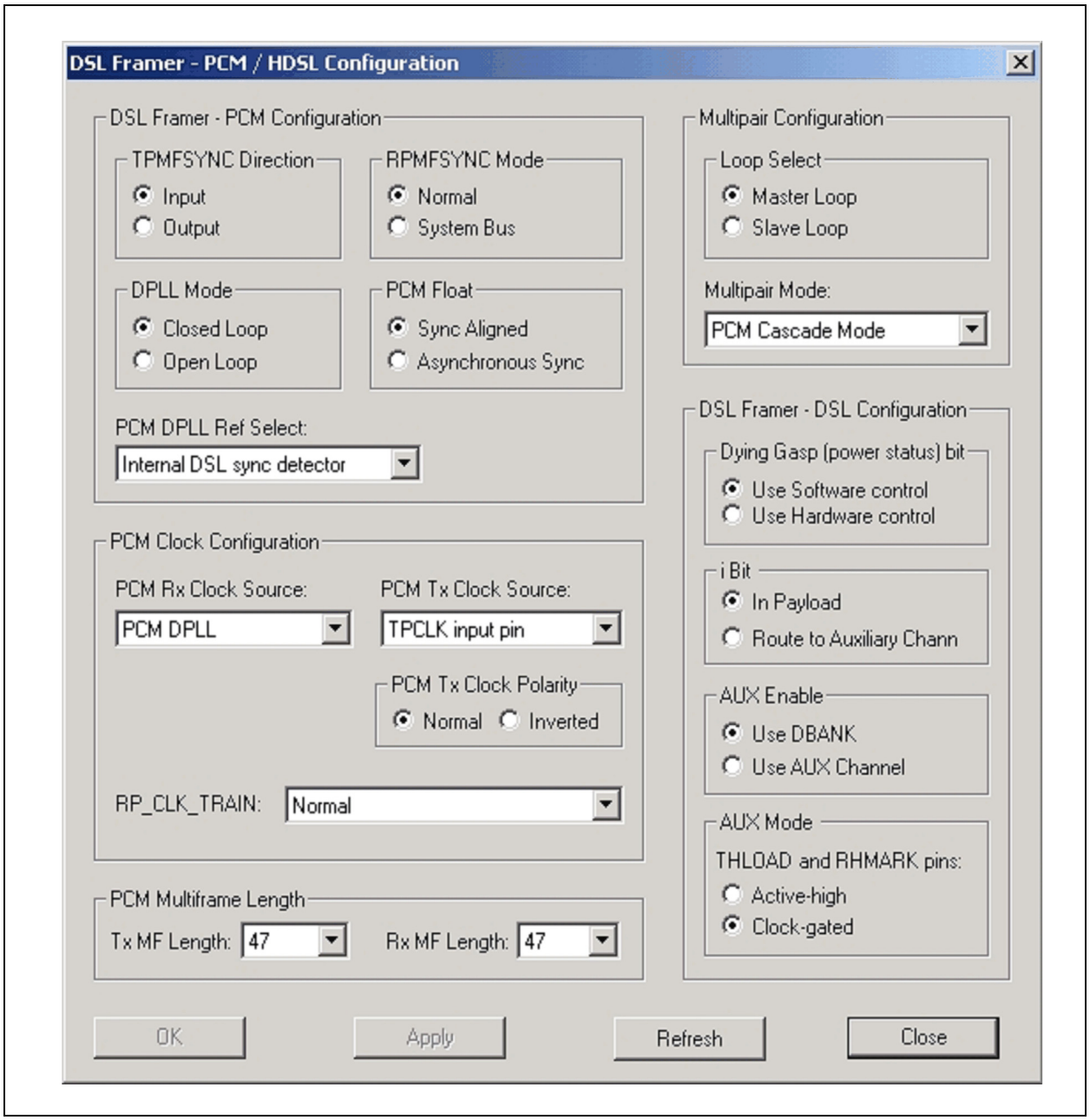


7. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration

  - PCM Rx Clock Source - **PCM DPLL**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-36. TextExec PCM/HDSL Configuration for Master



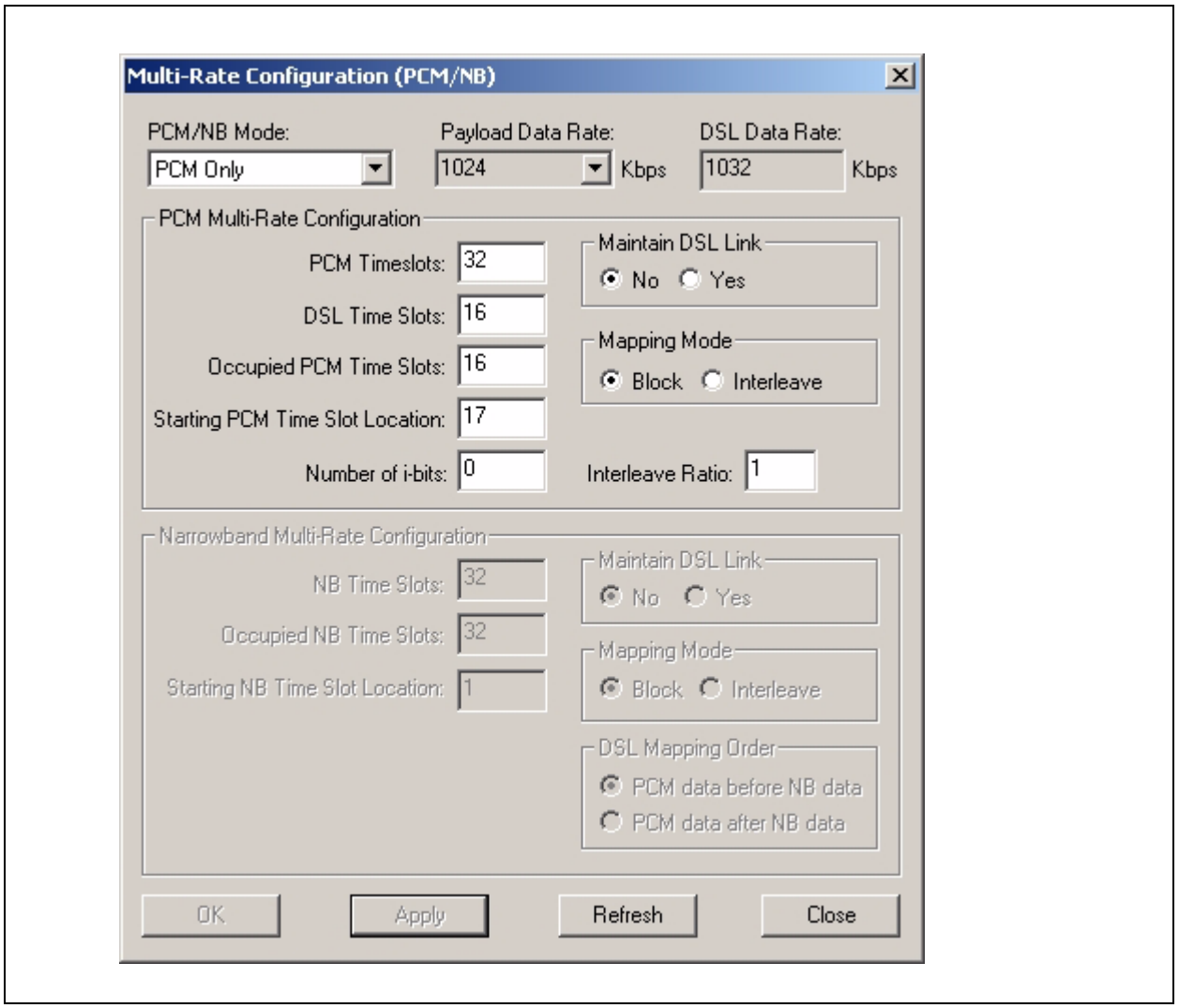
11. Click on **Apply** button and then click on the **Close** button.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
13. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.3.5.2.3 Slot 2 (HTU-C Slave)

1. Click on the **System Configuration** tab.

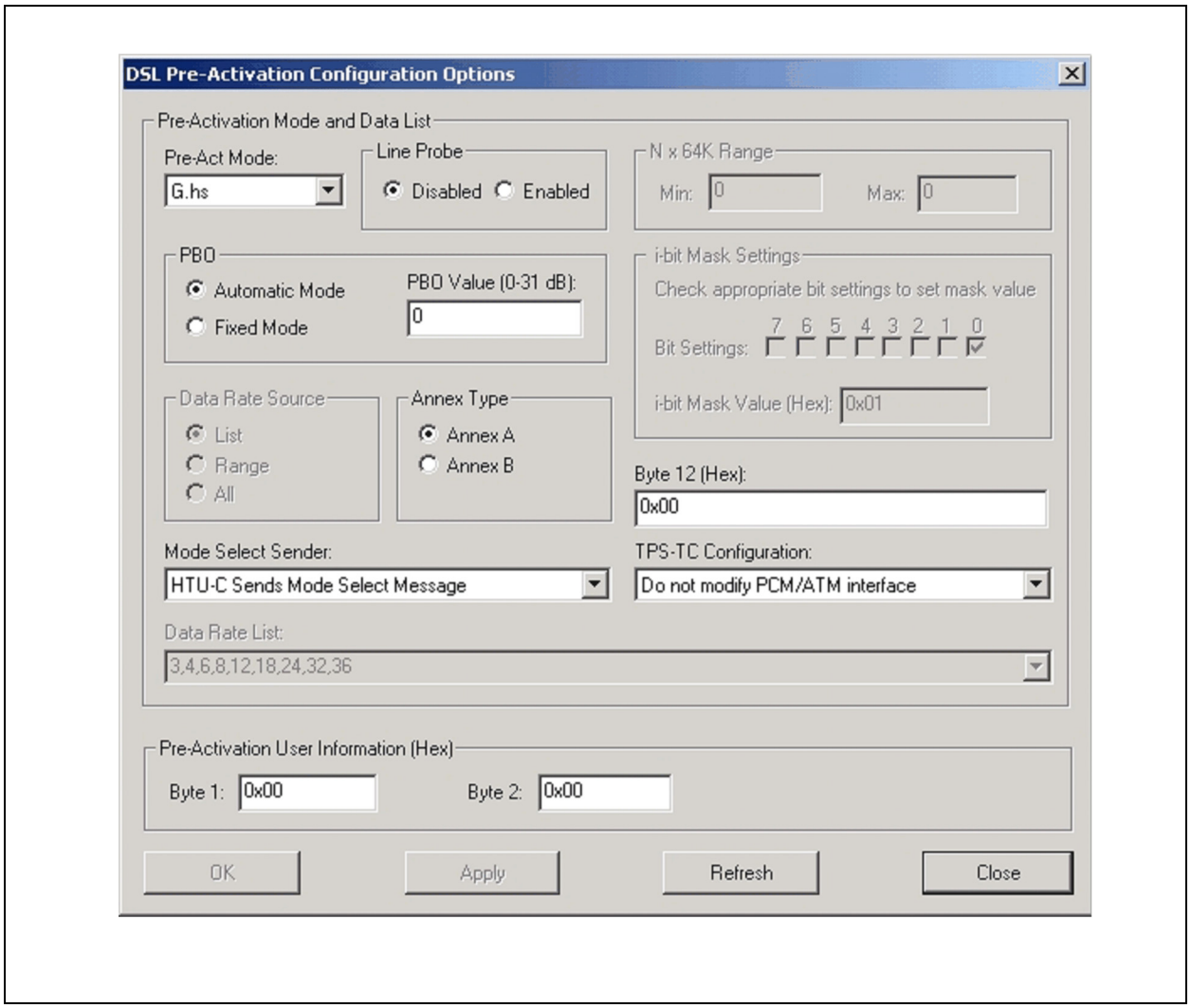
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:
   - PCM/NB Mode - **PCM Only**
   - PCM Timeslots - **32**
   - DSL Time Slots - **32**
   - Occupied Time Slots - **16**
   - Starting PCM Time Slot Location - **17**
   - Number of i-bits - **0**

Figure 3-37. TestExec Multi Rate Configuration for Slave



5. Click the **Apply** button. The Payload Data Rate will change to 1024 Kbps and the DSL Data Rate will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-38. TestExec Preactivation Configuration for Slave

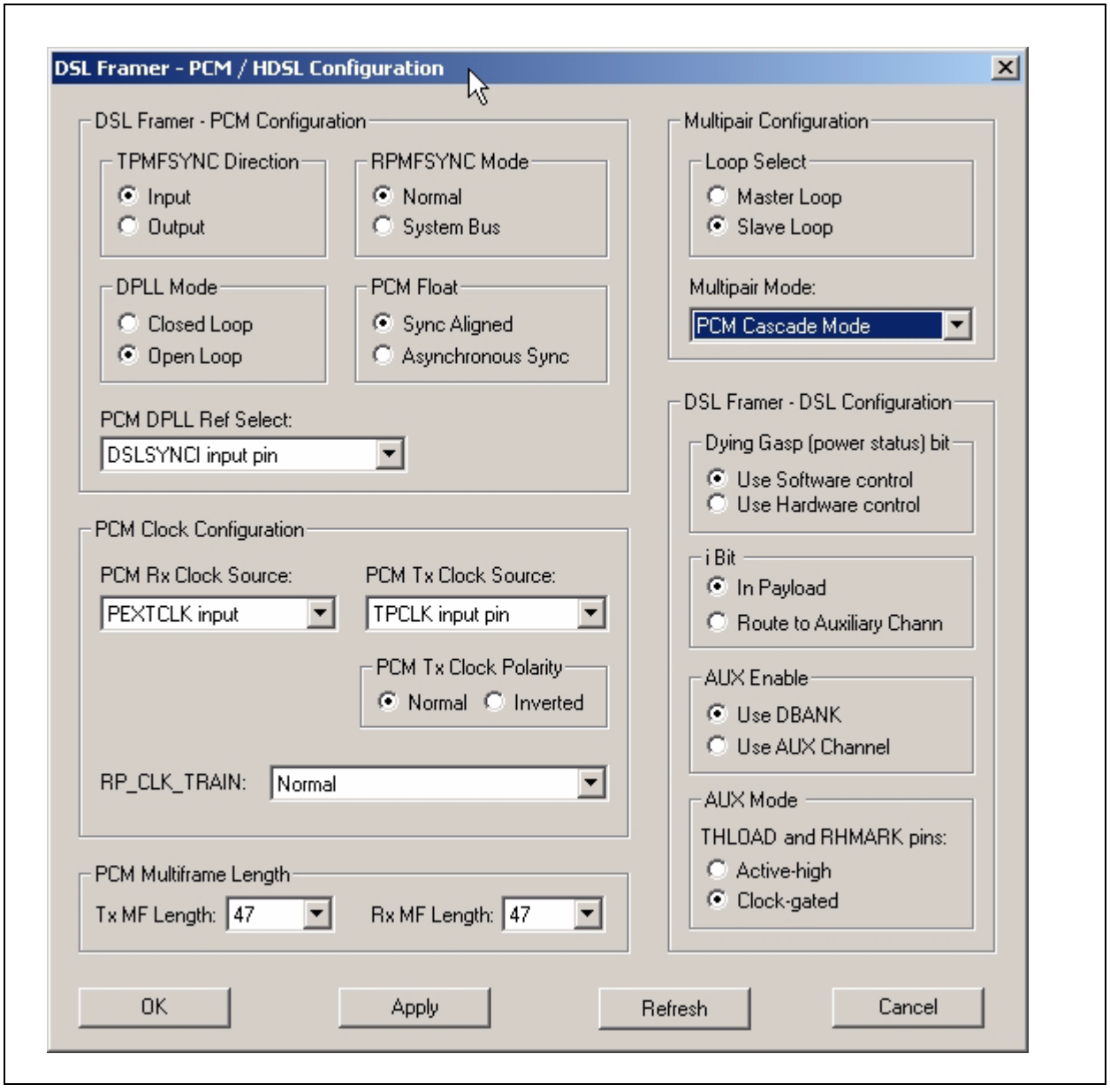


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **DSLSYNCI input pin**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PEXTCLK input**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**

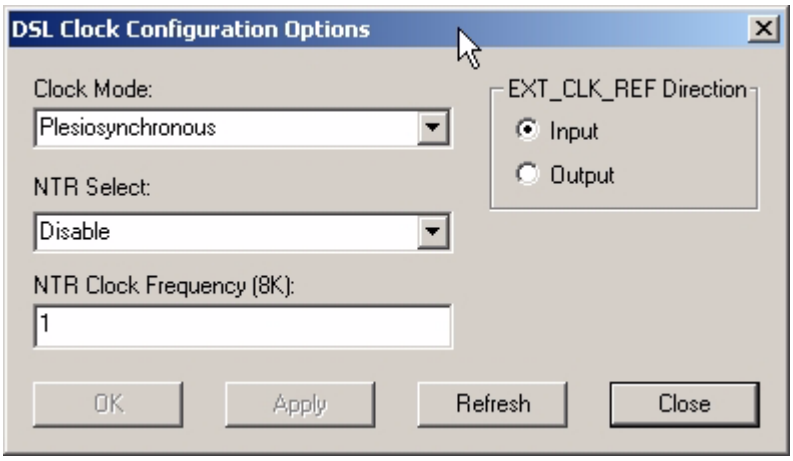
- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Slave Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-39. TextExec PCM/HDSL Configuration for Slave



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-40. TextExec DSL Clock Configuration

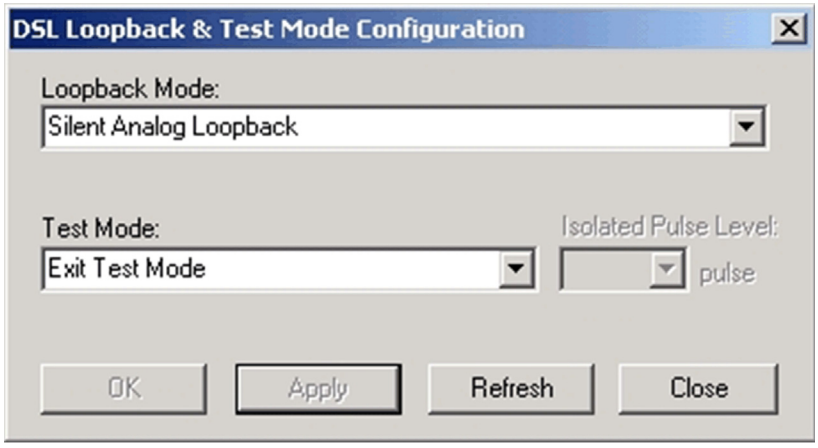


14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.3.5.2.4 Loopback

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Loopback/Test** button.
3. Set the **Loopback Mode** to **Silent Analog Loopback**.

Figure 3-41. Setting the ZipwirePlus Device into Loopback

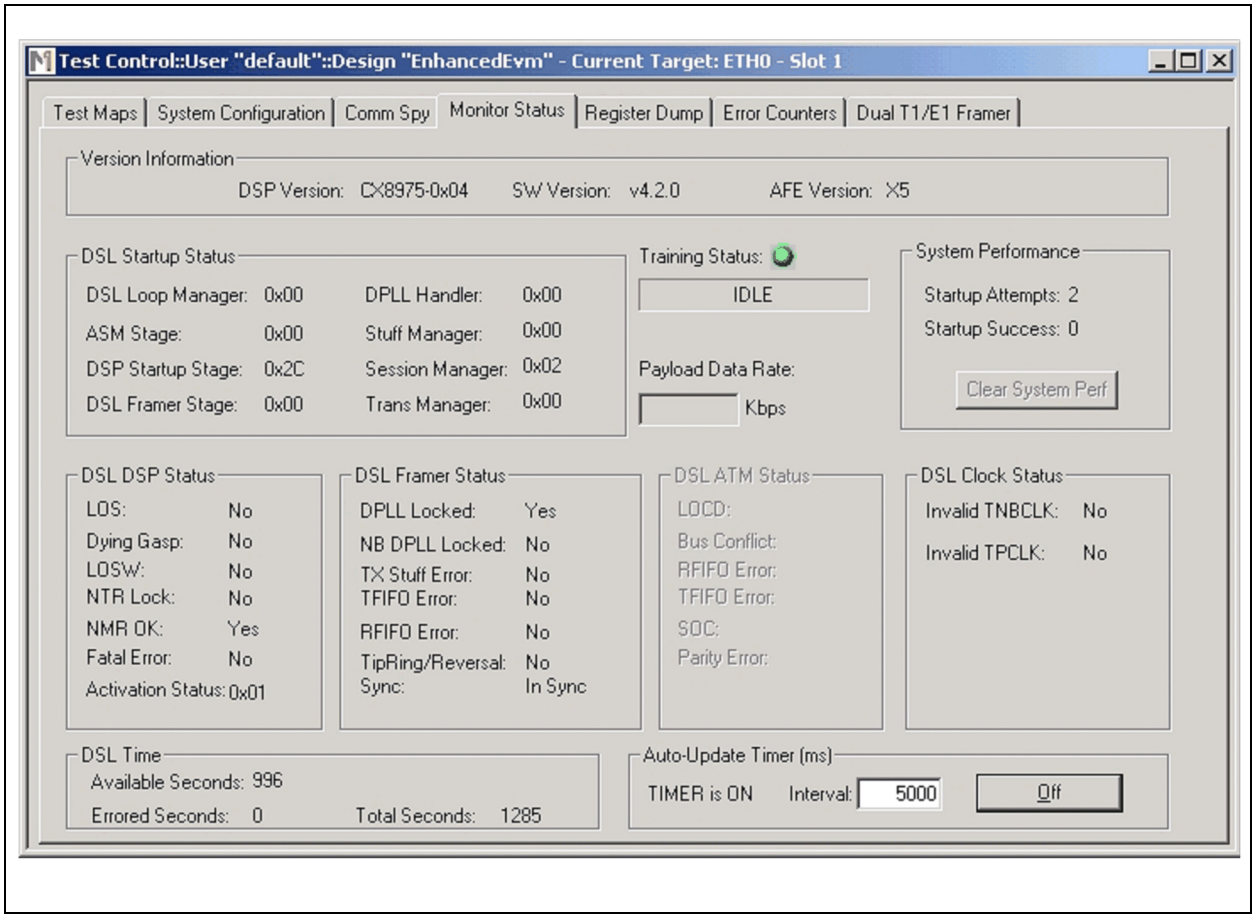


4. Click on the **Apply** button and then click on the Close button.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Click on the **Loopback/Test** button.
7. Set the **Loopback Mode** to **Silent Analog Loopback**. Click on the **Apply** button and then click on the **Close** button.

3.3.5.2.5 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the Set button in the **Auto Update Timer** box.
4. Verify that the Training Status is **GREEN** and showing **IDLE** State.

Figure 3-42. Monitoring the ZipWirePlus Device in Loopback



5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2.**
6. Repeat Steps 2 - 4.
7. Verify the Fireberd is in SYNC with no Bit Errors.

3.3.6 End to End Testing Using Two Enhanced EVMs

For end to end testing, one additional Enhanced EVM is needed.

3.3.6.1 Enhanced EVM Setup for HTU-R Side

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-R) and Slot 2(Slave HTU-R) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-R and the ZipWirePlus LIC in Slot 2 as the Slave HTU-R. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -

   Fireberd #2 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-R Master and HTU-R Slave cards.
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
8. Set up for Zero Loop Length

   a) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Master Slot 1) to J7 of the ZipWirePlus LIC(HTU-R Master Slot 1) of this Enhanced EVM.

   b) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Slave Slot 2) to J7 of the ZipWirePlus LIC(HTU-R Slave Slot 2) of this Enhanced EVM.

3.3.6.2 Fireberd #2 Setup

Configure the Fireberd as defined in Section 3.3.2

3.3.6.3 TestExec

3.3.6.3.1 Installation and Configuration

Please refer to Section 3.2.5.1 for detailed procedure for installing the configuring the TestExec(UIP) software.

Assuming the same PC is being used to control both HTU-C & HTU-R, we will use the **EnhancedEvm2** design file for the HTU-R Enhanced EVM.

3.3.6.3.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

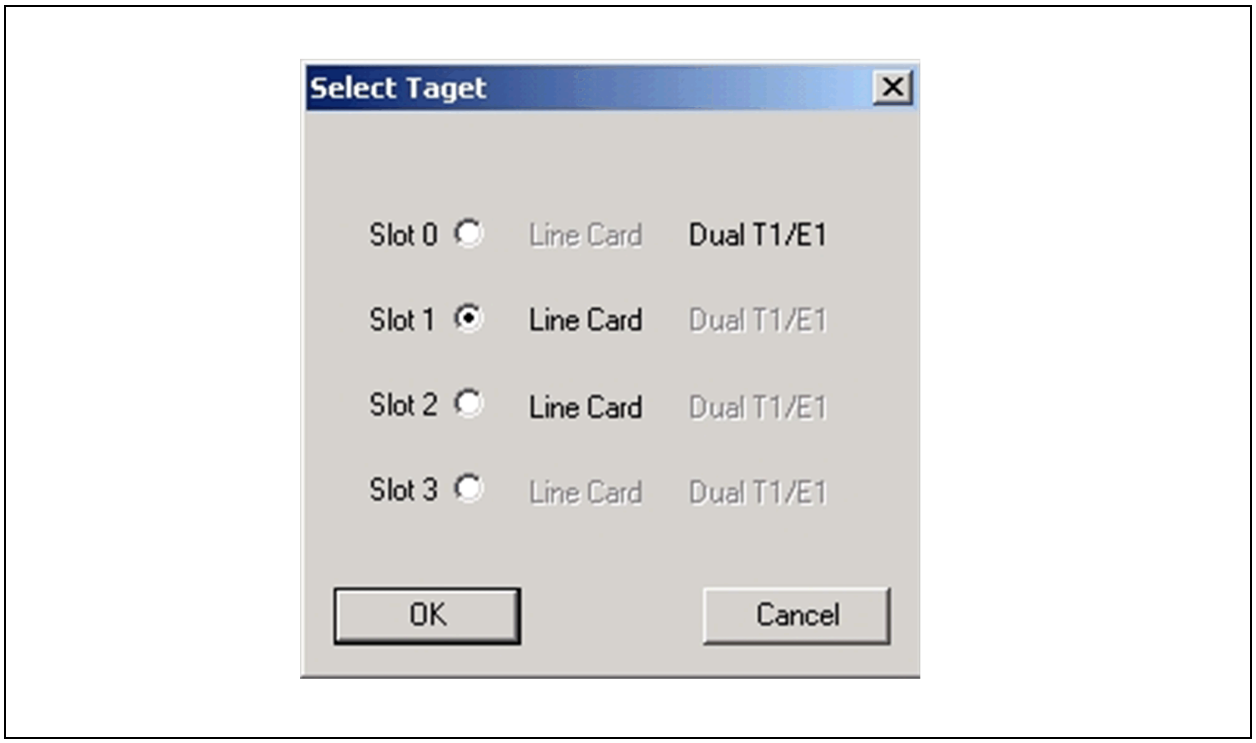
a.**EnhancedEvm**

b.**EnhancedEvm2**

c.**LegacyEvm**

4. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. The Enhanced EVM has four slots - starting from zero. Select the slot to be configured by right clicking the mouse. The following menu appears.

Figure 3-43. Selecting the Slot



8. Select **Slot 1**.

3.3.6.3.3 Slot 1 (HTU-R Master)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Master card. Please refer to Section 3.3.5.2.2.

3.3.6.3.4 Slot 2 (HTU-R Slave)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Slave card. Please refer to Section 3.3.5.2.3.

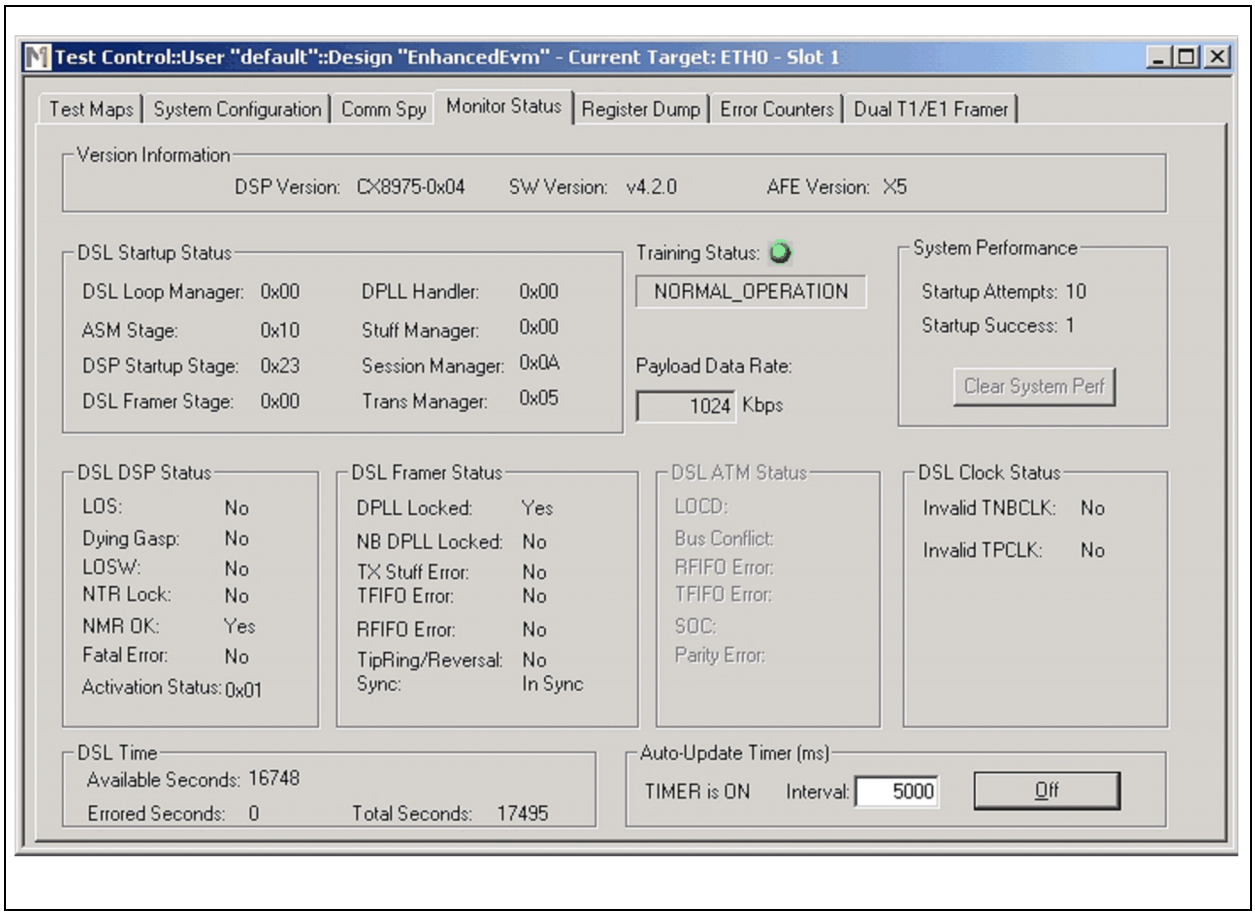
3.3.6.3.5 Loop Activation

1. Go to the TestExec GUI for HTU-C EVM.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Now take the HTU-C Master out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
4. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Master ZipWirePlus device and it will start training.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Now take the HTU-C Slave out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
7. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Slave ZipWirePlus device and it will start training.
8. Go to the TestExec GUI for HTU-R EVM.
9. Change to slot 1 by right clicking the mouse button and selecting Slot 1.
10. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Master ZipWirePlus device and it will start training.
11. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Slave ZipWirePlus device and it will start training.

3.3.6.3.6 Monitor the Link

1. Go the HTU-C TestExec GUI.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Click on the **Monitor Status** tab.
4. Click the **Set** button in the **Auto Update Timer** box.
5. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State.

Figure 3-44. Monitoring the DSL Link



6. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
7. Repeat Steps 2 - 4.
8. Verify the Fireberds are in SYNC with no Bit Errors.

3.3.6.4 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-29. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.4 Enhanced EVM Setup for Single Repeater/ Regenerator Mode

This section describes how to use the ZipWirePlus Enhanced EVM as an ETSI 101 524 compliant regenerator and an ITU 991.2 compliant regenerator.

3.4.1 Repeater Overview

In order to achieve data transmission over greater distances than are achievable over a single SHDSL segment, one or more signal regenerators (SRUs or REGs) may be employed.

3.4.1.1 ITU G.991.2 Reference Diagram

The figure below has been extracted from the G.991.2 specification. It is a reference diagram of a SHDSL span containing two regenerators. Up to eight (8)

regenerators per span are supported within the EOC addressing scheme, and no further limitation is intended herein.

Each SRU shall consist of two parts: an SRU-R for interfacing with the

STU-C (or a separate SRU-C), and an SRU-C for interfacing with the STU-R (or a separate SRU-R). An internal connection between the SRU-R and SRU-C shall provide the communication between the two parts during start-up and normal operation.

An SHDSL span containing X regenerators shall contain X + 1 separated SHDSL segments, designated TR_1 (STU-C to SRU_1-R), TR_2 (SRU_X-C to STU-R), and RRn (SRU_n-C to SRU_{n+1}-R, where $\mathbf{1} \leq \mathbf{n} \leq \mathbf{X - 1}$).

Figure 3-45. Block Diagram of a SHDSL Span with Two Signal Regenerators

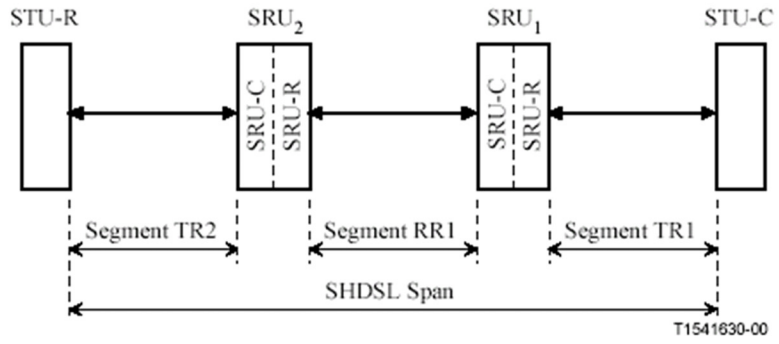


Figure D.1/G.991.2 – Block diagram of a SHDSL span with two signal regenerators

3.4.1.2 ETSI 101 524 Reference Diagram

The figure below has been extracted from the ETSI 101 524 Specification. It is a reference diagram of a SDSL span containing two regenerators. Up to eight (8) regenerators per span are supported within the EOC addressing scheme, and no further limitation is intended herein. Each REG shall consist of two parts: an REG-R for interfacing with the LTU (or a separate REG-C), and an REG-C for interfacing with the NTU (or a separate REG-R). An internal connection between the REG-R and REG-C shall provide the communication between the two parts during start-up and normal operation. An SDSL span containing X regenerators shall contain X+1

separated SDSL segments, designated TR_1 (LTU to REG_1-R), TR_2 (REG_X-C to NTU), and RRn

(REG_n-C to REG_{n+1}-R, where $1 \leq n \leq X - 1$).

Figure 3-46. Block Diagram of a SDSL Span with Two Signal Regenerators

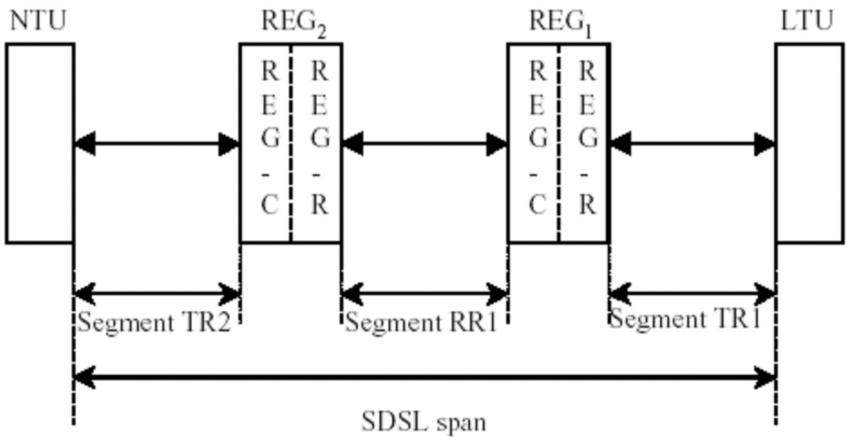


Figure C-1: Block Diagram of a SDSL Span with Two Signal Regenerators

3.4.2 ZipWirePlus Enhanced EVM Implementation

The Mindspeed implementation on the Enhanced EVM is a one regenerator span in fixed rate mode with the same DSL rates on both sides of the regenerator.

3.4.2.1 System Architecture

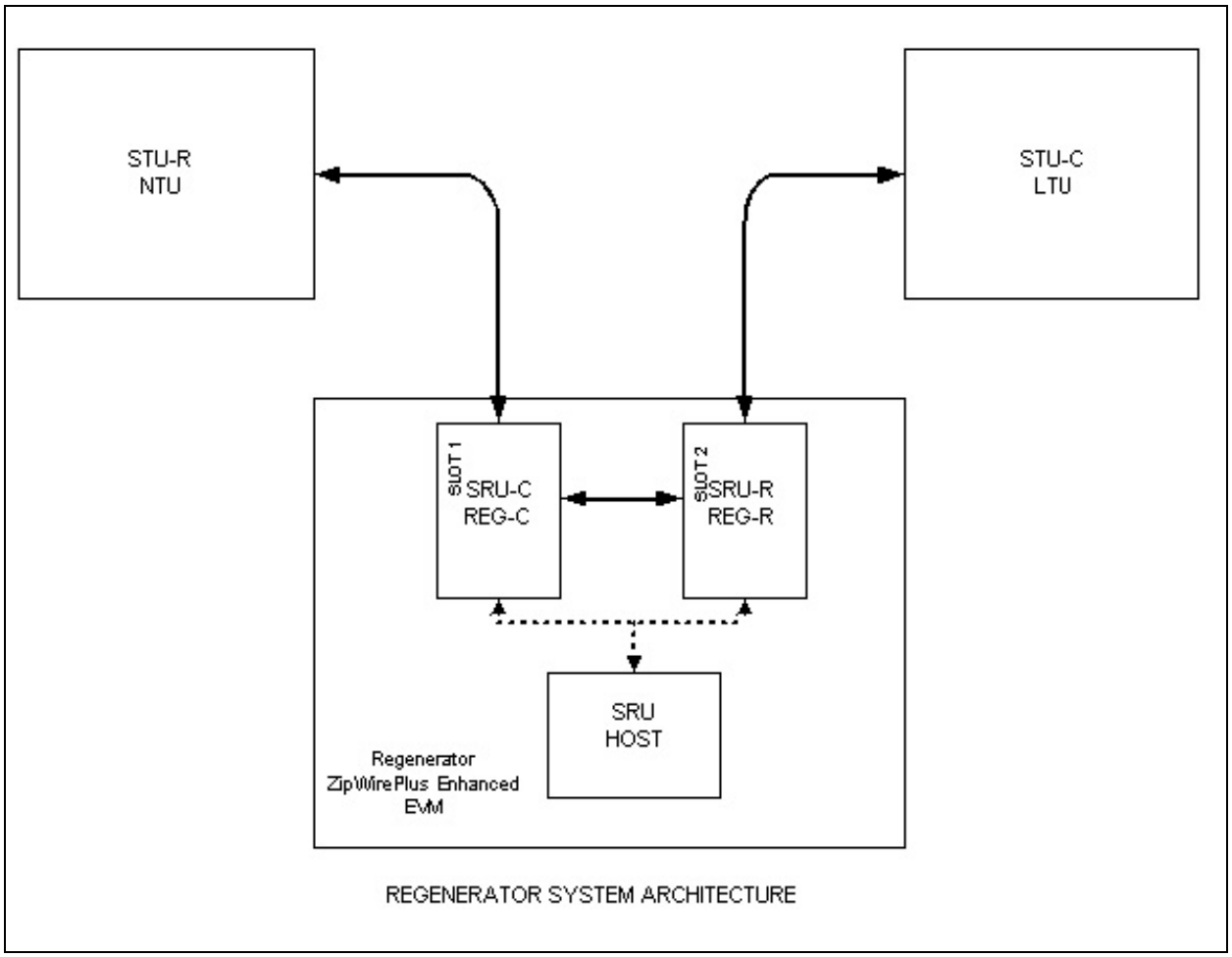
The regenerator consists of

- SRU-C / REG-C
- SRU-R / REG-R

In the Regenerator Enhanced EVM the ZipWirePlus LIC on slot 1 is the REG-C. The ZipWirePlus LIC on slot 2 is the REG-R.

The REG-C & REG-R are controlled by the Host Processor (MPC8260) located on the Elgin Microprocessor Board. The Host processor is called SRU Host.

Figure 3-47. Mindspeed Regenerator Enhanced EVM System Architecture



The SRU host controls the activation and deactivation of the links within the span. It also communicates information from REG-R to REG-C and viceversa.

3.4.2.2 Regenerator Host Software

3.4.2.2.1 Regenerator Host Software Overview

The Regenerator Host Software runs on the Host Microprocessor Board. It is responsible for the following

- Configuring the Enhanced EVM.
- Downloading the ZipWirePlus firmware image to the ZipWireDevices
- Creates a socket for the TestExec/UIP Software
- Regenerator State Machine
- Configuring and Managing the ZipWirePlus LICs for Regenerator Application.
- Implements the internal control communication channel between the REG-C and REG-R.

3.4.2.2.2 Regenerator Host Software Functionality

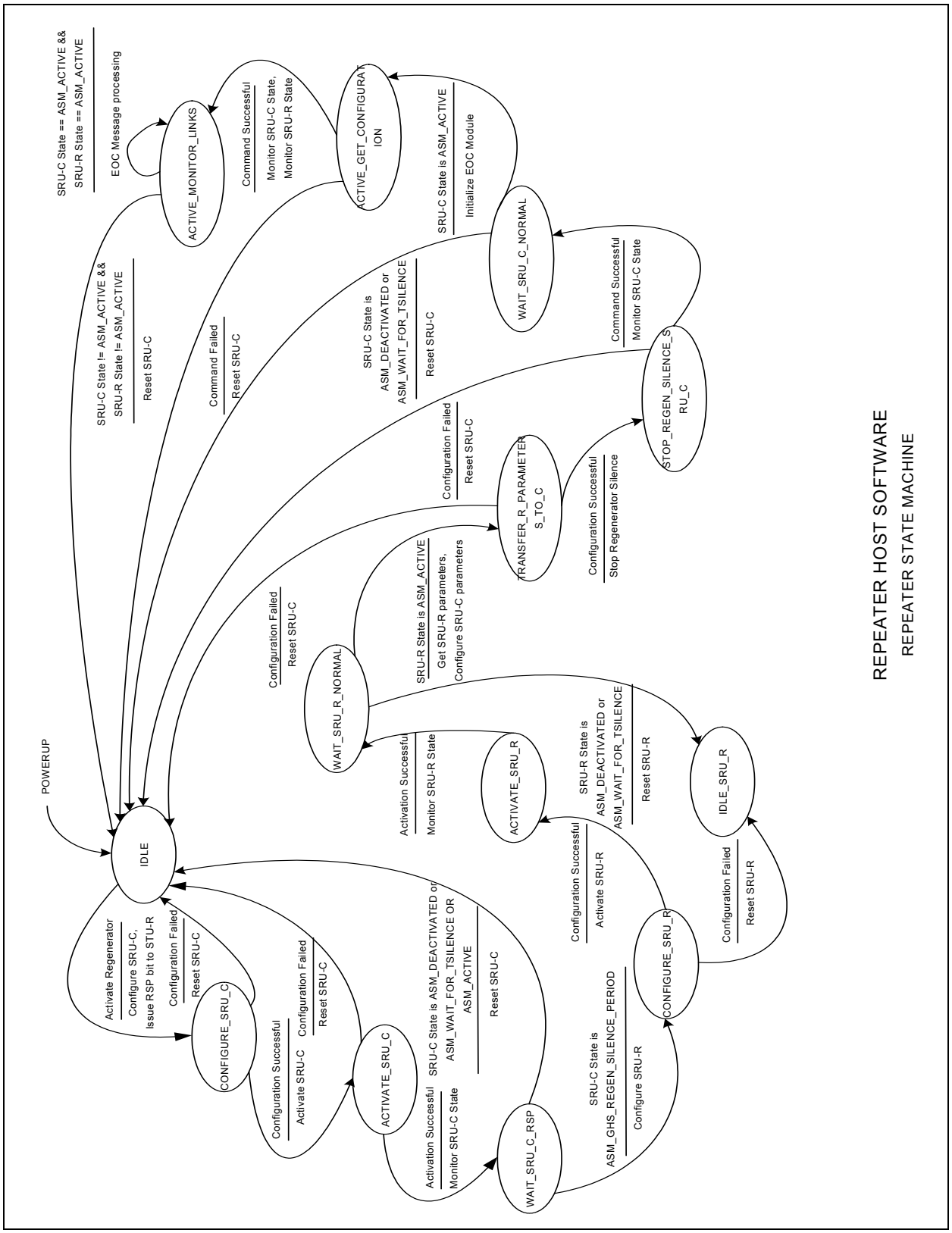
The Host Software upon power up configures the Regenerator Enhanced EVM and creates a socket for communication with the TestExec/UIP software.

Upon receiving command from the TestExec, the Host Software downloads the ZipWirePlus Firmware image to the ZipWirePlus LICs connected to Slot 1 and Slot 2 respectively. Choosing the Hardware configuration for Repeater (from the Testexec GUI) will start the Repeater State Machine.

Repeater State Machine

The State Machine will first bring up the link between the SRU-C (ZipWirePlus LIC inserted on Slot 1) and the HTU-R. It will configure the SRU-C and activate it. It monitors the ASM Stage inside the ZipWirePlus device (SRU-C) until it reaches ASM_GHS_REGEN_SILENCE_PERIOD stage("Silent Period").

Figure 3-48. Repeater State Machine



Then the State Machine will bring up the link between SRU-R (ZipWirePlus LIC inserted on Slot 2) and the HTU-C. It will configure and activate the SRU-R. It will monitor the ASM Stage inside the ZipWirePlus device(SRU-R) till it reaches ASM_ACTIVE_STATE. It polls the SRU-R for the Data Rate and Clock Mode information and transfers it to the SRU-C and takes the HTU-R out of "Silence Period" State.

Once both the links(SRU-C to HTU-R and SRU-R to HTU-C) are in NORMAL_OPERATION ("Active"), the State Machine will monitor the links and process EOC messages and handle any errors/exceptions that occur.

The Host Software supports the usage of Test Exec application at any time to monitor the status of the Repeater.

The Host Repeater Code uses the APIs defined in "M28945/M28946/M28947/ M28950 ZipWirePlus Programmers Reference Manual".

3.4.2.3 Regenerator Firmware

3.4.2.3.1 Regenerator Firmware Overview

The Regenerator firmware implements an ITU G.991.1/ETSI 101 524 compliant regenerator.

3.4.2.3.2 Regenerator Firmware Functionality

Prior to activation or configuration the SRU host issues the _DSL_START_REGEN_SILENCE API to the SRU-C. This API instructs the SRU-C to issue the Regenerator Silence Period bit during G.hs session to the HTU-R.

In the G.shdsl span the HTU-R starts the process off by generating R-TONES to the SRU-C. When activated by the SRU host the SRU-C generates C-TONES. When the HTU-R detects the SRU-C's C-TONES it begins the G.HS process by sending a CLR message. The SRU-C responds with a CL message. The HTU-R will indicate it can do all rates and sub-rates. The SRU-C will indicate it also can do all rates and sub-rates. The HTU-R then sends an MR message asking the SRU-C to select the mode. The SRU-C issues a mode select (MS) message with the Regenerator Silence Period (RSP) bit set. When the HTU-R sees the RSP bit set it goes into Regenerator Silence Period for up to 5 minutes. During the RSP time the HTU-R will stop sending R-TONES and the SRU-C will stop sending C-TONES. The HTU-R will start up again when it detects C-TONES again from the HTU-C. Both the SRU-C and HTU-R will go the ASM activation state in the Activation State Manager called REGEN_SILENCE_PERIOD that has a value of 0x1B.

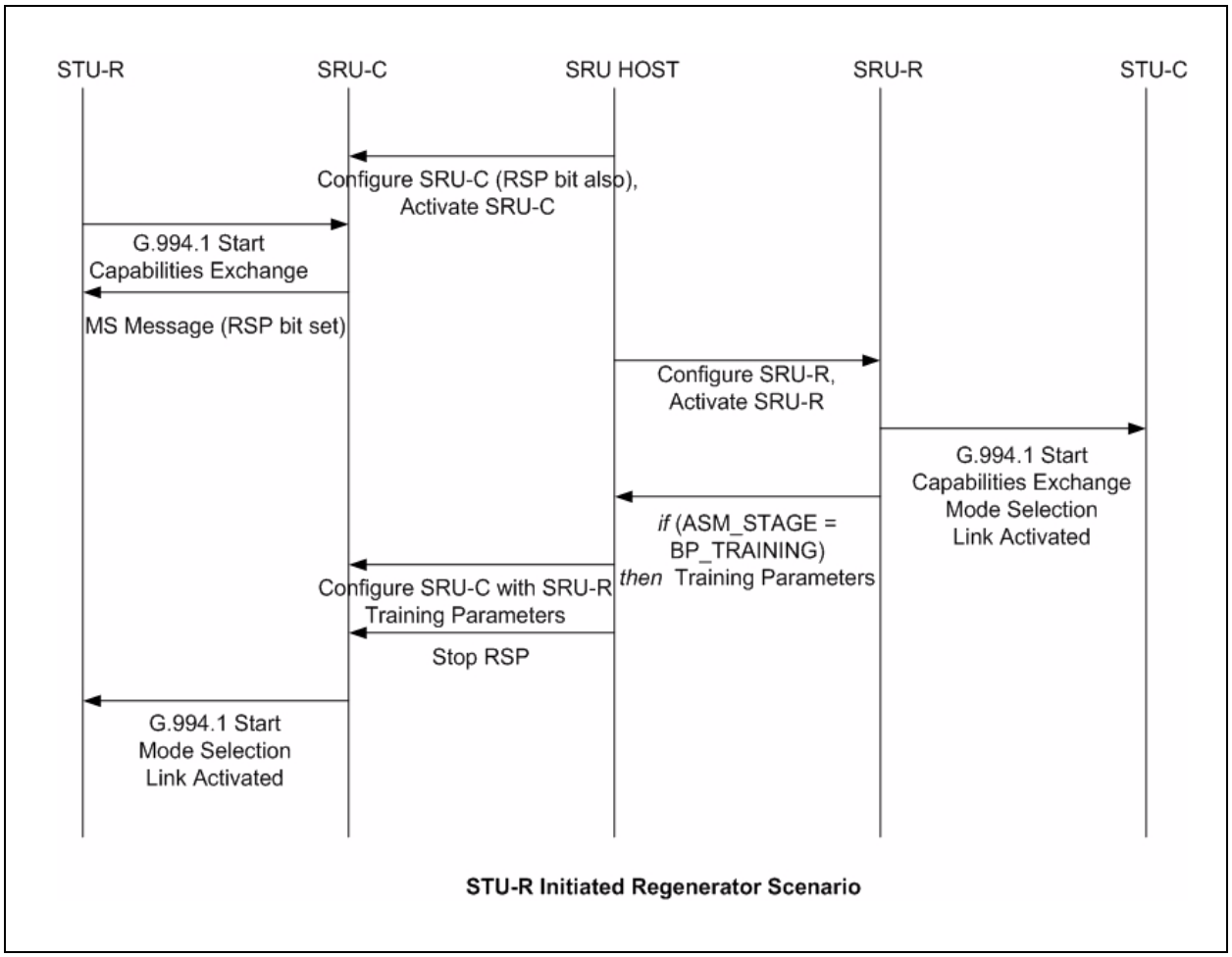
The new activation state was added so the SRU host could detect when the devices is in the RSP state. Also, this new activation stage informs the SRU host when it is time to activate the link between the SRU-R and HTU-C.

The SRU host issues the DSL_ACTIVATION API to the SRU-R device. The SRU-R and HTU-C will start a G.hs session. There will be the capabilities exchange (CLR/ CL) messages, mode select messages (MR/MS) then training. The SRU host monitors the activation stages of the SRU-R and waits until the link is in BP_TRAINING ASM activation state. When this state is achieved, the SRU host has enough parameter information to program the SRU-C device. The SRU host issues the _DSL_GHS_GET_FINAL_RATE API (0x81) to get the down stream rate, down

stream sub-rate, up stream rate and up stream sub-rate information from the HTU-C to SRU-R link. The data presented to the SRU host is in N rate and I bits format. The data extracted from the API is the total number of timeslots (N rate or Payload Rate) and total number of I-bits (I bit sub rate). This along with the clock configuration is used to configure the SRU-C device. The SRU host issues the _DSL_GHS_REGEN_OVERRIDE API to the SRU-C. This API overrides previous N and I rate configurations already present in the SRU-C. It also makes the data rate a match between the SRU-R to HTU-C link and the SRU-C to HTU-R link.

The SRU host then issues the _DSL_GHS_STOP_REGEN_SILENCE API to the SRU-C. The SRU-C begins generating C-TONES to the HTU-R. At the HTU-R, when C-TONES are detected, it begins transmitting R-TONES and initiates data transmission by sending a mode request (MR) message asking the SRU-C to issue the mode. The SRU-C responds by issuing a mode select (MS) message with the instruction to train up at the N and I rate programmed into it by the SRU host. From there the SRU-C to HTU-R link will train up to NORMAL_OPERATION. The entire span is in NORMAL_OPERATION (ACTIVE).

Figure 3-49. STU-R Initiated Regenerator Scenario



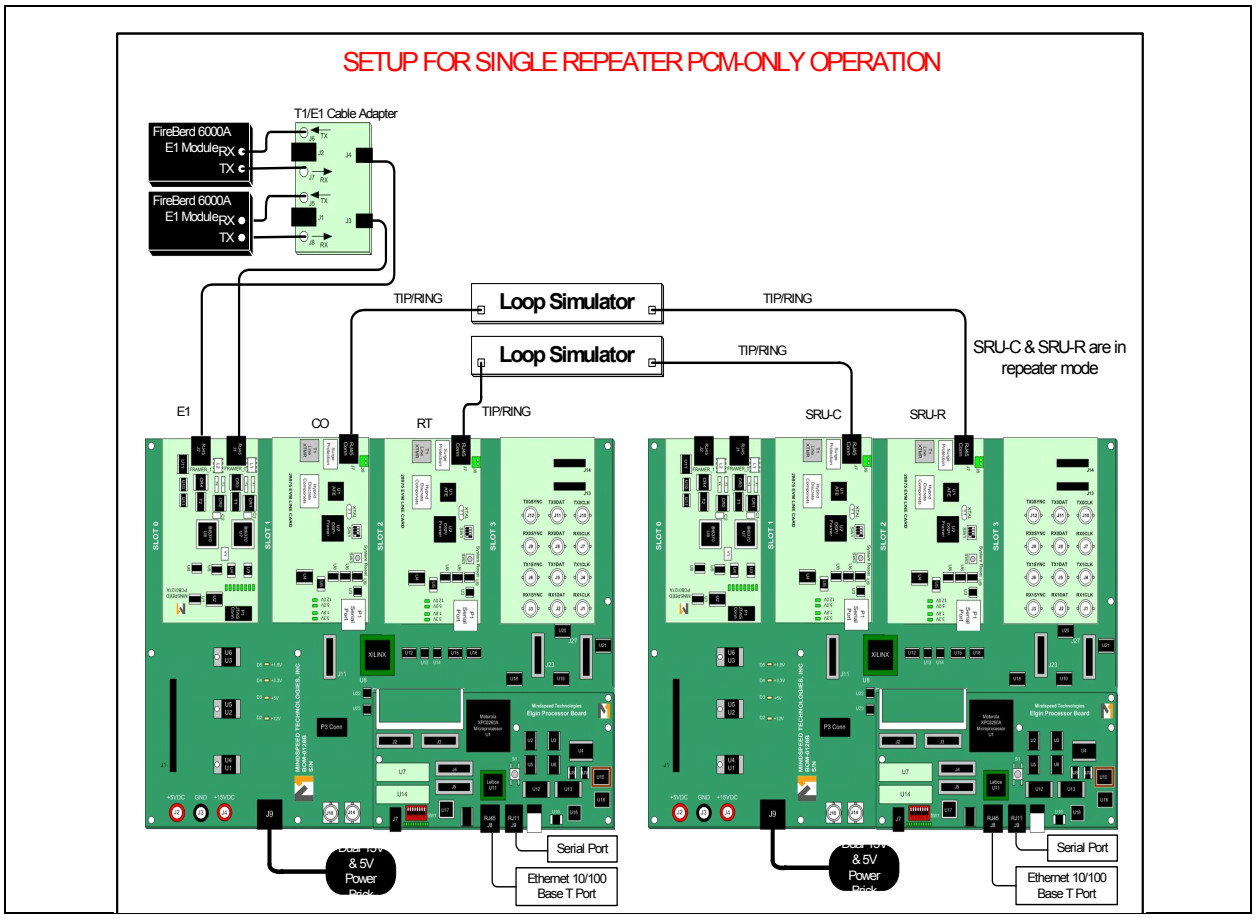
3.4.3 Enhanced EVM Setup

It is assumed that the customer has a Single-Pair PCM Only Application already up and running. And now the ZipWirePlus Regenerator Enhanced EVM shall be introduced between the HTU-C and HTU-R.

1. Place the Regenerator Enhanced EVM on a bench.
2. Ensure that the ZipWirePlus LICs are plugged into Slot 1(SRU-C or REG-C) and Slot 2(SRU-R or REG-R) respectively. Please note that the Dual T1/E1 framer card is not needed for this setup.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the SRU-C or REG-C and the ZipWirePlus LIC in Slot 2 as the SRU-R or REG-R.
6. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

Figure 3-50 shows more details of the setup.

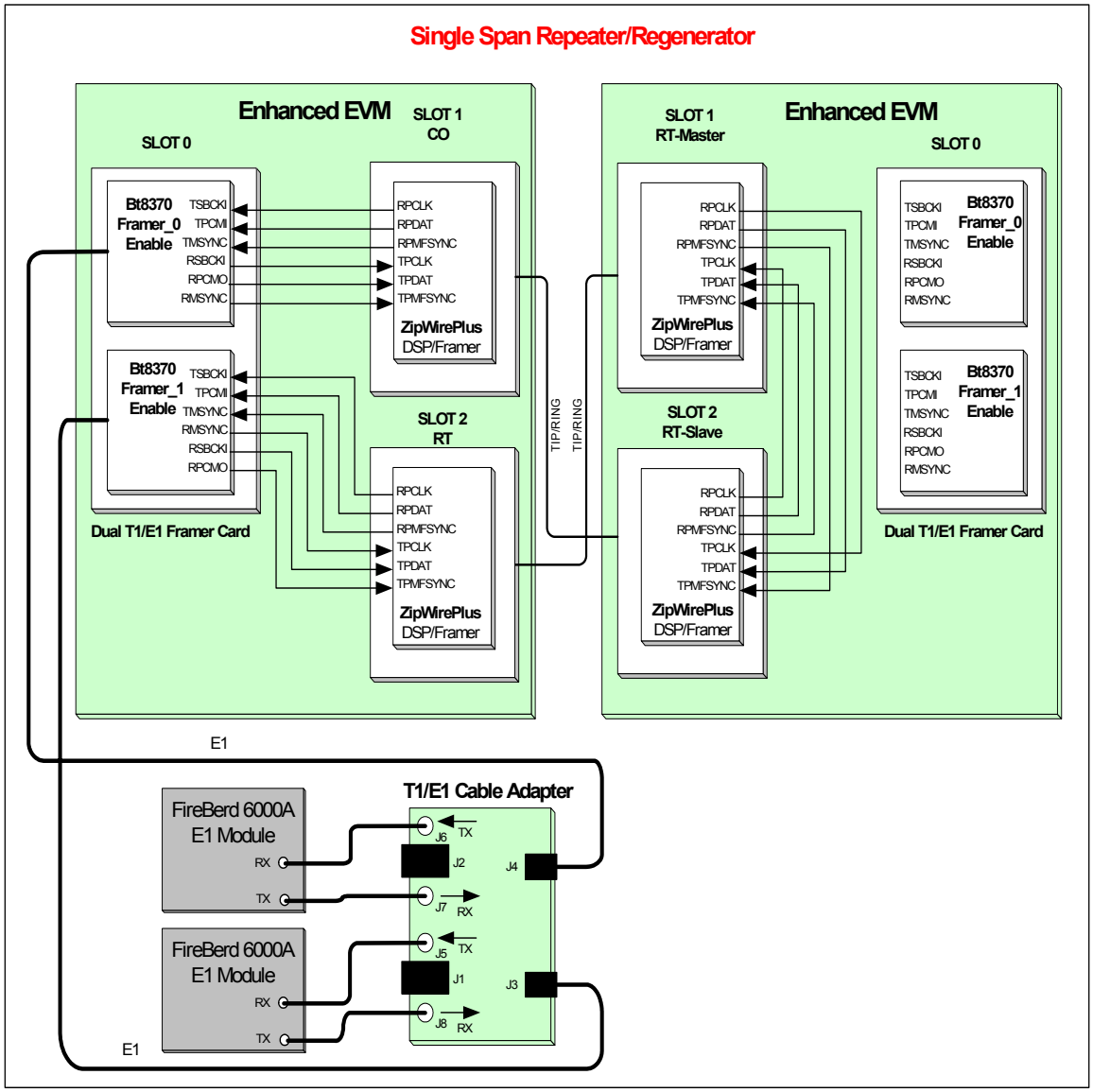
Figure 3-50. Setup for Single Repeater



3.4.4 FPGA Configuration

This configuration will connect the PCM bus of the ZipWirePlus device (slot 1) to the ZipWirePlus device (slot 2). Figure 3-51 explains the pin interconnections for this application.

Figure 3-51. Connections of Repeater PCM-only Operation Block Diagram



3.4.5 Enhanced EVM Configuration

3.4.5.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- ZipWirePlus firmware image

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the

Enhanced EVM when powering up the Enhanced EVM for the first time.

3.4.5.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.4.6 TestExec

3.4.6.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the **EnhancedEvm2** design file for the Repeater Enhanced EVM. It is assumed that the **EnhancedEvm** design file is used for the HTU-C & HTU-R Enhanced EVM.

3.4.6.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a. **EnhancedEvm**

   b. **EnhancedEvm2**

   c. **LegacyEvm**
4. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Select **Slot1** by right clicking the mouse.

3.4.6.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x3 for Annex A Repeater. For Annex B Repeater please enter 0x6.
3. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-52. Miscellaneous Settings Window- for Hardware configuration of Repeater Annex A

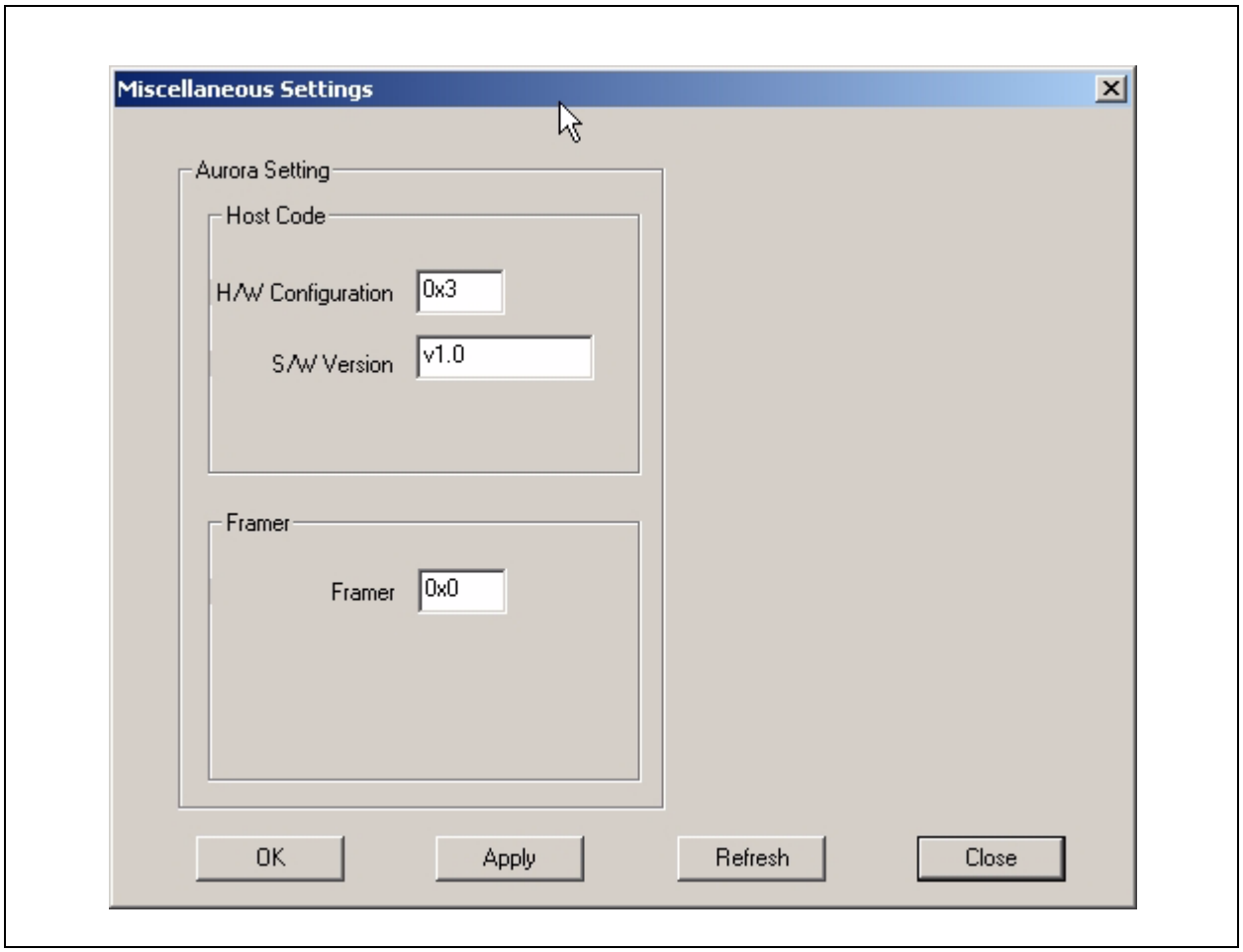
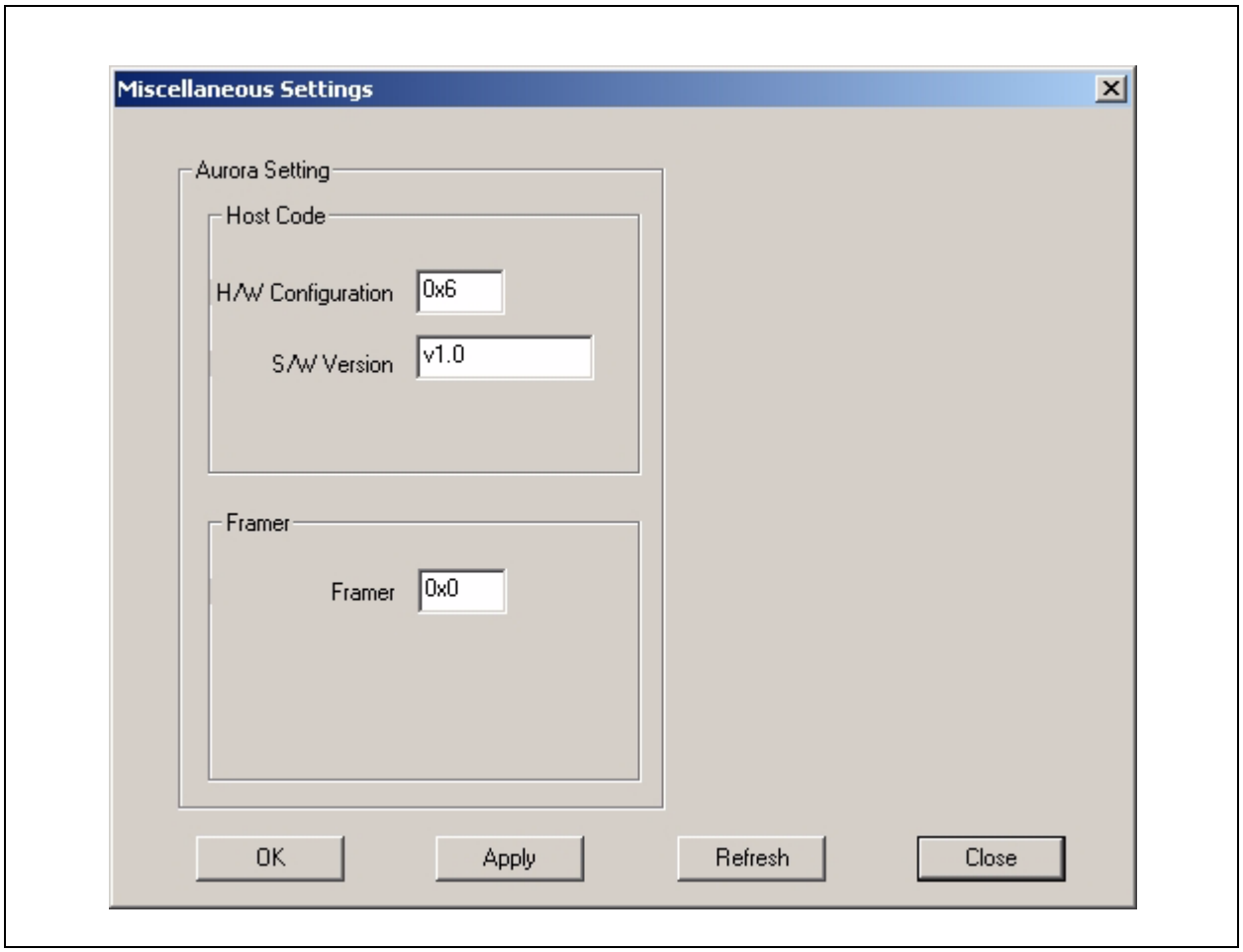


Figure 3-53. Miscellaneous Settings Window- for Hardware configuration of Repeater Annex B



4. This will start the Repeater State Machine and the following output shall appear on the serial port console.

Figure 3-54. Serial Console - Repeater State Machine on Startup

```
FPGA Configuration: Repeater Annex_A

Repeater State: IDLE

Repeater State: CONFIGURE_SRU_C

Repeater State: ACTIVATE_SRU_C

Repeater State: WAIT_SRU_C_RSP
ASM Stage: GHS_ACTIVATING


Repeater State: WAIT_SRU_C_RSP
ASM Stage: GHS_ACTIVATING
```

3.4.7 Activating the Repeater

For this example we have an Enhanced EVM set up, in the Single pair PCM Only Operation as defined in the Section 3.2. Verify that the DSL Link between the HTU-C and HTU-R is up.

1. Disconnect the RJ-45 cable which connects the HTU-C to HTU-R.
2. Verify from the DSL Link has gone down.
3. Monitor the serial output from the Regenerator EVM.
4. Connect the RJ-45 cable(provided) from HTU-R to J7 of the ZipWirePlus LIC (SRU-C, Slot 1 on Regenerator EVM).
5. Connect the RJ-45 cable(provided) from HTU-C to J7 of the ZipWirePlus LIC (SRU-C, Slot 1 on Regenerator EVM).
6. Wait till we get the following output from the serial console.

Figure 3-55. Serial Console -Repeater State Machine on Activation

```
Repeater State: TRANSFER_R_PARAMETERS_TO_C
Clock Mode: Length: 3, Data: 0x0 0x1 0x0
0x20 0x0 0x20 0x0 0x0

Repeater State: STOP_REGEN_SILENCE_SRU_C

Repeater State: WAIT_SRU_C_NORMAL
ASM Stage: BP_ACTIVATING

Repeater State: WAIT_SRU_C_NORMAL
ASM Stage: ACTIVE

Repeater State: ACTIVE_GET_CONFIGURATION

Repeater State: ACTIVE_MONITOR_LINKS
ASM Stage: ACTIVE
ASM Stage: ACTIVE
SRU_R_EOC_STATE: OFFLINE
SRU_C_EOC_STATE: OFFLINE

Repeater State: ACTIVE_MONITOR_LINKS
ASM Stage: ACTIVE
ASM Stage: ACTIVE
```

7. Verify that the DSL Link is active and the fireberds are in sync again.

3.5 Enhanced EVM Setup for Single-pair Framed PCM and Unframed Narrowband Operation

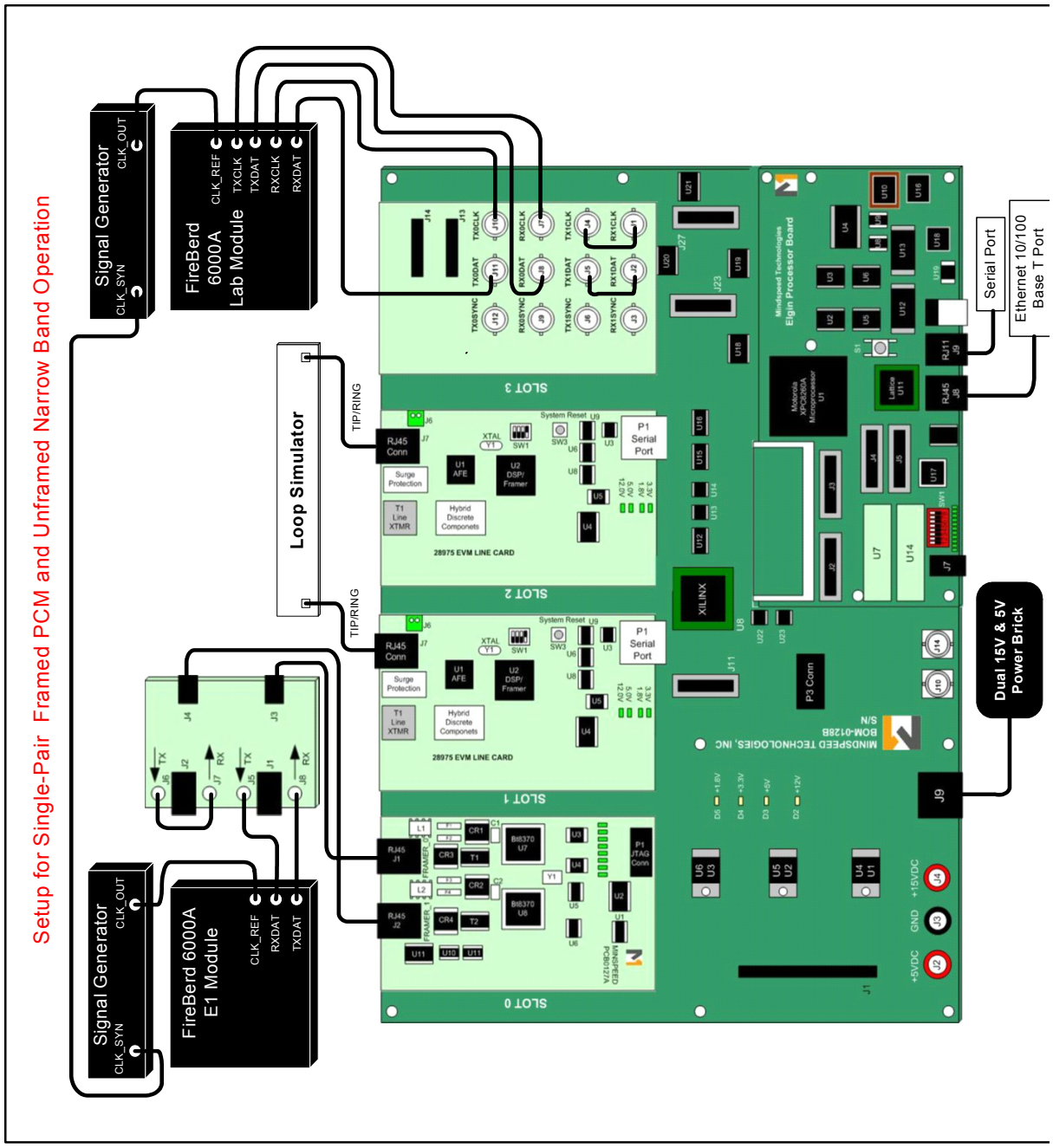
The following steps are required for running the ZipWirePlus Enhanced EVM in Single-Pair Framed PCM and Unframed Narrowband Operation. This setup needs one enhanced EVM.

This configuration is valid for M28945, M28946 and M28947 devices only.

The Hardware setup for this application is shown in Figure 3-56.

NOTE: This setup needs two(2) fireberds (one with 2M/nX64, one with Lab Interface Adapter). Please note that the Fireberds should have the same clock source. Two function generators have been used for that. Figure 3-56 illustrates the required interconnections.

Figure 3-56. Enhanced EVM Setup - Single-Pair Framed PCM and Unframed Narrowband Application



3.5.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. .
6. Fireberd Connections -
   - Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-C card. Connect the Function Generator #1 output (2048 khz signal) to the **GEN CLK IN** port on the Fireberd. Please note the reference signal from this Function Generator should be fed to Function Generator #2.
   - Fireberd #2 - Make the following connections
     – TX DATA (Fireberd) to RX0DAT (BNC Tester)
     – TX CLK OUT(Fireberd) to RX0CLK (BNC Tester)
     – RCV DATA (Fireberd) to TX0DAT (BNC Tester)
     – RCV CLK (Fireberd) to TX0CLK (BNC Tester)

   Connect the Function Generator #2 output (number of timeslots X 64 khz signal) to the **GEN CLK IN** port on the Fireberd.
7. BNC Tester Card Connections - Make the following connections
   - TX1DAT to RX1DAT
   - TX1CLK to RX1CLK
8. Loopback externally the FRAMER_1 of the Dual T1/E1 card using the T1/E1 cable adapter.
9. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.5.2 Fireberd Setup

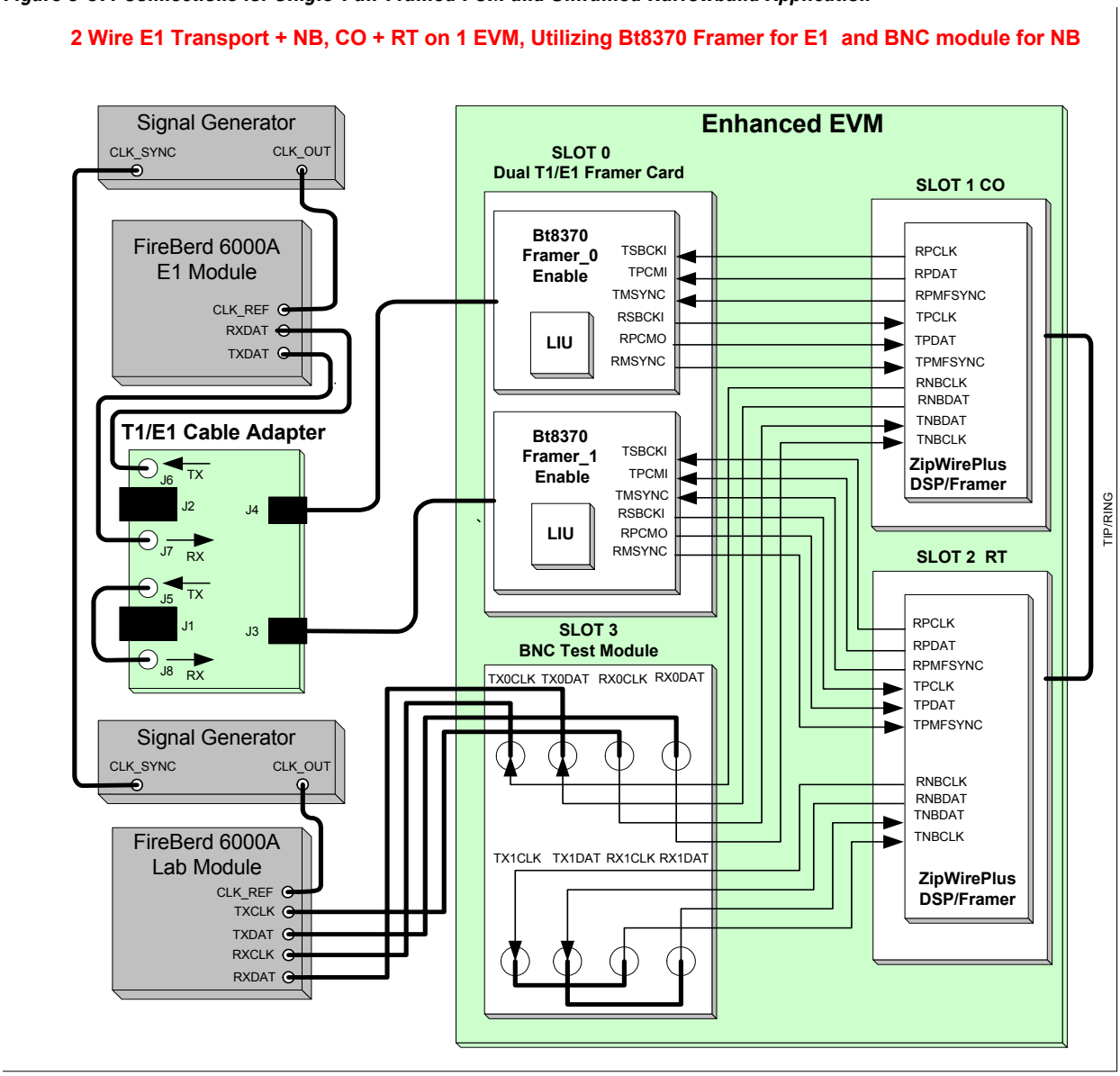
1. Configure the Fireberd #1 E1 Module front panel as follows:
   - DATA: 2^{23}-1
   - GEN CLK: BNC
   - INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
   - INTF SETUP: 2M/n64: MODE: FULL2M
2. Configure the Fireberd#2 Lab Interface Adapter as follows
   - DATA: 2^{23}-1

- GEN CLK: BNC

3.5.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - HTU-C) to the Framer #0 (slot 0) and the Narrowband bus of ZipWirePlus device (HTU-C) to the Port 0 of the BNC Tester Card (Slot 3). Likewise on the RT side, it will connect the PCM bus of ZipWirePlus device (slot 2- HTU-R) to the Framer #1 (slot 0) and the Narrowband bus of ZipWirePlus device (HTU-R) to the Port 1of the BNC Tester Card (Slot 3). The Figure 3-57 explains the pin interconnections for this application.

Figure 3-57. Connections for Single-Pair Framed PCM and Unframed Narrowband Application



3.5.4 Enhanced EVM Configuration

3.5.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28946 or M28947.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.5.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.5.5 TestExec

3.5.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the EnhancedEvm design file for the HTU-C Enhanced EVM.

3.5.5.2 Enhanced EVM Configuration

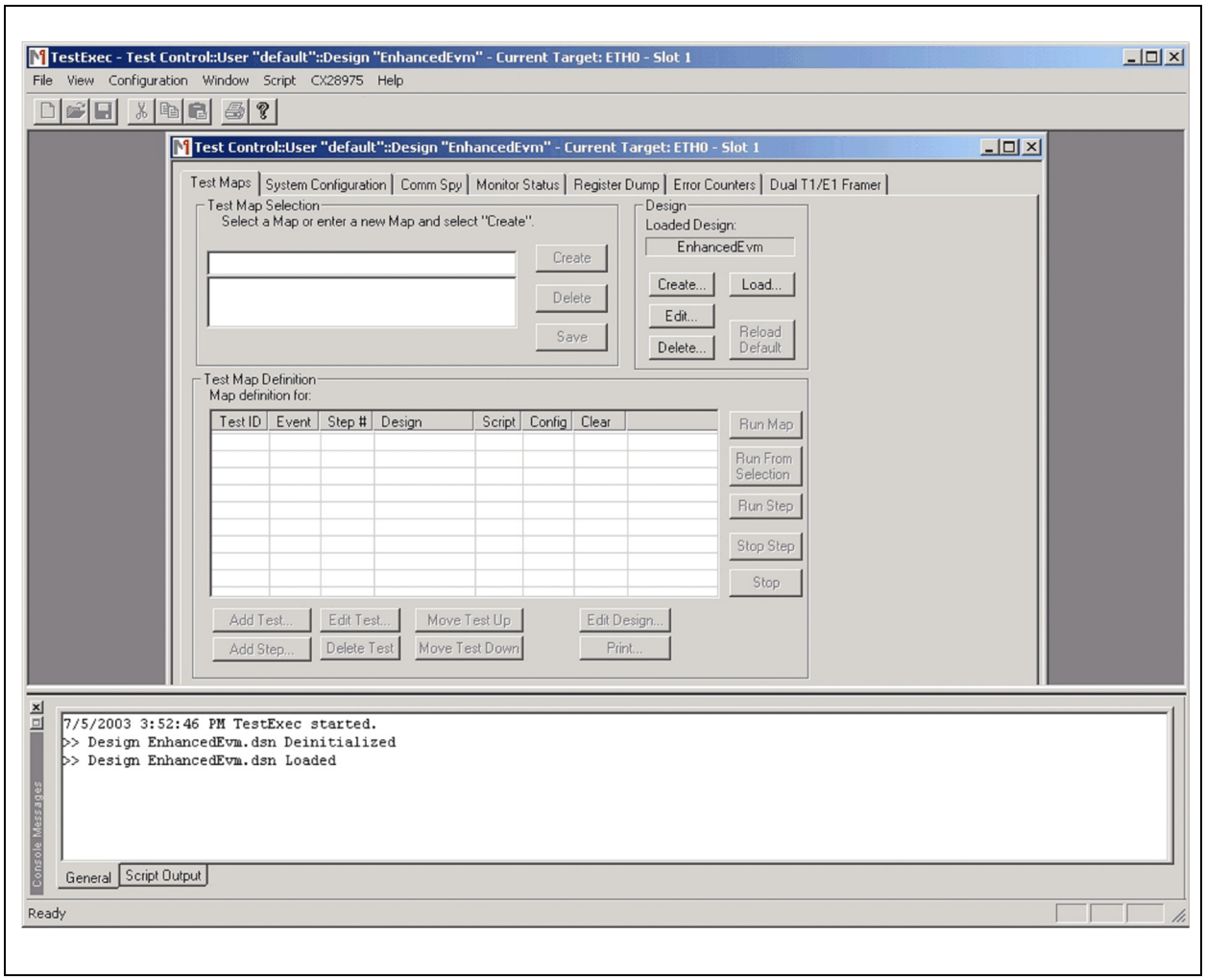
1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.

Figure 3-58. TestExec GUI after Design File is Loaded

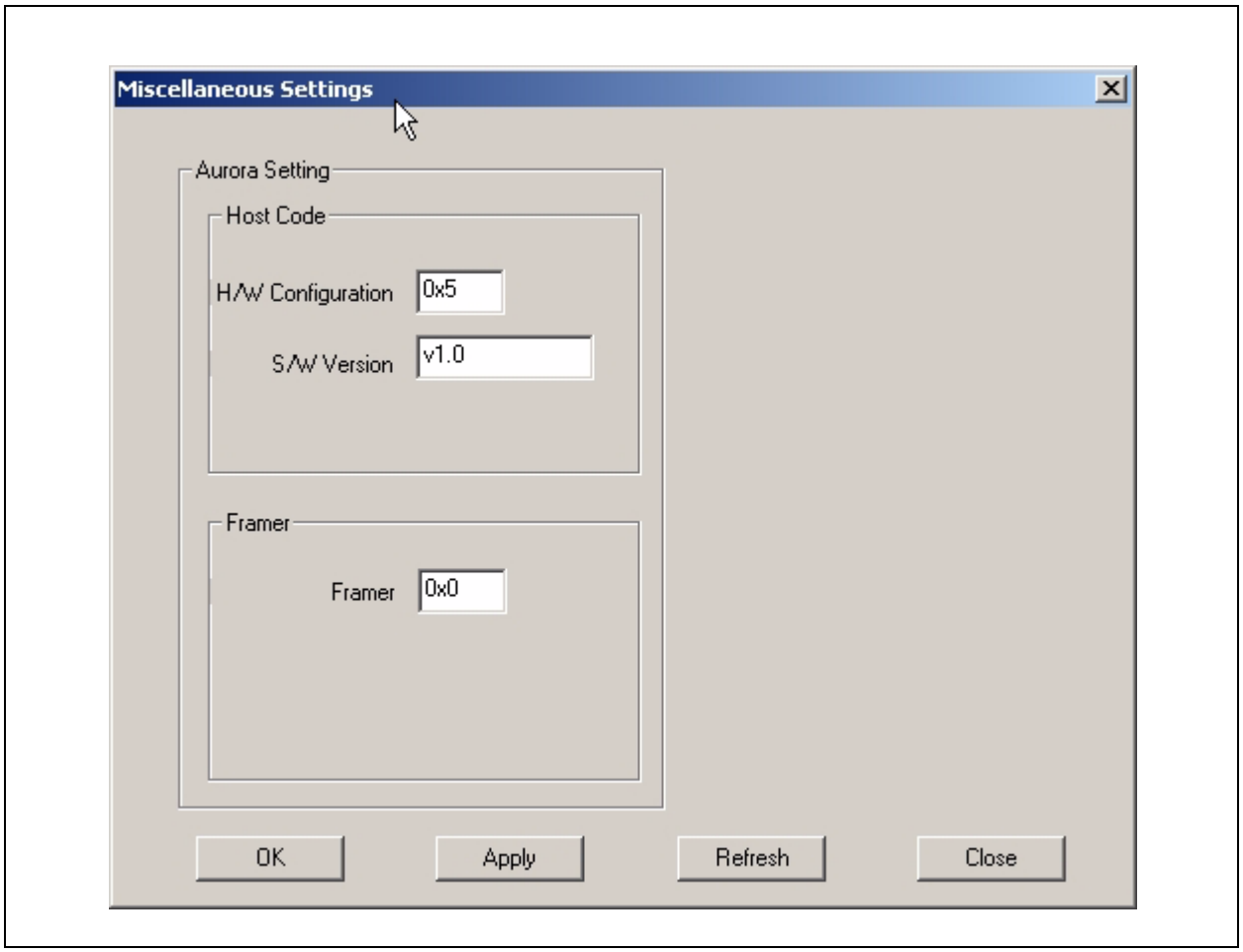


5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Select **Slot1** by right clicking the mouse.

3.5.5.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x5.
3. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

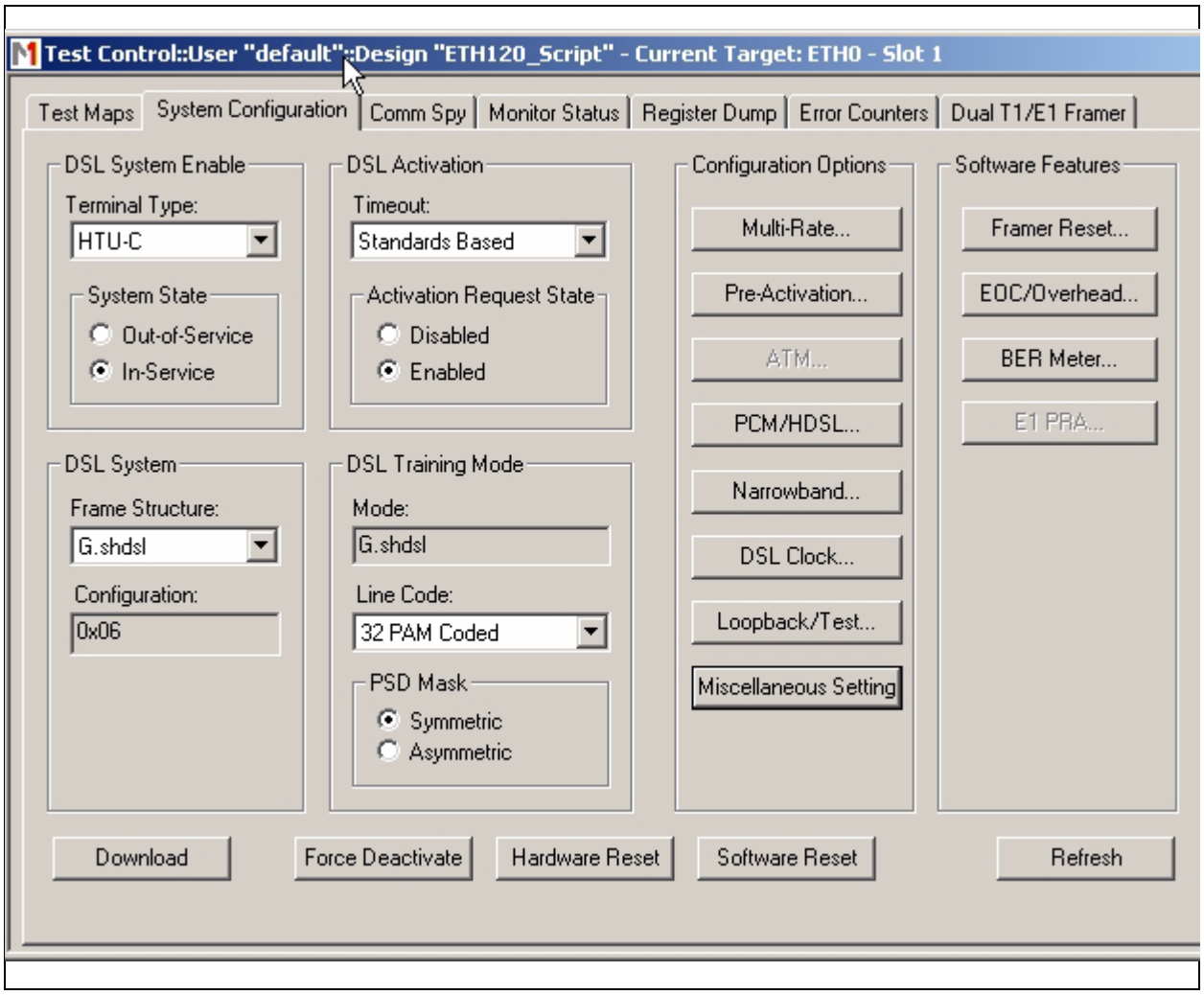
Figure 3-59. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM



3.5.5.2.2 Slot 1 (HTU-C)

1. Set the **System State** to **In-Service**.
2. Set the **Line Code** to be **32 PAM Coded**

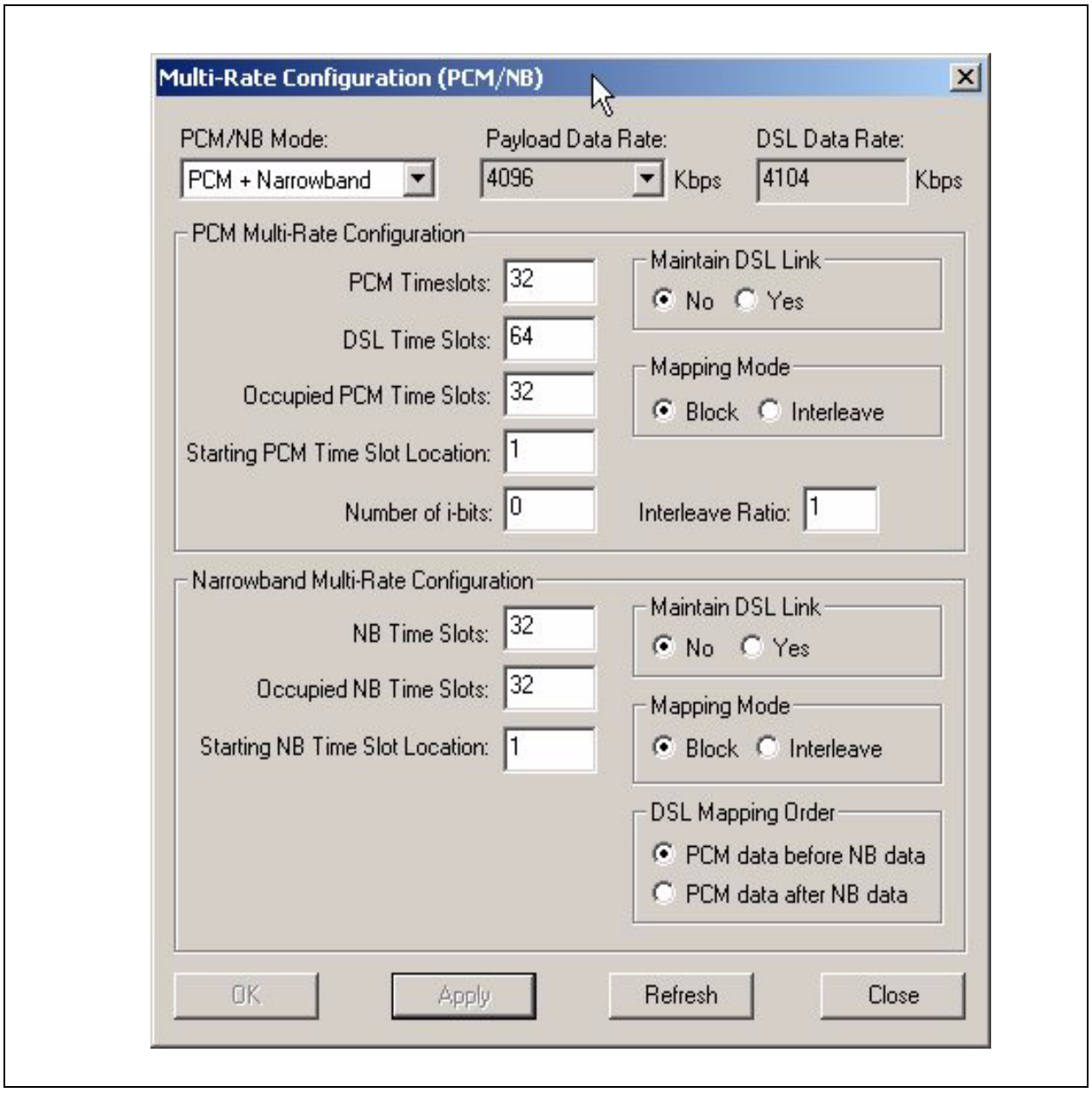
Figure 3-60. System Configuration Window for HTU-C



3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

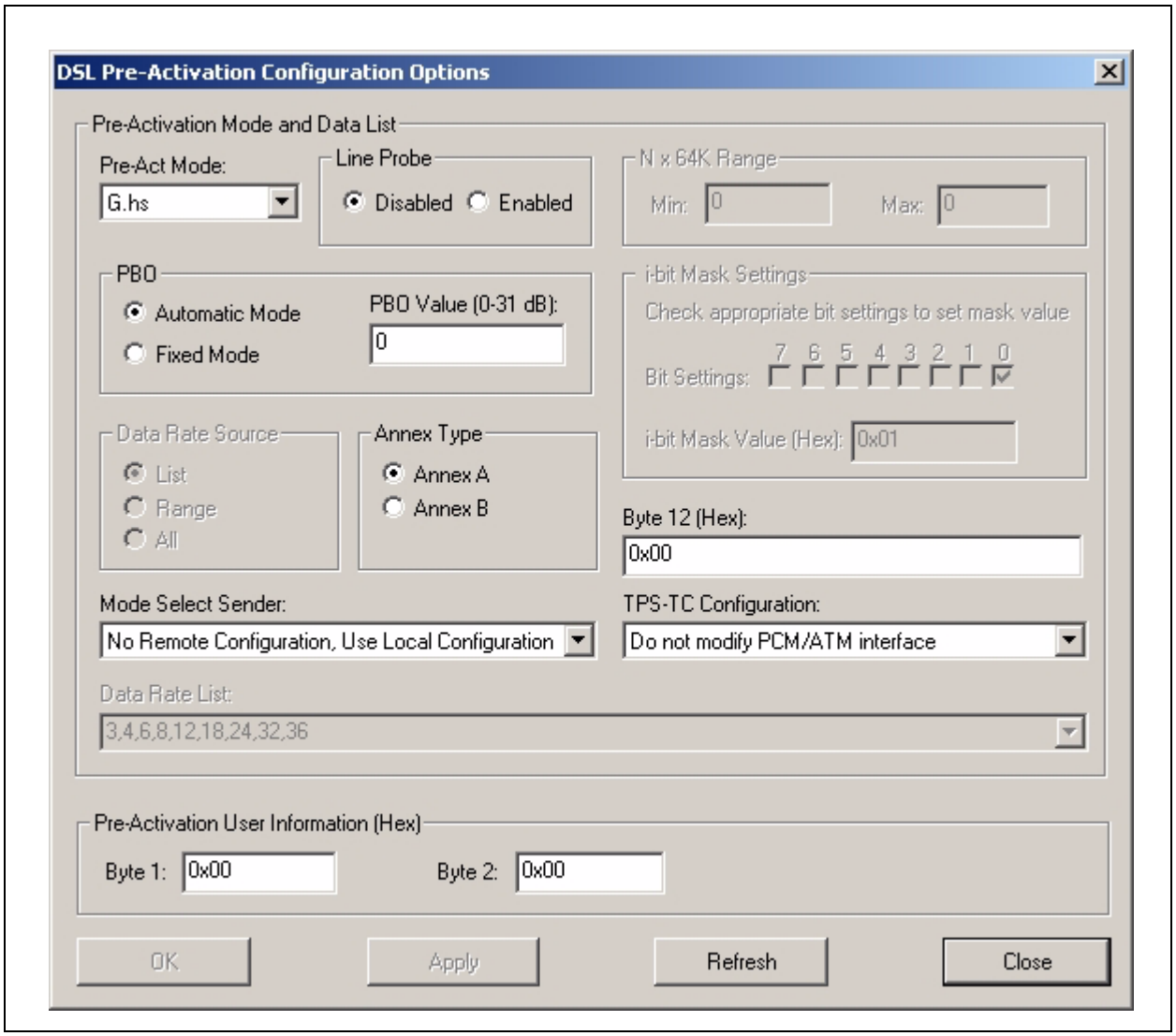
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **64**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **32**
- Starting NB Time Slot Location - **1**

Figure 3-61. TestExec Multi-Rate Configuration for HTU-C



5. Click the **Apply** button. The **Payload Data Rate** will change to 4096 Kbps and the **DSL Data Rate** will change to be 4104 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-62. TestExec Preactivation Configuration for HTU-C



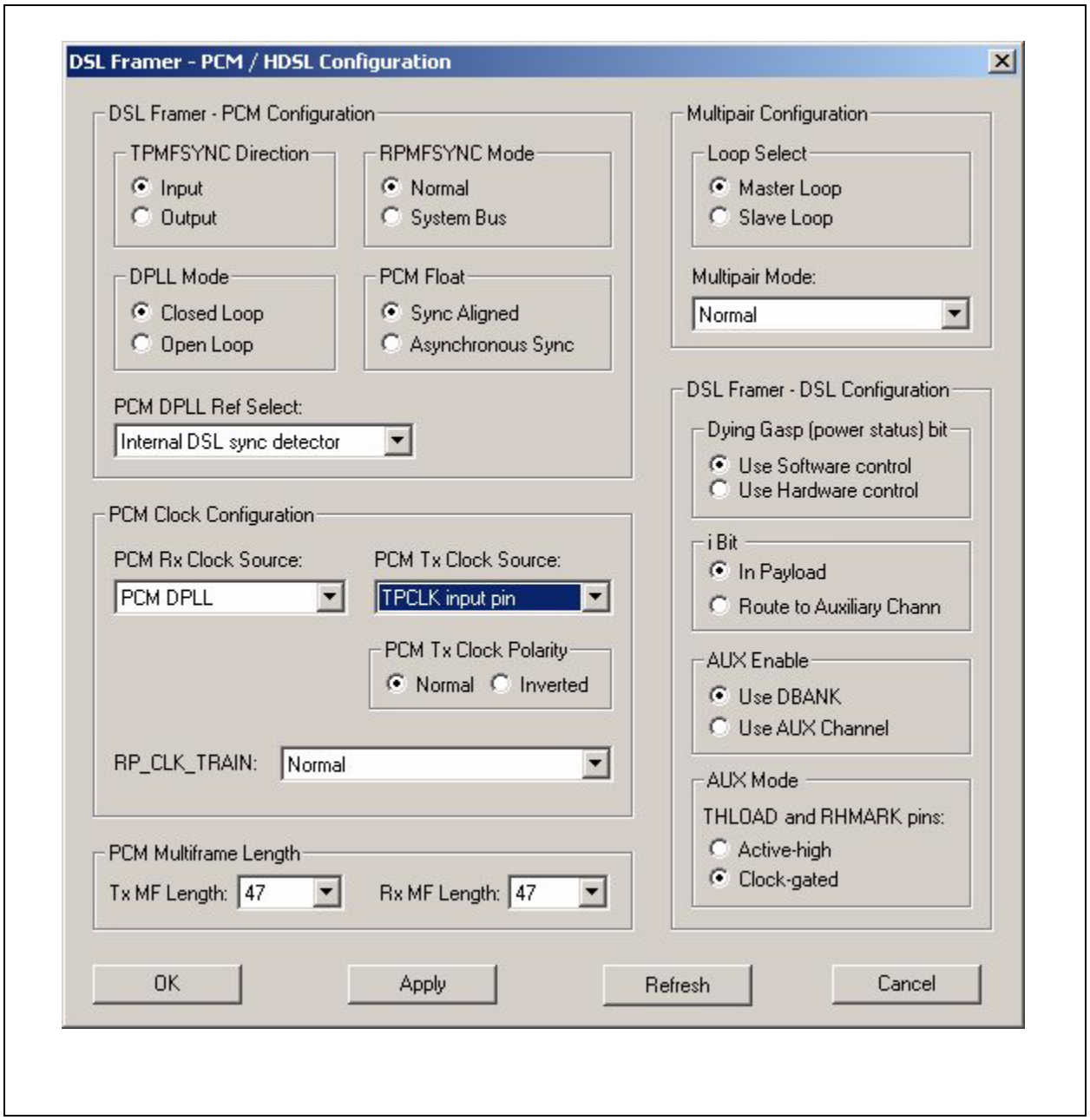
7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Change the **Mode Select Sender** to **No Remote Configuration, Use Local Configuration**..
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **PCM/HDSL** button.
11. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PCM DPLL**

- PCM Tx Clock Source - **TPCLK Input**
- PCM Tx Clock Polarity - **Normal**
- RP_CLK_TRAIN - **Normal**

- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-63. TextExec PCM/HDSL Configuration for HTU-C

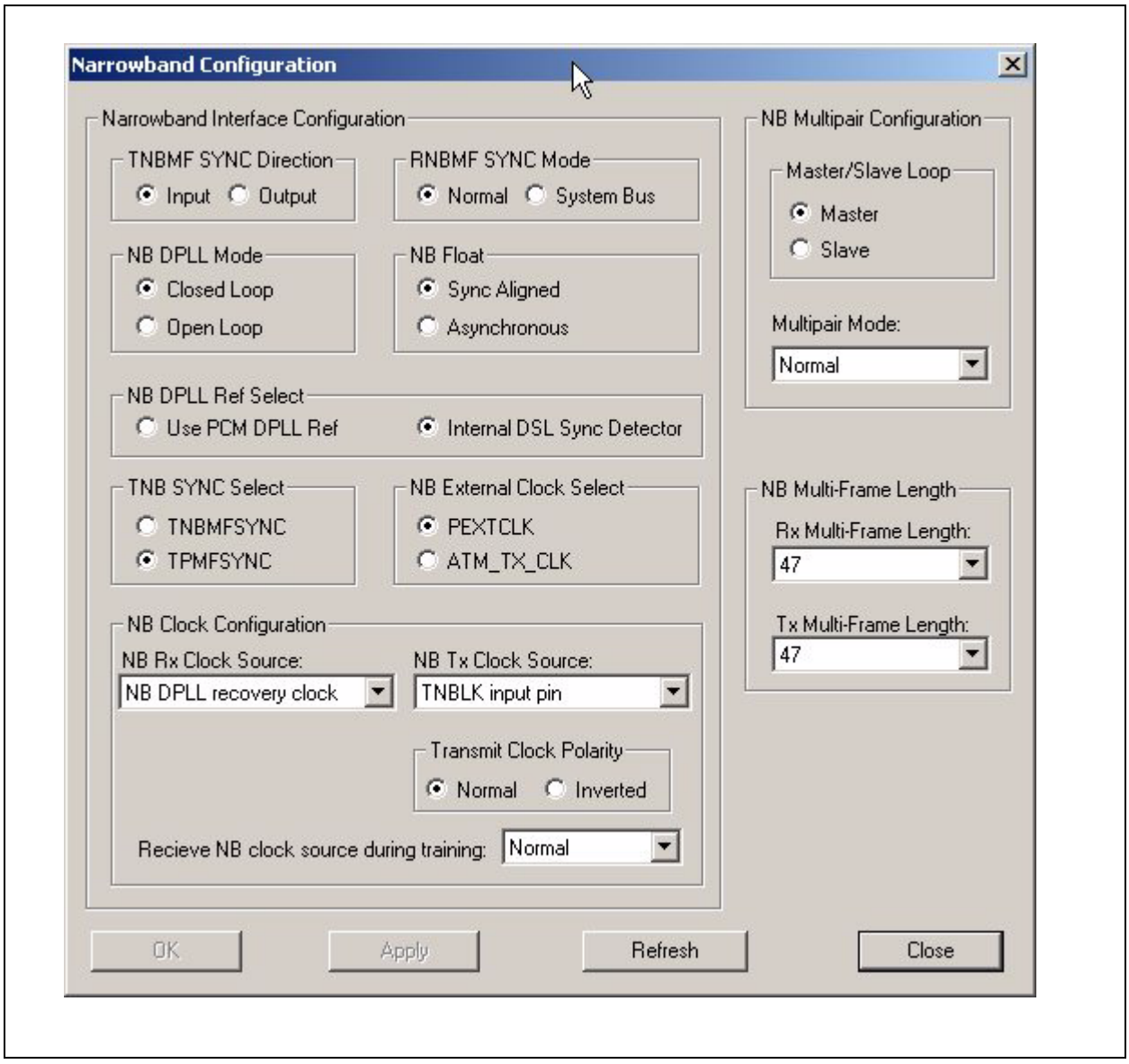


12. Click on **Apply** button and then click on the **Close** button.
13. Click on the **Narrowband** Button.
14. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**

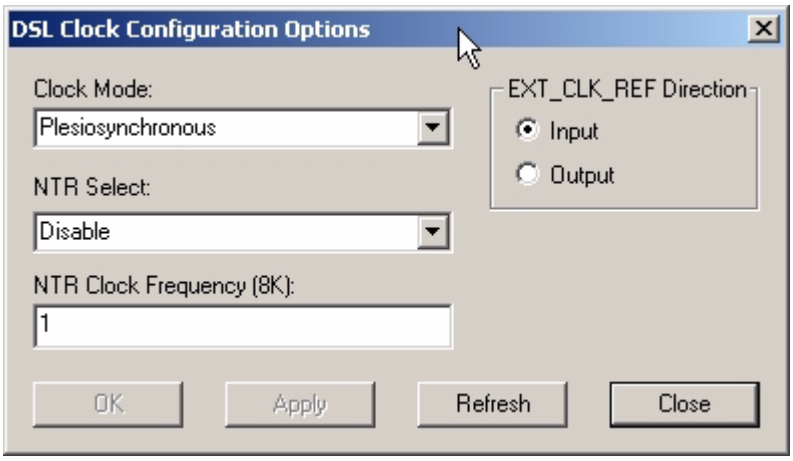
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**

Figure 3-64. TextExec Narrowband Configuration for HTU-C



15. Click on **Apply** button and then click on the **Close** button.
16. Click on the **DSL Clock** Button.
17. Enter the following values:

Figure 3-65. TextExec DSL Clock Configuration for HTU-C

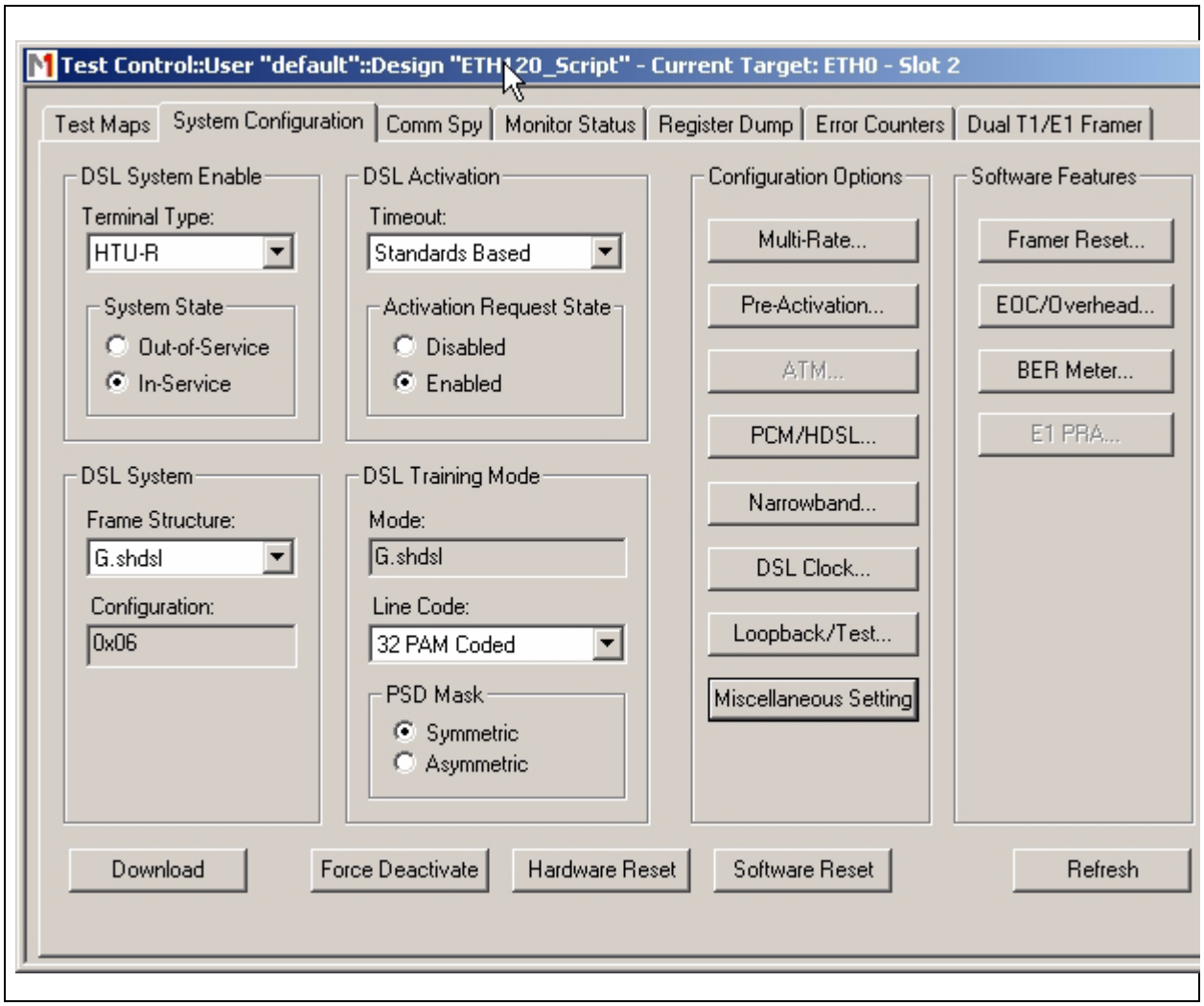


18. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
19. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.5.5.2.3 Slot 2 (HTU-R)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Set the **Line Code** to be **32 PAM Coded**

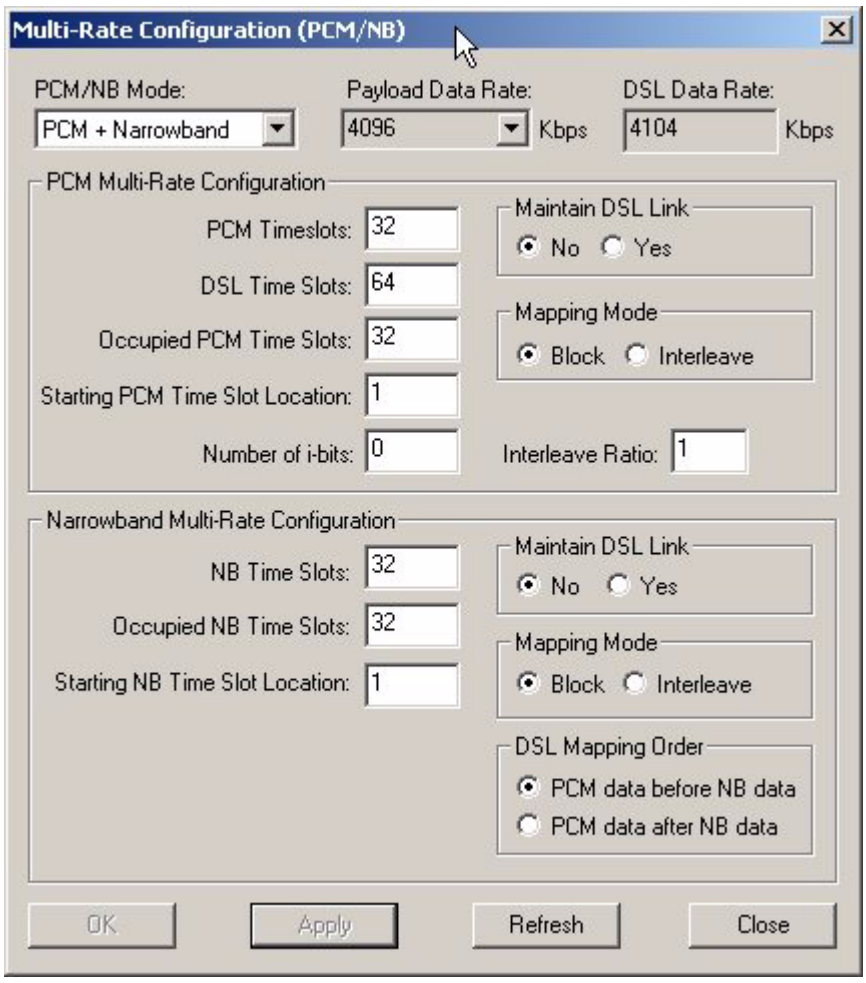
Figure 3-66. System Configuration for HTU-R



4. Click on the **Multi-Rate** Button.
5. Enter the values as follows:

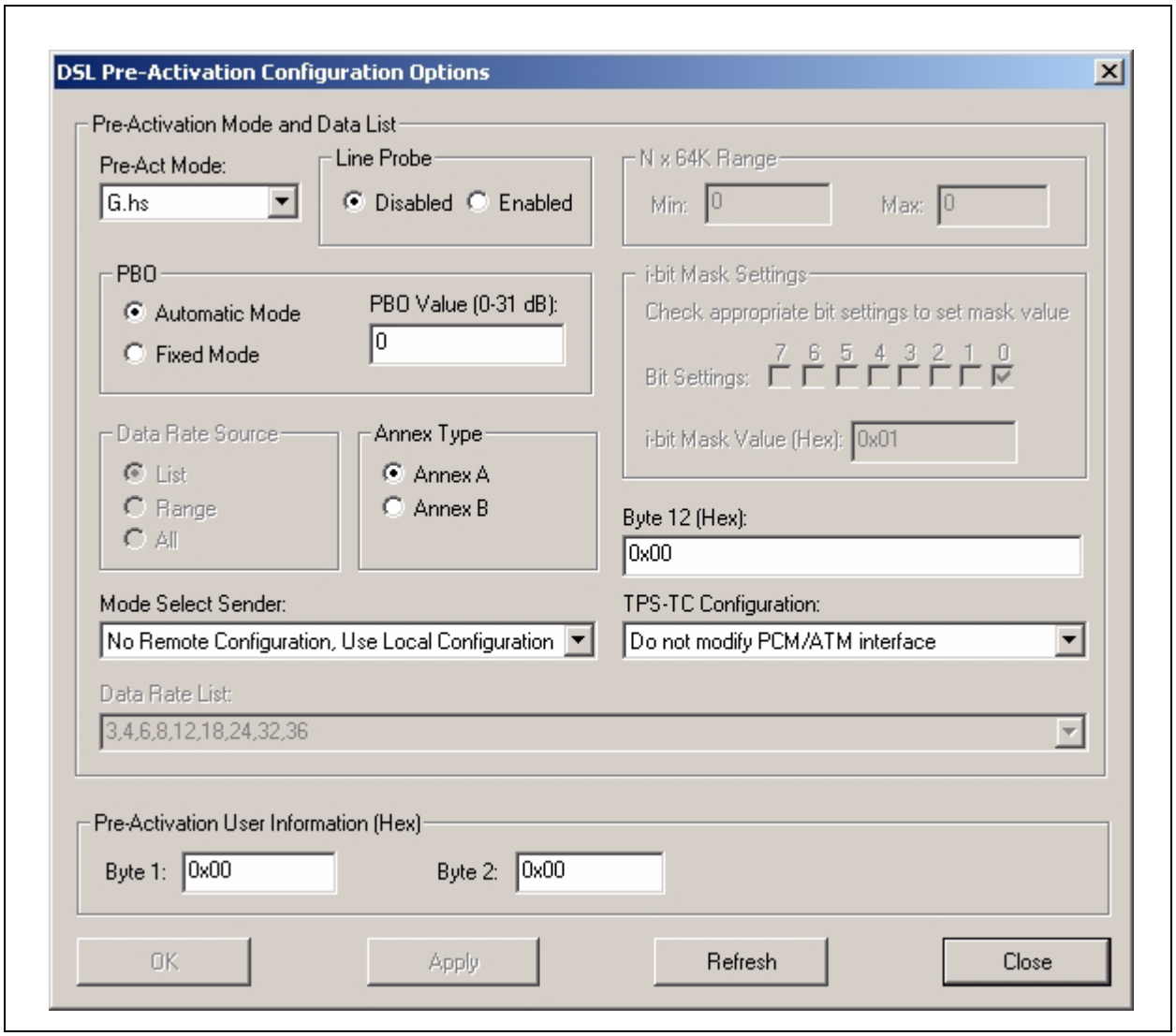
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **64**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **32**
- Starting NB Time Slot Location - **1**

Figure 3-67. TestExec Multi Rate Configuration for HTU-R



6. Click the **Apply** button. The Payload Data Rate will change to 4096 Kbps and the DSL Data Rate will change to be 4104 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

Figure 3-68. TestExec Preactivation Configuration for HTU-R



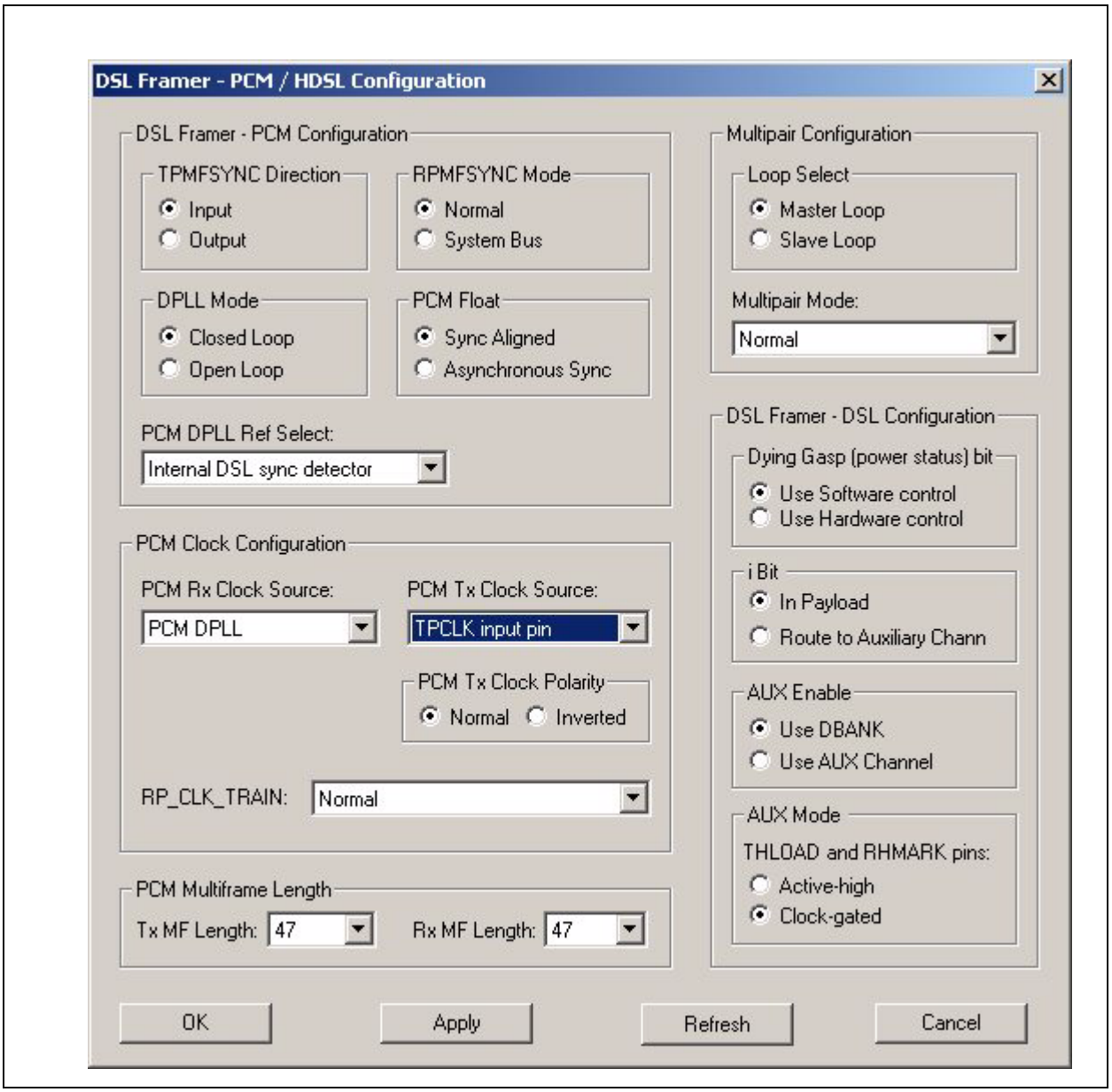
8. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
9. Change the **Mode Select Sender** to **No Remote Configuration, Use Local Configuration**.
10. Click on **Apply** button and then click on the **Close** button.
11. Click on the **PCM/HDSL** button.
12. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PCM DPLL**

- PCM Tx Clock Source - **TPCLK Input**
- PCM Tx Clock Polarity - **Normal**
- RP_CLK_TRAIN - **Normal**

- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-69. TestExec PCM/HDSL Configuration for HTU-R

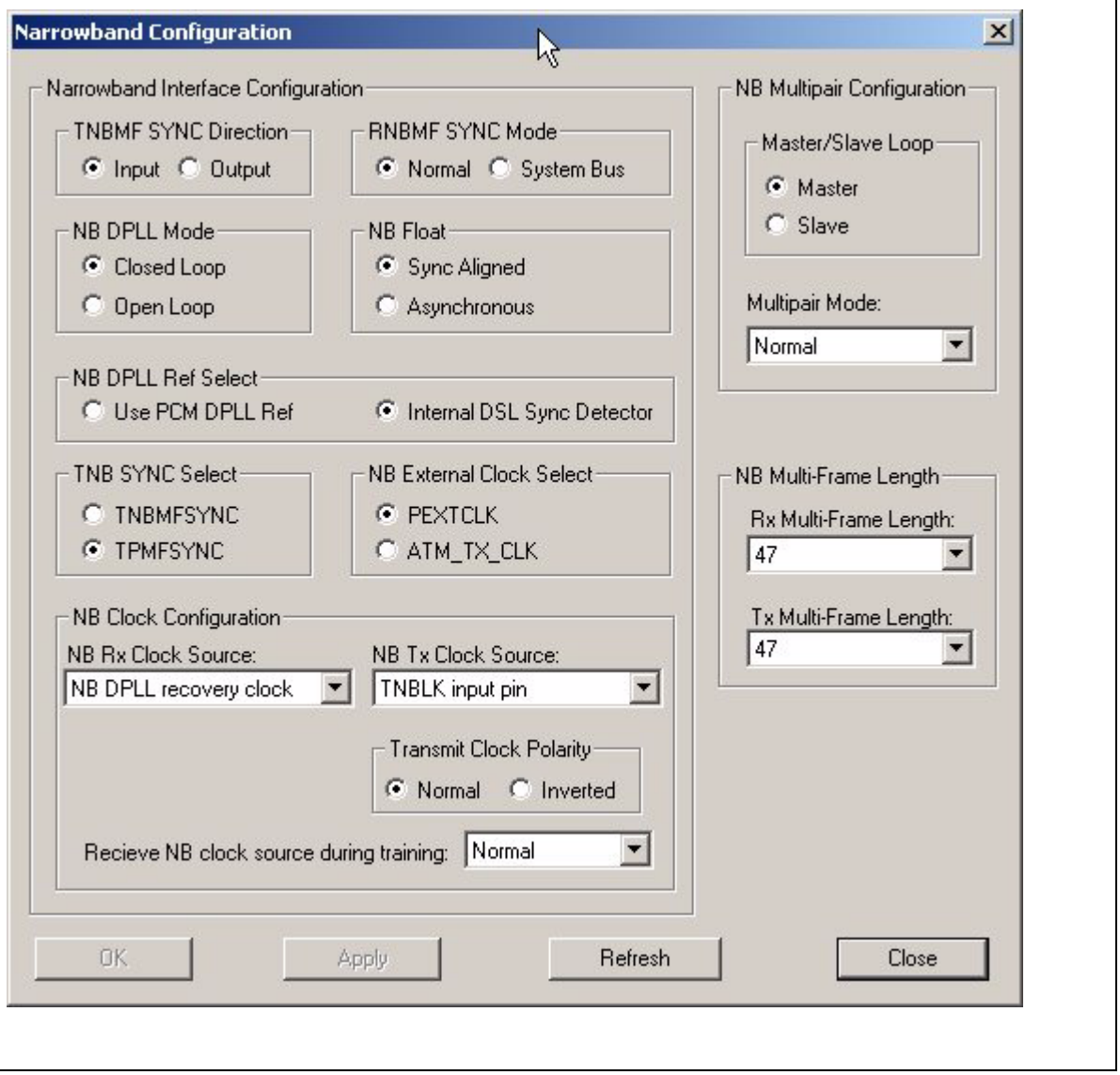


13. Click on **Apply** button and then click on the **Close** button.
14. Click on the **Narrowband** Button.
15. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**

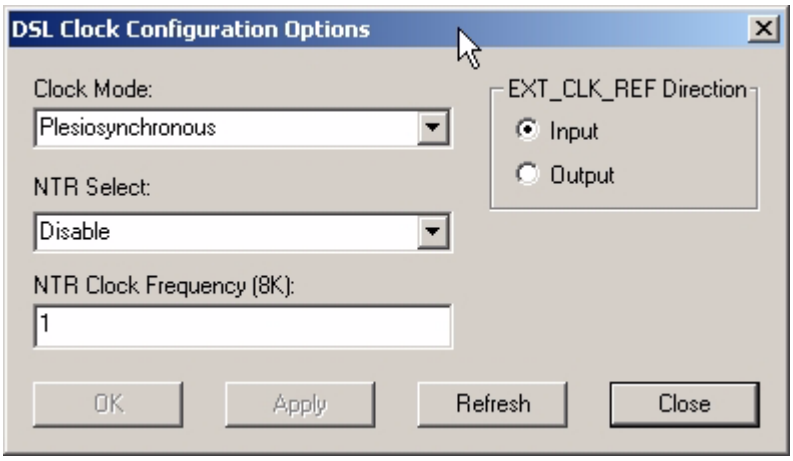
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**

Figure 3-70. TextExec Narrowband Configuration for HTU-C



16. Click on **Apply** button and then click on the **Close** button.
17. Click on the **DSL Clock** Button.
18. Enter the following values:

Figure 3-71. TextExec DSL Clock Configuration for HTU-R



19. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.5.5.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.

3.5.5.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-56. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.5.5.4 Varying the rates for PCM and Narrowband

The above configuration transports 32 timeslots of framed PCM data and 32 timeslorts of unframed Narrowband data. The user can vary the rates for PCM and Narrowband. Please note that the user would need to set the water level for the PCM and Narrowband traffic. This can be done through the Comm Spy window in the

TestExec using the APIs _DSL_PCM_WATER_LEVEL (0x2C) and _DSL_NB_WATER+LEVEL (0x2D).

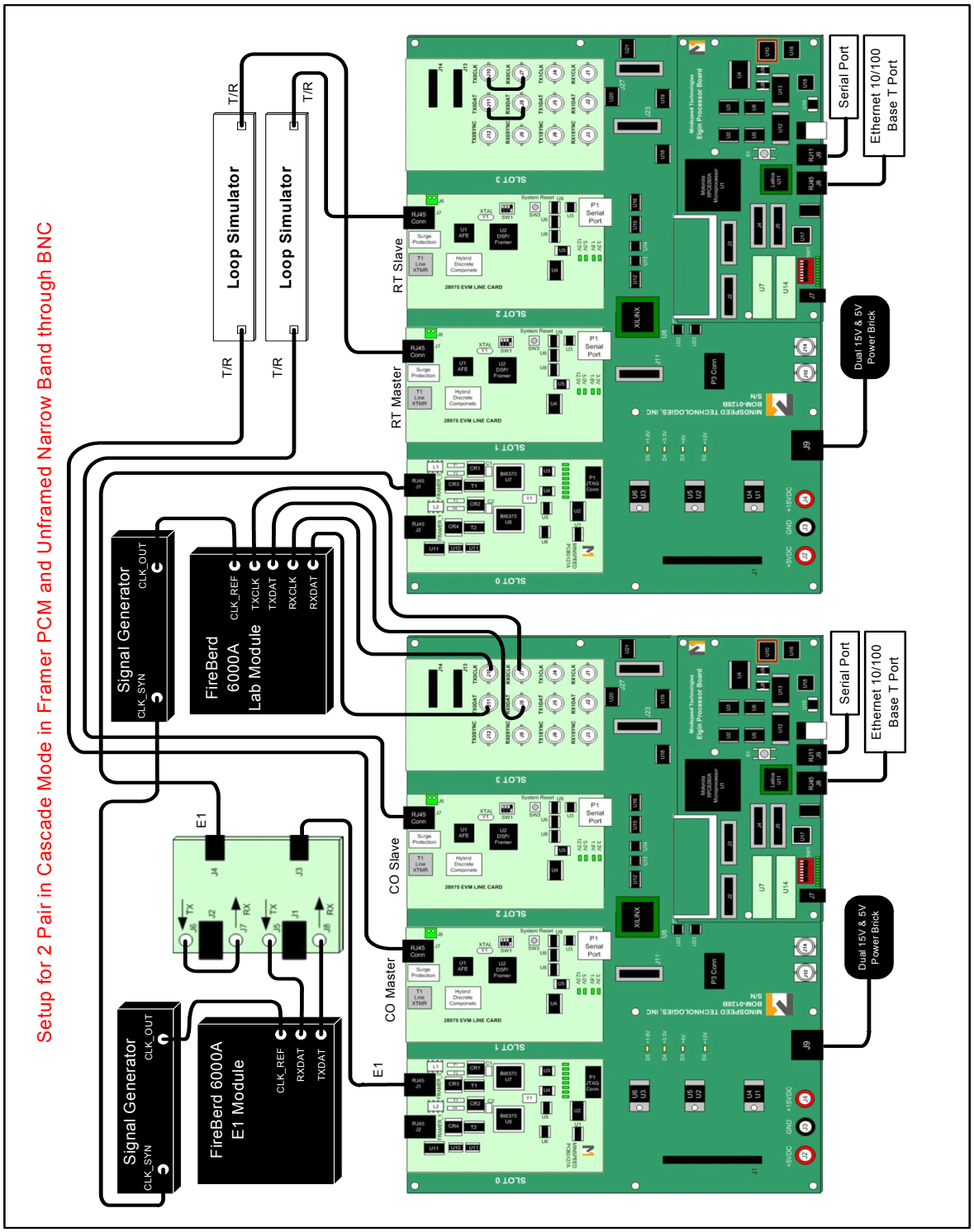
3.6 Enhanced EVM Setup for Multi-pair Cascade Mode in Framer PCM and Unframed Narrowband Operation

The following steps are required for running the ZipWirePlus Enhanced EVM in Multi-Pair Cascade Mode PCM + Narrowband Operation. This setup needs two enhanced EVMs.

First, we shall use only the HTU-C EVM and put the DSL side is put into loopback. Then we shall perform end to end testing with two enhanced EVMs. The Hardware setup for this application is shown in Figure 3-72.

NOTE: This setup needs two(2) fireberds (one with 2M/nX64, one with Lab Interface Adapter). Please note that the Fireberds should have the same clock source. Two function generators have been used for that. Figure 3-72 illustrates the required interconnections.

Figure 3-72. Enhanced EVM Setup for Two-Pair PCM + Narrowband (unframed) Operation



3.6.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -
   - Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-C PCM Ports. Connect the Function Generator #1 output (2048 khz signal) to the **GEN CLK IN** port on the Fireberd. Please note the reference signal from this Function Generator should be fed to Function Generator #2.
   - Fireberd #2 - Make the following connections
     – TX DATA (Fireberd) to RX0DAT (BNC Tester)
     – TX CLK OUT(Fireberd) to RX0CLK (BNC Tester)
     – RCV DATA (Fireberd) to TX0DAT (BNC Tester)
     – RCV CLK (Fireberd) to TX0CLK (BNC Tester)

   Connect the Function Generator #2 output (number of timeslots X 64 khz signal) to the **GEN CLK IN** port on the Fireberd.
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

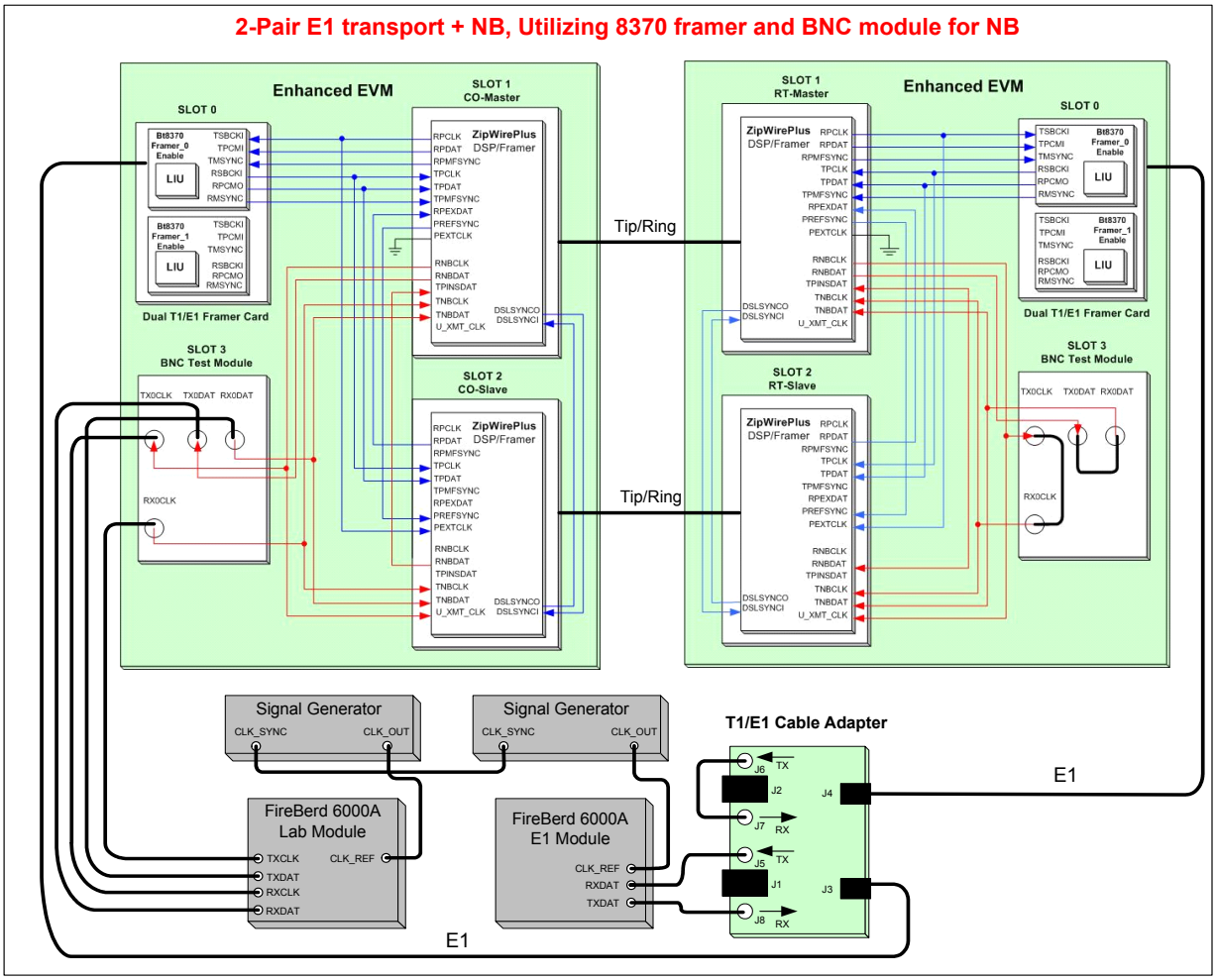
3.6.2 Fireberd Setup

1. Configure the Fireberd #1 E1 Module front panel as follows:
   - DATA: 2^{23}-1
   - GEN CLK: BNC
   - INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
   - INTF SETUP: 2M/n64: MODE: FULL2M
2. Configure the Fireberd#2 Lab Interface Adapter as follows
   - DATA: 2^{23}-1
   - GEN CLK: BNC

3.6.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Framer #0 (slot 0) and the Narrowband bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Port 0 of the BNC Tester Card(slot 3). The Figure 3-73 explains the pin interconnections for this application.

Figure 3-73. Connections for Multi-Pair Framed PCM + Narrowband (unframed) Application in Cascade Mode



3.6.4 Enhanced EVM Configuration

3.6.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28945, M28946 or M28947.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.6.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.6.5 TestExec

3.6.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software.

We will use the EnhancedEvm design file for the HTU-C Enhanced EVM.

3.6.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup.
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

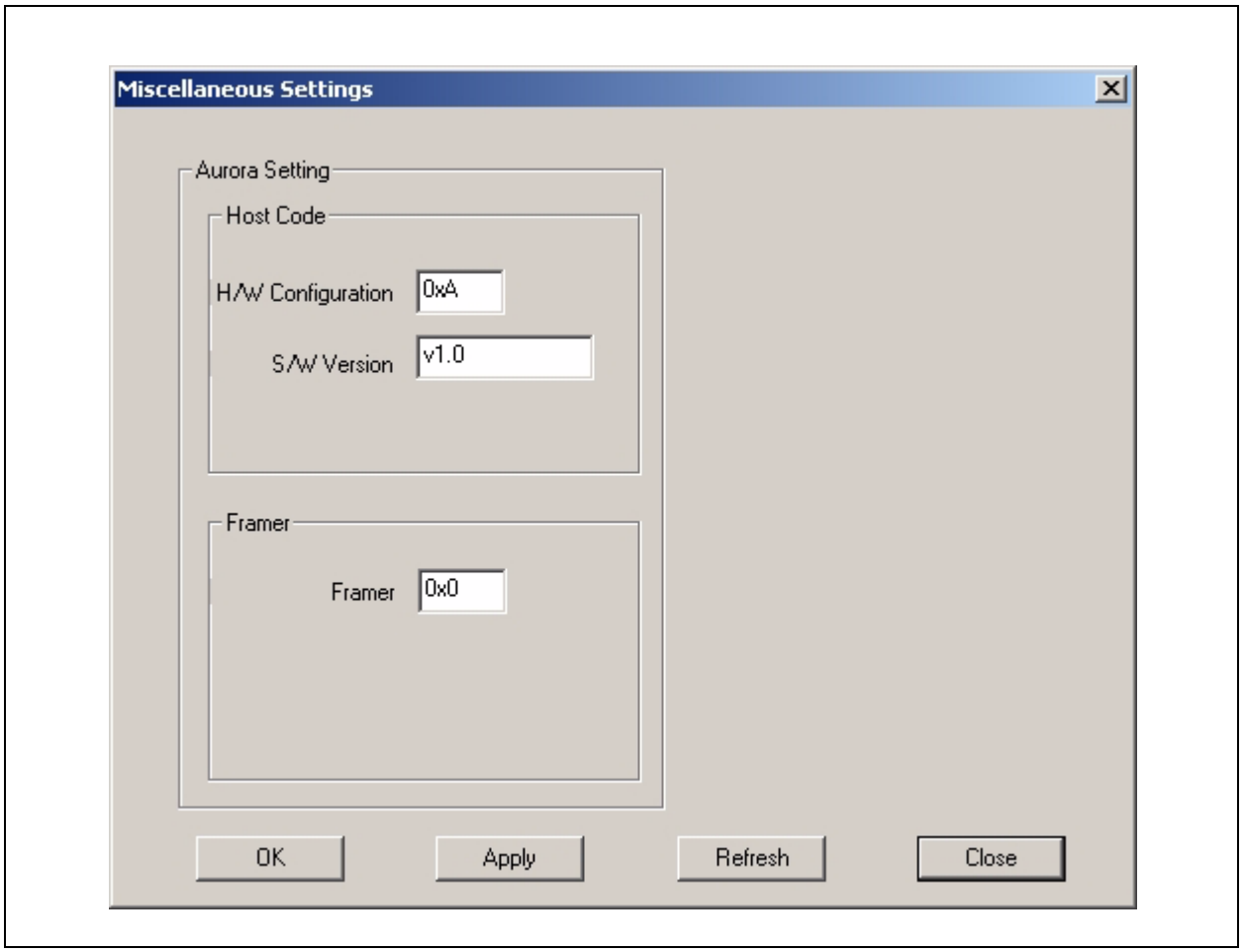
   b.**EnhancedEvm2**

   c.**LegacyEvm**
5. Select the **EnhancedEvm** design file. The TestExec will load the selected design file. Please note that for the HTU-C (CO) side EVM please select **EnhancedEvm** design file. For HTU-R (RT) side EVM please select the **EnhancedEvm2** design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. Select **Slot 1** by right clicking the mouse.

3.6.5.2.1 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0x0A.
4. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-74. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

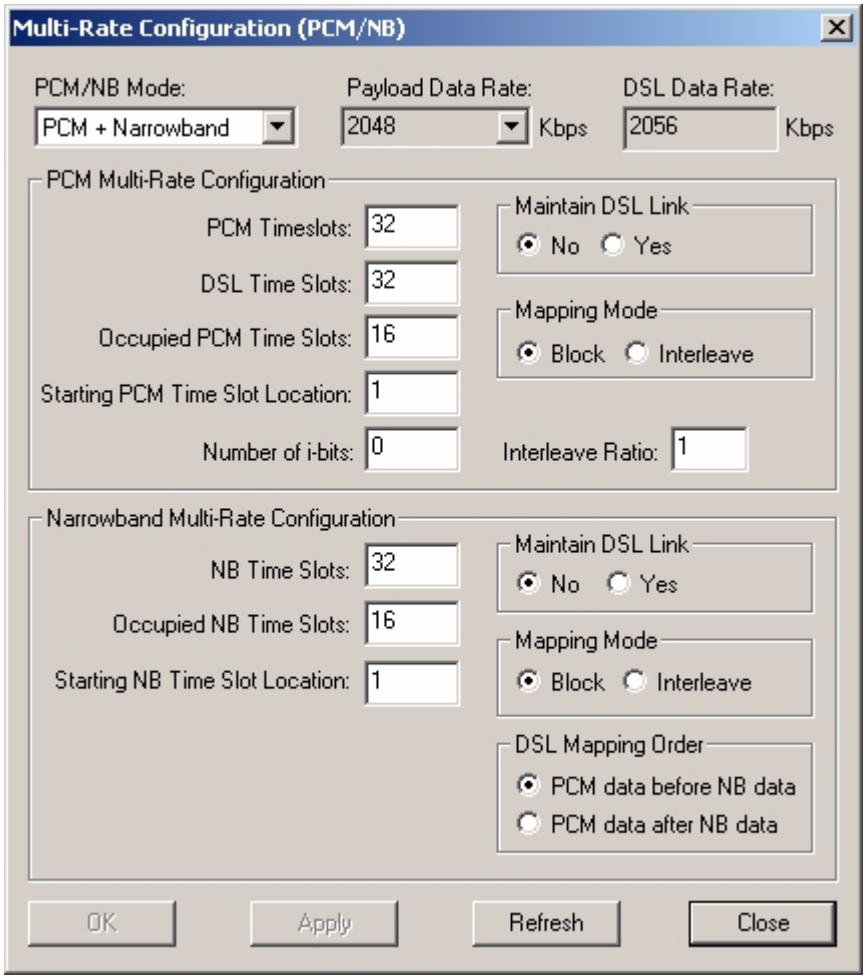


3.6.5.2.2 Slot 1 (HTU-C Master)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

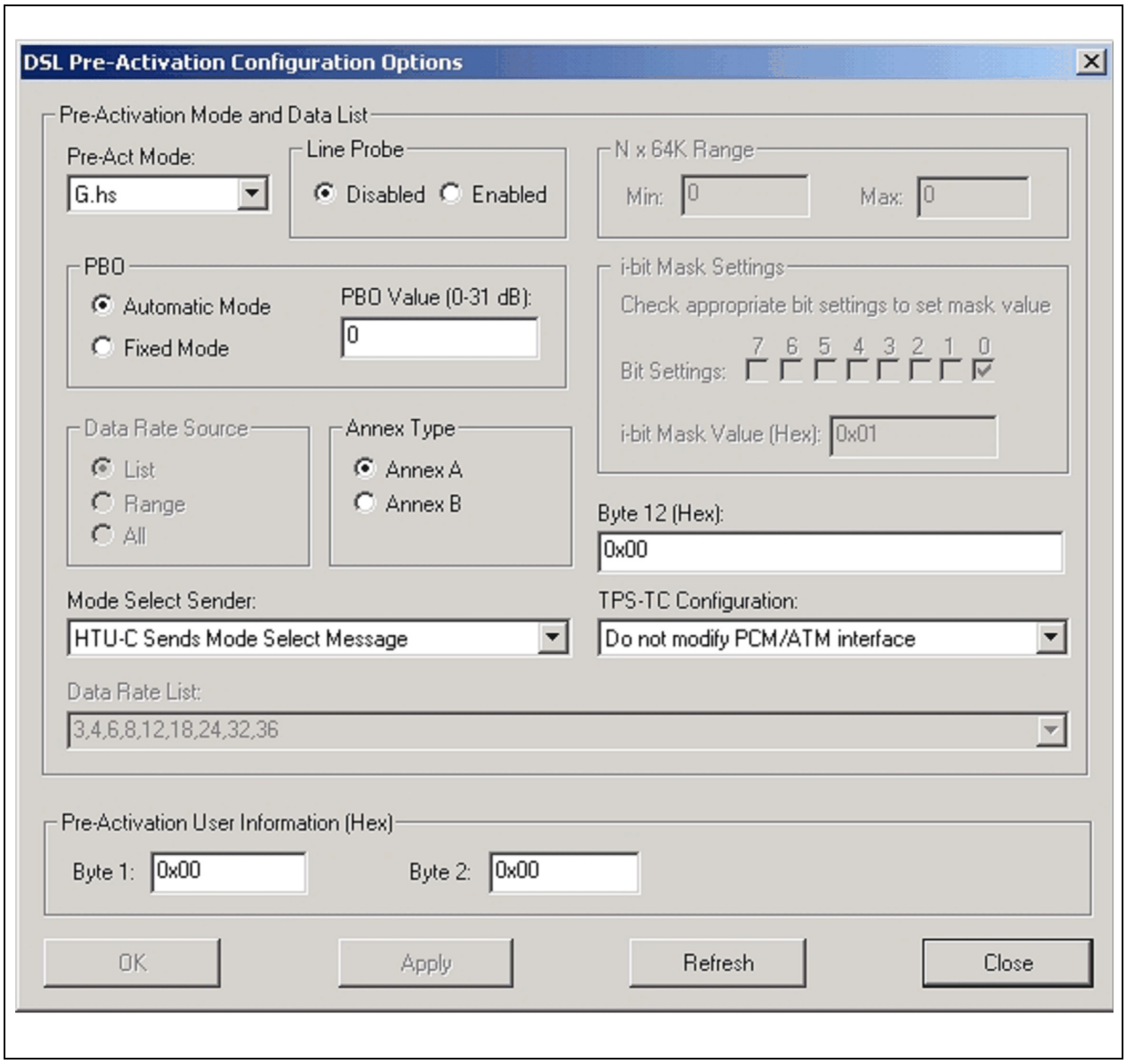
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **16**
- Starting NB Time Slot Location - **1**

Figure 3-75. TestExec Multi-Rate Configuration for Master



5. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-76. TestExec Preactivation Configuration for Master

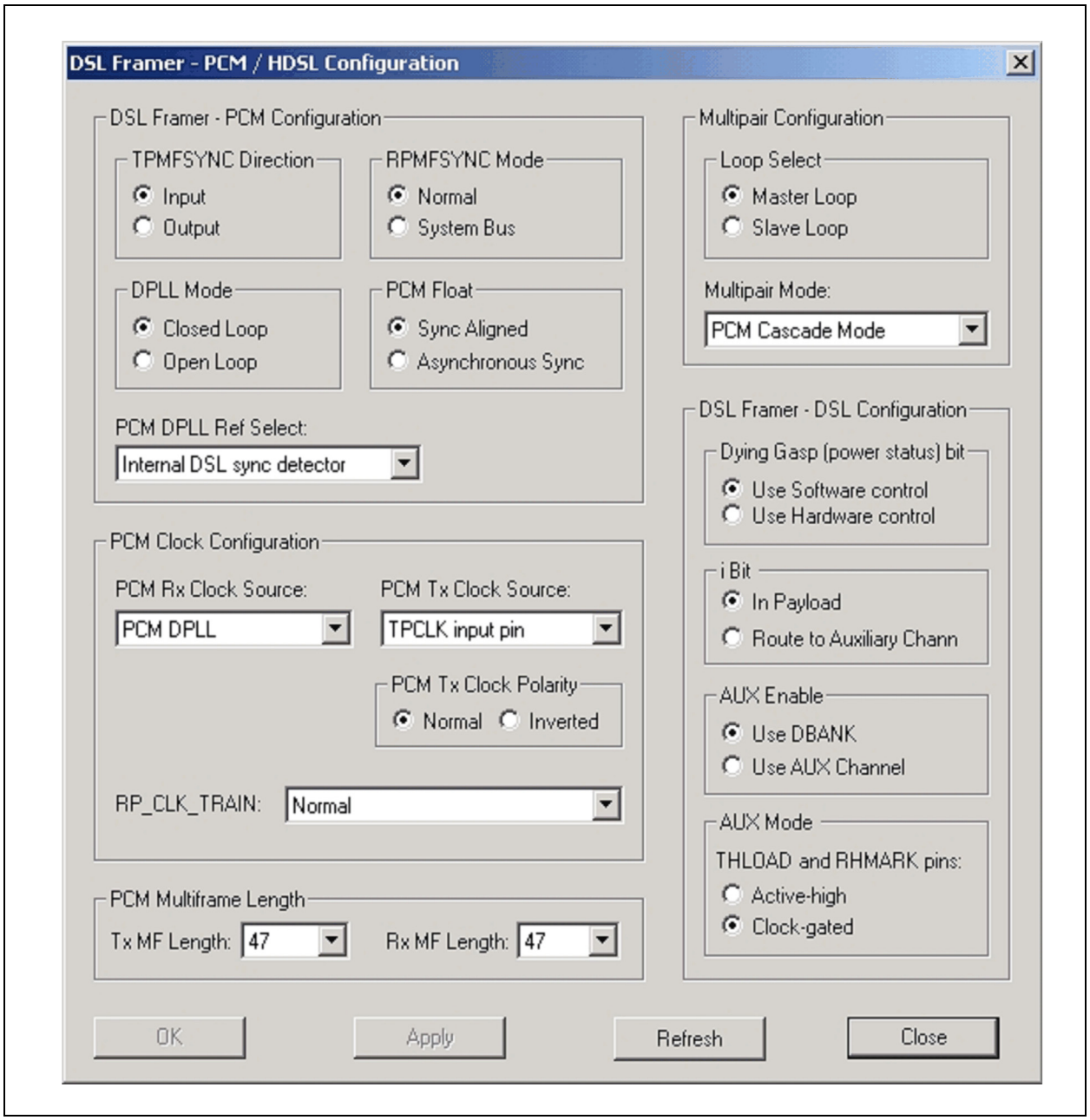


7. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration

  - PCM Rx Clock Source - **PCM DPLL**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-77. TextExec PCM/HDSL Configuration for Master

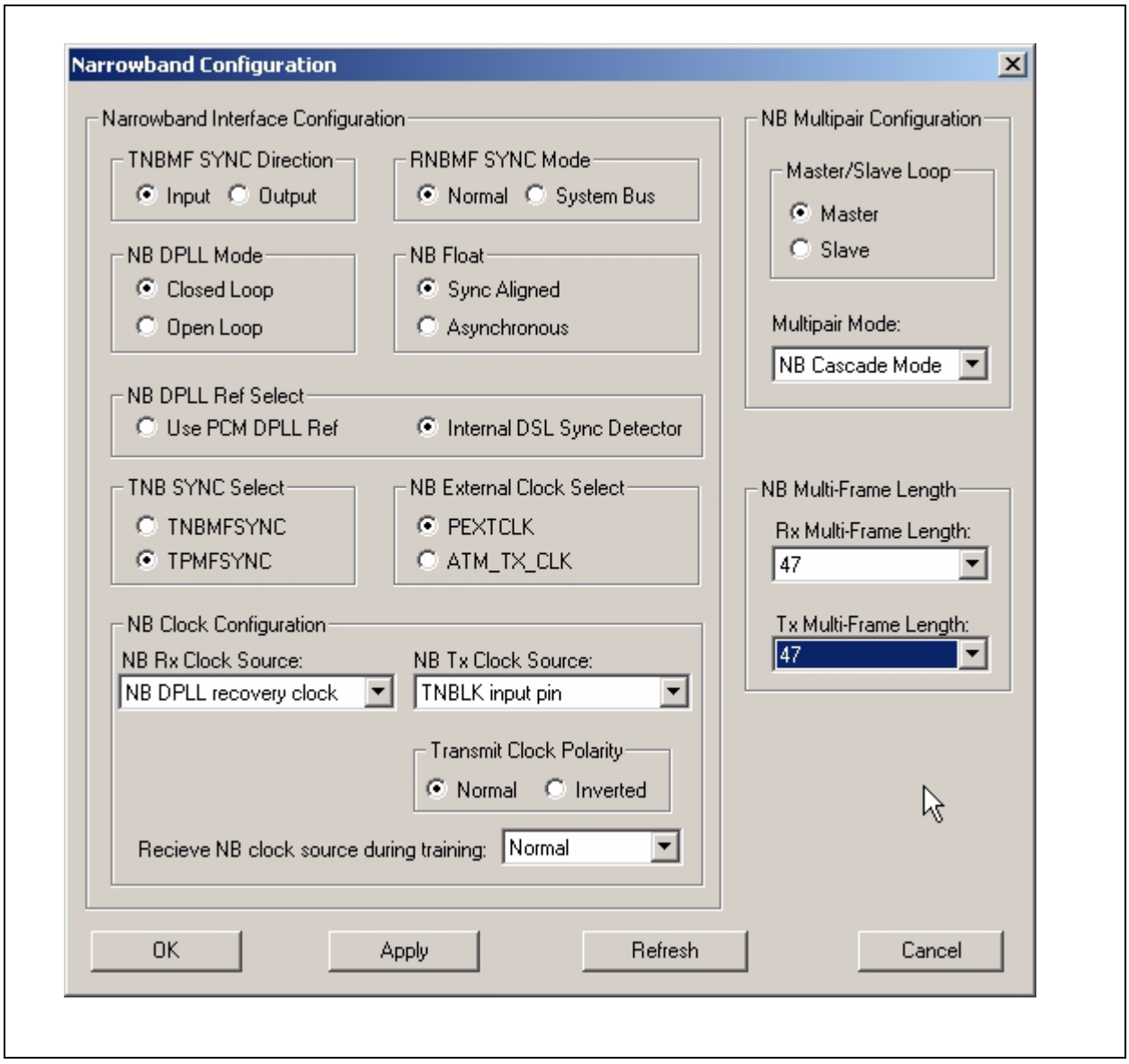


11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **Narrowband** Button.
13. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**

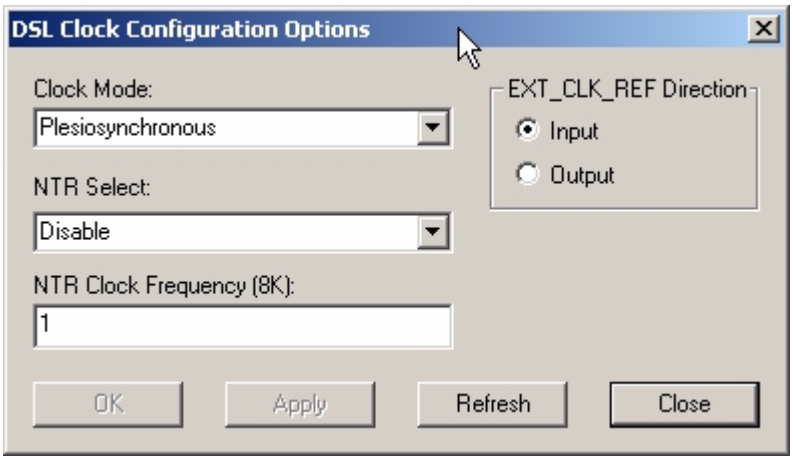
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**

Figure 3-78. TextExec Narrowband Configuration for Master



14. Click on **Apply** button and then click on the **Close** button.
15. Click on the **DSL Clock** Button.
16. Enter the following values:

Figure 3-79. TextExec DSL Clock Configuration for Master



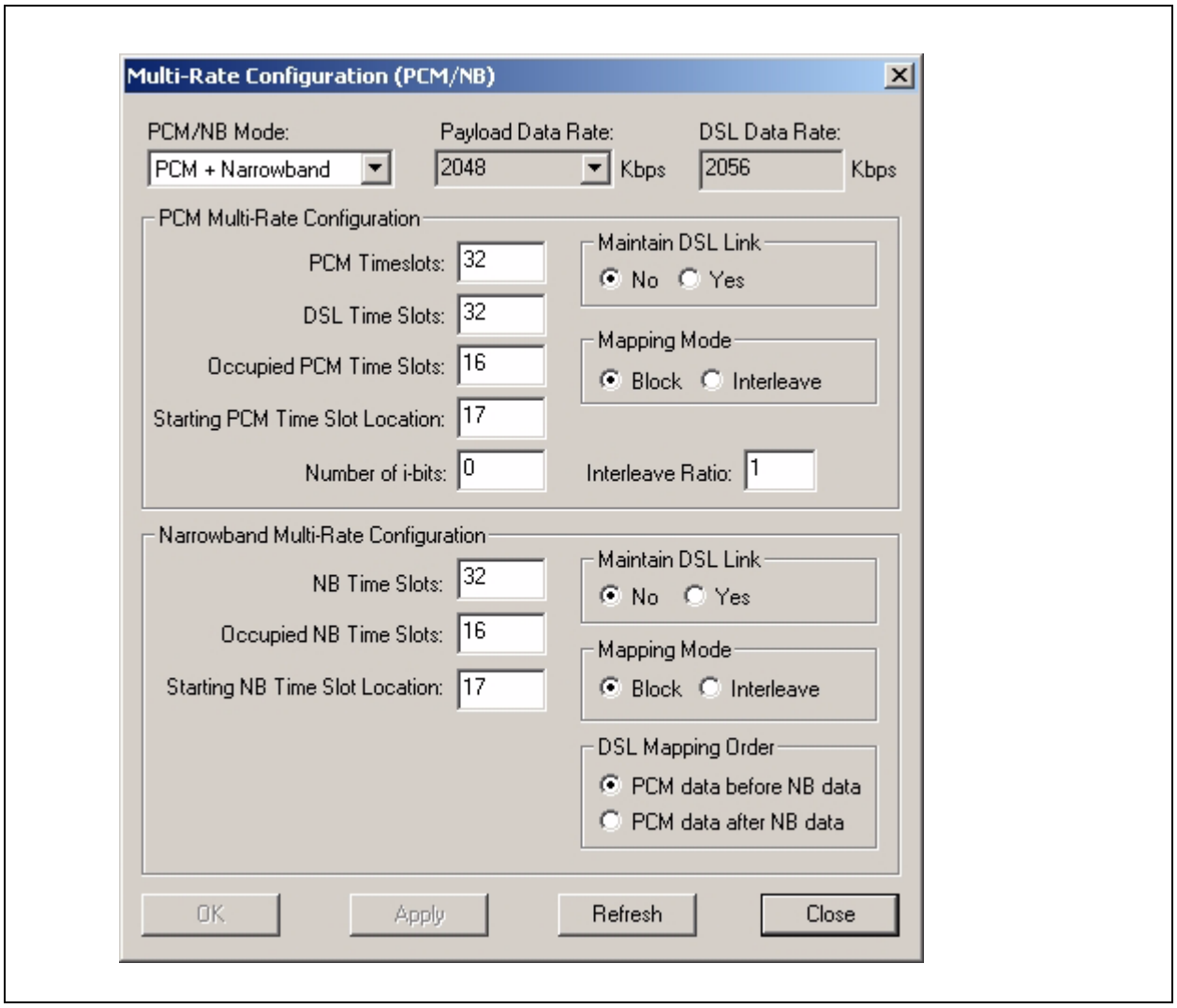
17. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
18. For setting the water level for the Narrowband Interface, Click on **Comm Spy** Tab.
19. Enter the following values
    - Opcode (HEX) - **2D**
    - Data (HEX) - **00 A0 00 A0 00**
20. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
21. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.6.5.2.3 Slot 2 (HTU-C Slave)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

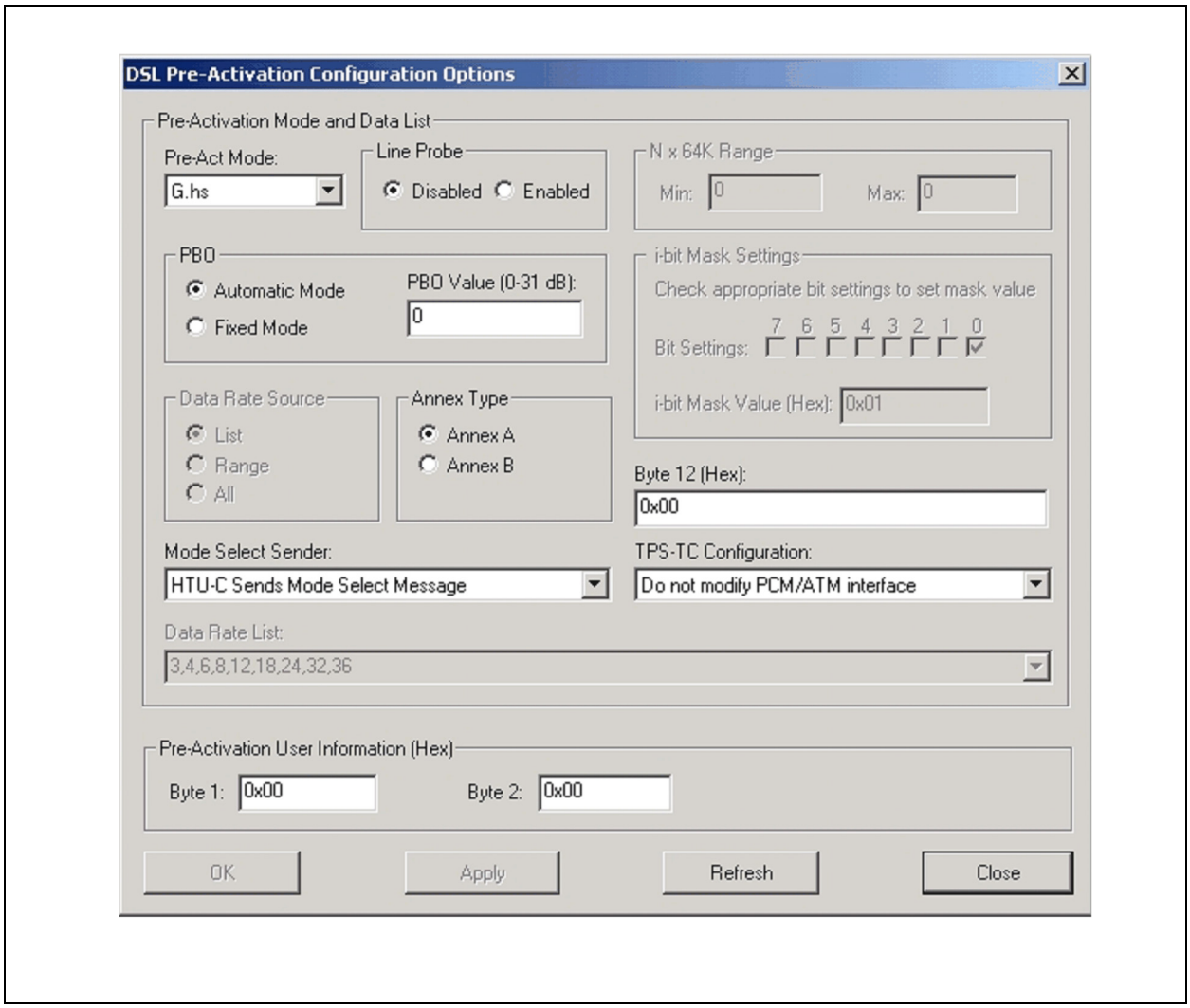
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **17**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **16**
- Starting NB Time Slot Location - **17**

Figure 3-80. TestExec Multi Rate Configuration for Slave



5. Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-81. TestExec Preactivation Configuration for Slave

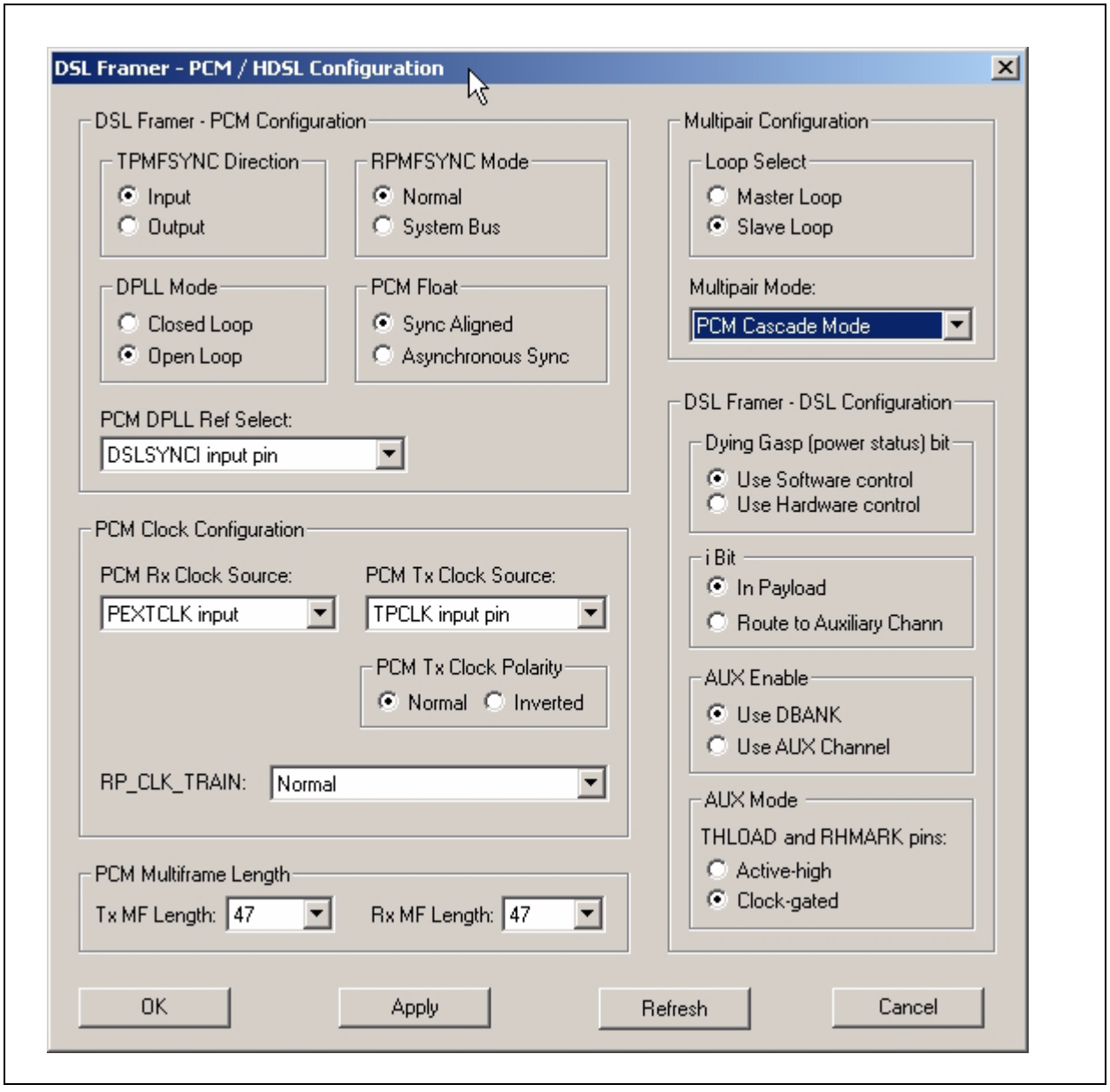


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **DSLSYNCI input pin**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PEXTCLK input**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**

- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Slave Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

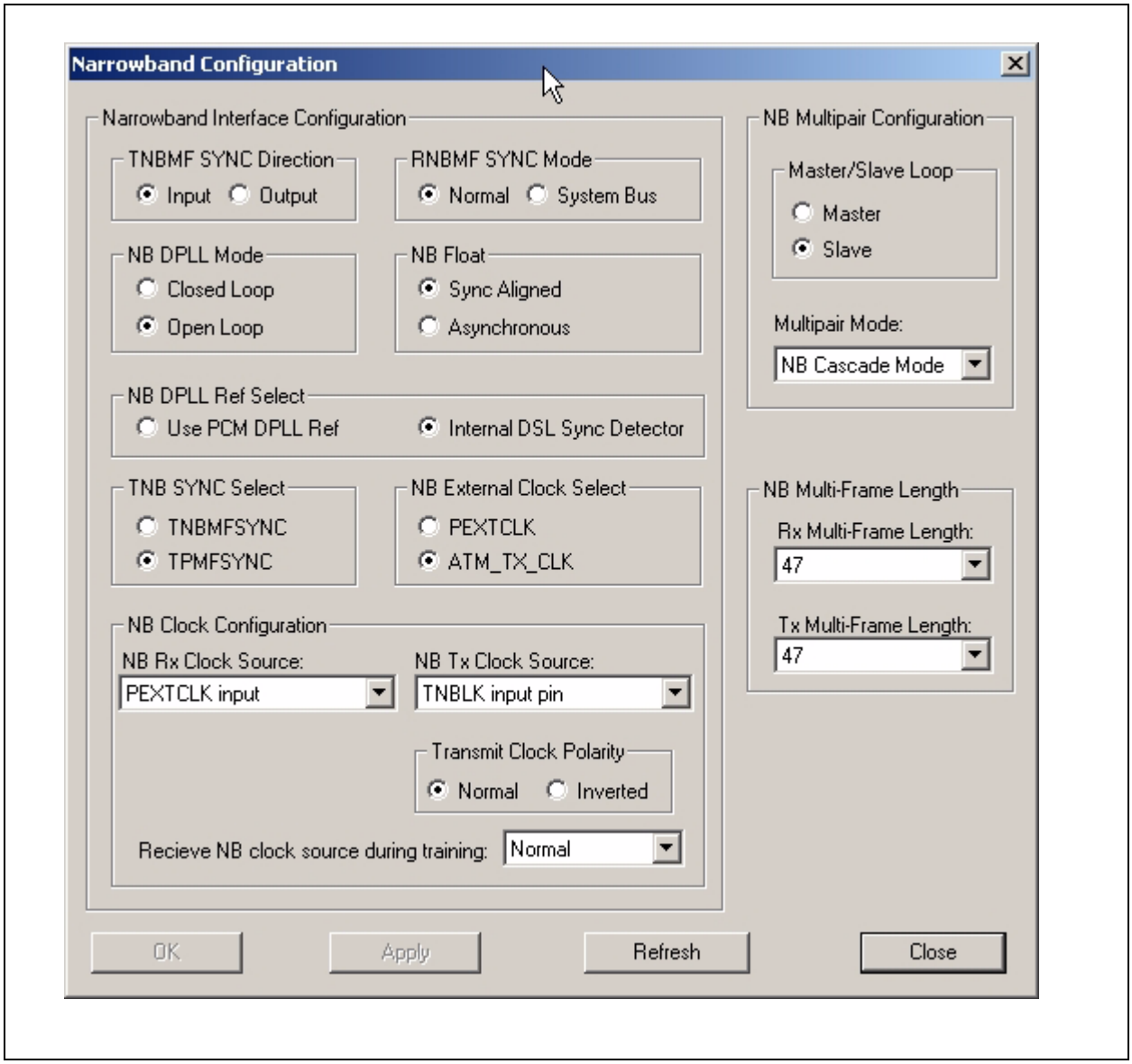
Figure 3-82. TextExec PCM/HDSL Configuration for Slave



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **Narrowband** Button.
13. Enter the following values:

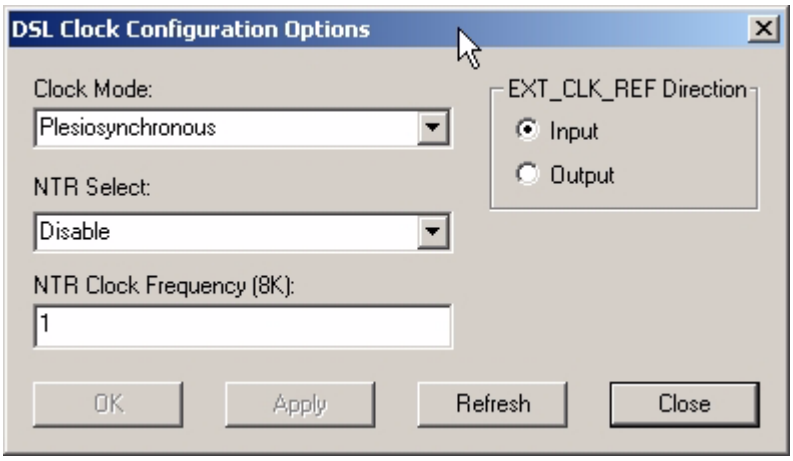
- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Open Loop**
  - NB Float - **Sync Aligned**
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Slave**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**

Figure 3-83. TextExec Narrowband Configuration for Slave



14. Click on **Apply** button and then click on the **Close** button.
15. Click on the **DSL Clock** Button.
16. Enter the following values:

Figure 3-84. TextExec DSL Clock Configuration for Slave

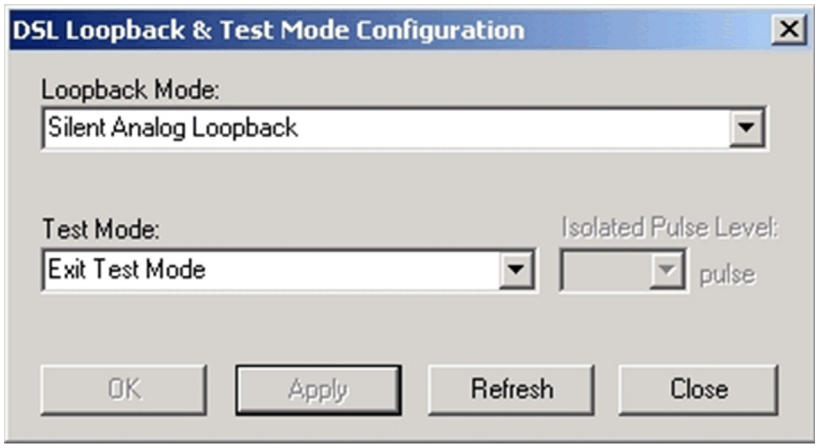


17. For setting the water level for the Narrowband Interface, Click on **Comm Spy** Tab.
18. Enter the following values
    - Opcode (HEX) - **2D**
    - Data (HEX) - **00 A0 00 A0 00**
19. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.6.5.2.4 Loopback

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Loopback/Test** button.
3. Set the **Loopback Mode** to **Silent Analog Loopback**.

Figure 3-85. Setting the ZipwirePlus Device into Loopback

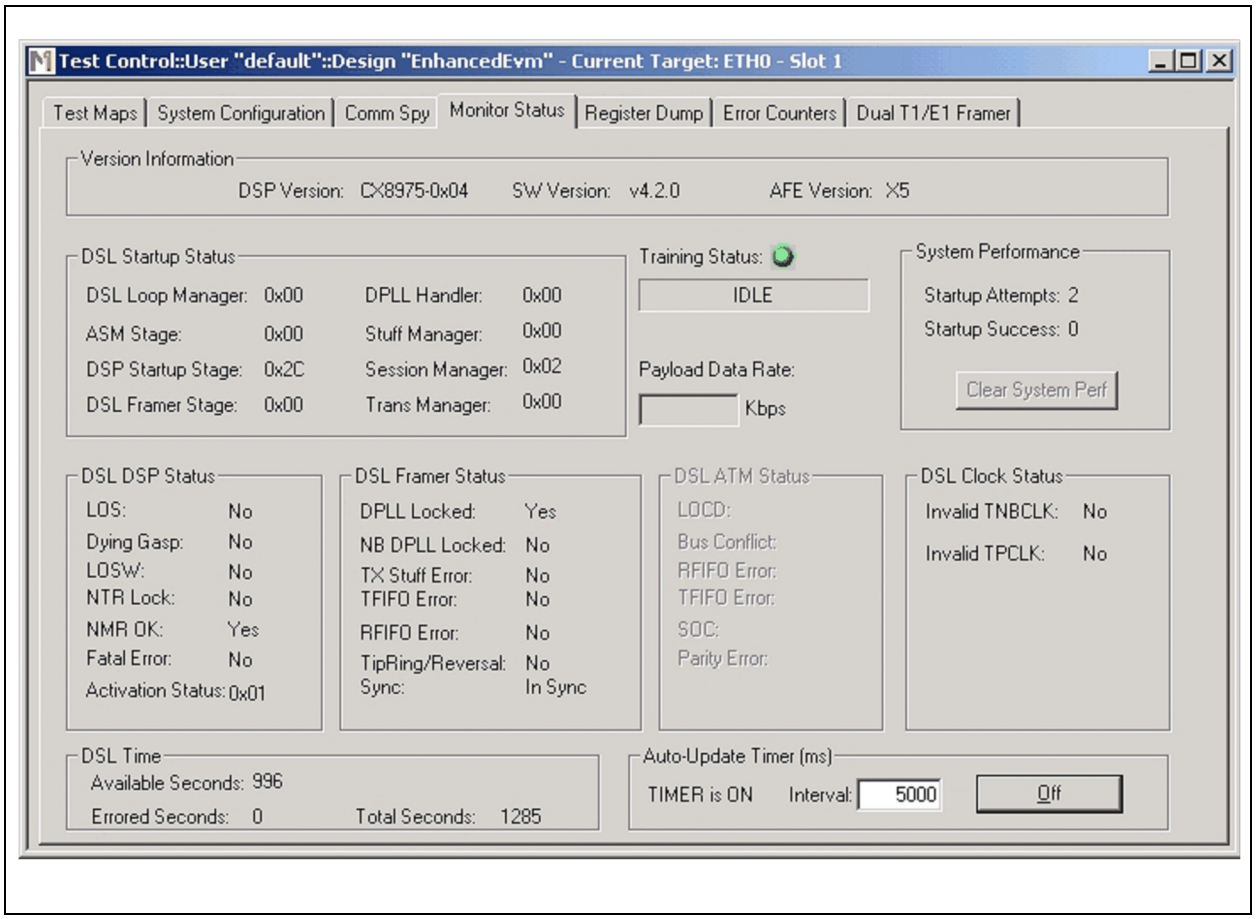


4. Click on the **Apply** button and then click on the Close button.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Click on the **Loopback/Test** button.
7. Set the **Loopback Mode** to **Silent Analog Loopback**. Click on the **Apply** button and then click on the **Close** button.

3.6.5.2.5 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the Set button in the **Auto Update Timer** box.
4. Verify that the Training Status is **GREEN** and showing **IDLE** State.

Figure 3-86. Monitoring the ZipWirePlus Device in Loopback



5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2.**
6. Repeat Steps 2 - 4.

3.6.5.2.6 FIFO Resets

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on Framer Reset button under Software Features.
3. Issue FIFO resets for the Master Loop in the following sequence.
   - Click on **TX_WL_RESET**
   - Click on **TX_FIFO_RESET**
   - Click on **RX_WL_RESET**
   - Click on **RX_FIFO_RESET**
4. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
5. Repeat Steps 2-3.
6. Verify the Fireberd #1 is in SYNC with no Bit Errors.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
8. For issing FIFO resets for the Narrowband Interface, Click on **Comm Spy** Tab.
9. Enter the following values
   - Opcode (HEX) - **75**
   - Data (HEX) - **01 50 00 05**

10. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
11. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 35**
12. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
13. Click on Framer Reset button under Software Features.
14. Issue FIFO resets for the Master Loop in the following sequence.
    - Click on **TNB_WL_RESET**
    - Click on **TNB_FIFO_RESET**
    - Click on **RNB_WL_RESET**
    - Click on **RNB_FIFO_RESET**
15. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
16. Repeat Steps 13-14.
17. Verify the Fireberd #2 is in SYNC with no Bit Errors or else repeat Steps 12 - 16.
18. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
19. Click on **Comm Spy** Tab.
20. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 04**
21. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
22. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 34**

3.6.6 End to End Testing Using Two Enhanced EVMs

For end to end testing, one additional Enhanced EVM is needed.

3.6.6.1 Enhanced EVM Setup

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-R and the ZipWirePlus LIC in Slot 2 as the Slave HTU-R. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. BNC Tester Card Connections - Make the following connections
    - TX1DAT to RX1DAT
    - TX1CLK to RX1CLK

7. Loopback externally the FRAMER_1 of the Dual T1/E1 card using the T1/E1 cable adapter.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
9. Set up for Zero Loop Length

   a) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Master Slot 1) to J7 of the ZipWirePlus LIC(HTU-R Master Slot 1) of this Enhanced EVM.

   b) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Slave Slot 2) to J7 of the ZipWirePlus LIC(HTU-R Slave Slot 2) of this Enhanced EVM.

3.6.6.2 TestExec

3.6.6.2.1 Installation and Configuration

Please refer to Section 3.2.5.1 for detailed procedure for installing the configuring the TestExec(UIP) software.

Assuming the same PC is being used to control both HTU-C & HTU-R, we will use the **EnhancedEvm2** design file for the HTU-R Enhanced EVM.

3.6.6.2.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup.
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

   c.**LegacyEvm**
5. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. Setup the Hardware Configuration as defined in Section 3.6.5.2.1.

3.6.6.2.3 Slot 1 (HTU-R Master)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Master card. Please refer to Section 3.6.5.2.2.

3.6.6.2.4 Slot 2 (HTU-R Slave)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.

3. The rest of the configuration is exactly the same as HTU-C Slave card. Please refer to Section 3.6.5.2.3.

3.6.6.2.5 Loop Activation

1. Go to the TestExec GUI for HTU-C EVM.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Now take the HTU-C Master out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
4. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Master ZipWirePlus device and it will start training.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Now take the HTU-C Slave out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
7. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Slave ZipWirePlus device and it will start training.
8. Go to the TestExec GUI for HTU-R EVM.
9. Change to slot 1 by right clicking the mouse button and selecting Slot 1.
10. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Master ZipWirePlus device and it will start training.
11. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Slave ZipWirePlus device and it will start training.

3.6.6.2.6 Monitor the Link

1. Go the HTU-C TestExec GUI.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Click on the **Monitor Status** tab.
4. Click the **Set** button in the **Auto Update Timer** box.
5. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State.
6. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
7. Repeat Steps 2 - 4.

3.6.6.2.7 FIFO Resets

1. Go to the TestExec GUI for HTU-C EVM.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
3. Click on **Framer Reset** button under Software Features.
4. Go to the TestExec GUI for HTU-R EVM
5. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
6. Click on **Framer Reset** button under Software Feature.
7. Issue FIFO resets for the Master Loop in the following sequence.
   - Click on **TX_WL_RESET** (HTU-C Master)

- Click on **TX_FIFO_RESET** (HTU-C Master)
- Click on **RX_WL_RESET** (HTU-R Master)
- Click on **RX_FIFO_RESET** (HTU-R Master)
- Click on **TX_WL_RESET** (HTU-R Master)
- Click on **TX_FIFO_RESET** (HTU-R Master)
- Click on **RX_WL_RESET** (HTU-C Master)
- Click on **RX_FIFO_RESET** (HTU-C Master)

8. Go to the TestExec GUI for HTU-C EVM.
9. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
10. Go to the TestExec GUI for HTU-R EVM.
11. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
12. Issue FIFO resets for the Slave Loop in the following sequence.
    - Click on **TX_WL_RESET** (HTU-C Slave)
    - Click on **TX_FIFO_RESET** (HTU-C Slave)
    - Click on **RX_WL_RESET** (HTU-R Slave)
    - Click on **RX_FIFO_RESET** (HTU-R Slave)
    - Click on **TX_WL_RESET** (HTU-R Slave)
    - Click on **TX_FIFO_RESET** (HTU-R Slave)
    - Click on **RX_WL_RESET** (HTU-C Slave)
    - Click on **RX_FIFO_RESET** (HTU-C Slave)
13. Verify the Fireberd #1 is in SYNC with no Bit Errors.
14. Go to the TestExec GUI for HTU-C EVM.Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
15. For issing FIFO resets for the Narrowband Interface, Click on **Comm Spy** Tab.
16. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 05**
17. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
18. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 35**
19. Go to the TestExec GUI for HTU-R EVM.Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
20. Repeats Steps 16-18.
21. Go to the TestExec GUI for HTU-C EVM.
22. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
23. Go to the TestExec GUI for HTU-R EVM.
24. Change to slot 1by right clicking the mouse button and selecting **Slot 1**
25. Issue FIFO resets for the Master Loop in the following sequence.
    - Click on **TNB_WL_RESET** (HTU-C Master)
    - Click on **TNB_FIFO_RESET** (HTU-C Master)
    - Click on **RNB_WL_RESET** (HTU-R Master)
    - Click on **RNB_FIFO_RESET** (HTU-R Master)
    - Click on **TNB_WL_RESET** (HTU-R Master)
    - Click on **TNB_FIFO_RESET** (HTU-R Master)
    - Click on **RNB_WL_RESET** (HTU-C Master)
    - Click on **RNB_FIFO_RESET** (HTU-C Master)
26. Go to the TestExec GUI for HTU-C EVM.
27. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**

28. Go to the TestExec GUI for HTU-R EVM.
29. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
30. Issue FIFO resets for the Slave Loop in the following sequence.
    - Click on **TNB_WL_RESET** (HTU-C Slave)
    - Click on **TNB_FIFO_RESET** (HTU-C Slave)
    - Click on **RNB_WL_RESET** (HTU-R Slave)
    - Click on **RNB_FIFO_RESET** (HTU-R Slave)
    - Click on **TNB_WL_RESET** (HTU-R Slave)
    - Click on **TNB_FIFO_RESET** (HTU-R Slave)
    - Click on **RNB_WL_RESET** (HTU-C Slave)
    - Click on **RNB_FIFO_RESET** (HTU-C Slave)
31. Verify the Fireberd #2 is in SYNC with no Bit Errors or else repeat Steps 20- 26.
32. Go to the TestExec GUI for HTU-C EVM.Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
33. Click on **Comm Spy** Tab.
34. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 04**
35. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
36. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 34**
37. Go to the TestExec GUI for HTU-R EVM.Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
38. Repeats Steps 24-27.
39. Verify the Fireberd #2 is in SYNC with no Bit Errors.

3.6.6.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-72. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.7 Enhanced EVM Setup for Single-pair E1 Transport utilizing M28947 integrated E1 Framer.

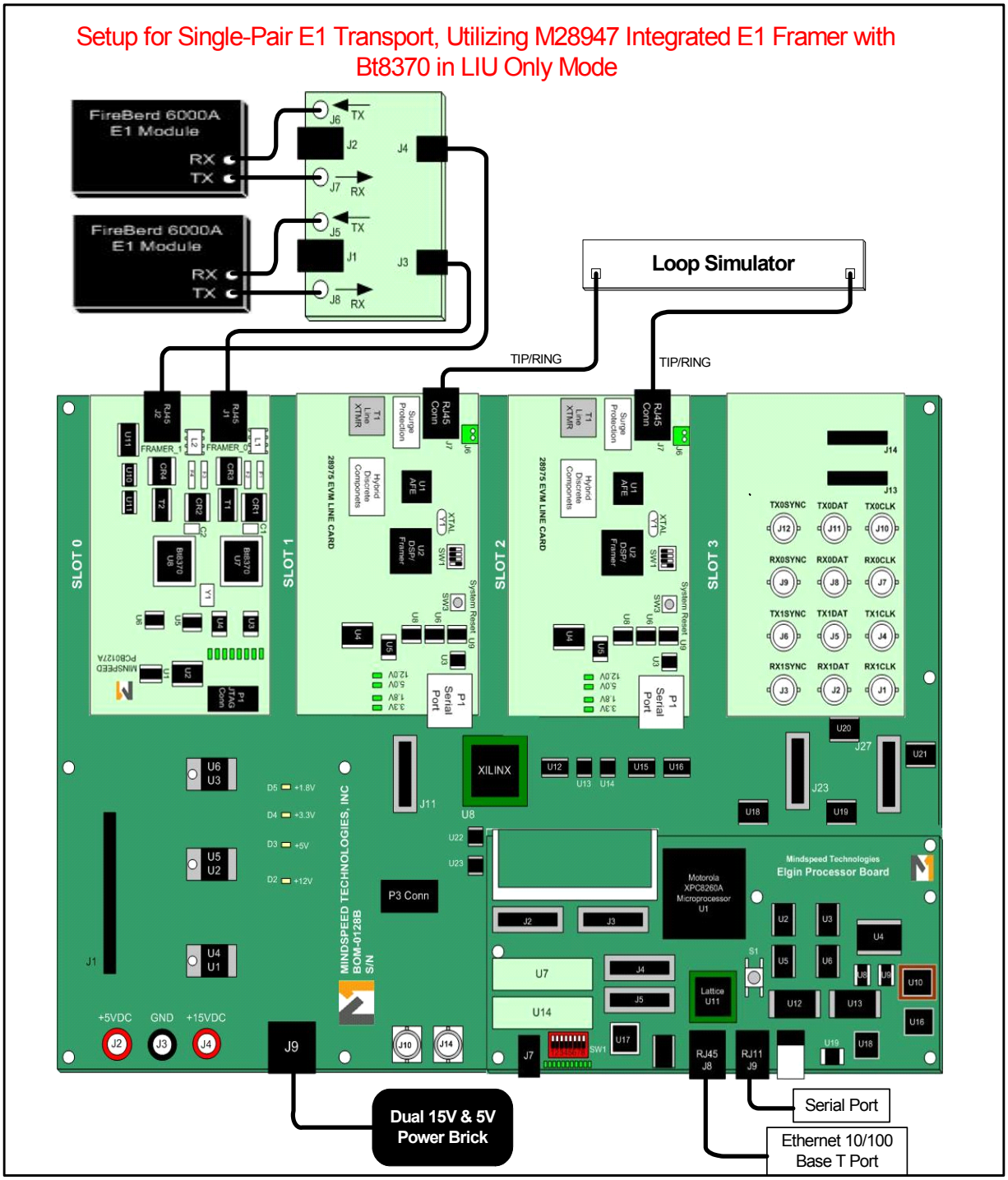
The following steps are required for running the ZipWirePlus Enhanced EVM for Single-Pair E1 Transport using the M28947 Integrated (Internal) E1 Framer Application. This setup needs one enhanced EVM.

This configuration is valid for M28947 device only.

The Hardware setup for this application is shown in Figure 3-87.

NOTE: The Fireberd must be equipped with a 2M/ nX64 interface (E1 Module) to proceed with the setup described in this section. Figure 3-87 illustrates the required interconnections.

Figure 3-87. Enhanced EVM Setup - Single-Pair E1 Transport using M28947 Integrated E1 Framer



3.7.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. .
6. Fireberd Connections -
   - Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-C card.
   - Fireberd #2 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_1 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-R card..
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.7.2 Fireberd Setup

Configure the Fireberd #1 E1 Module front panel as follows:

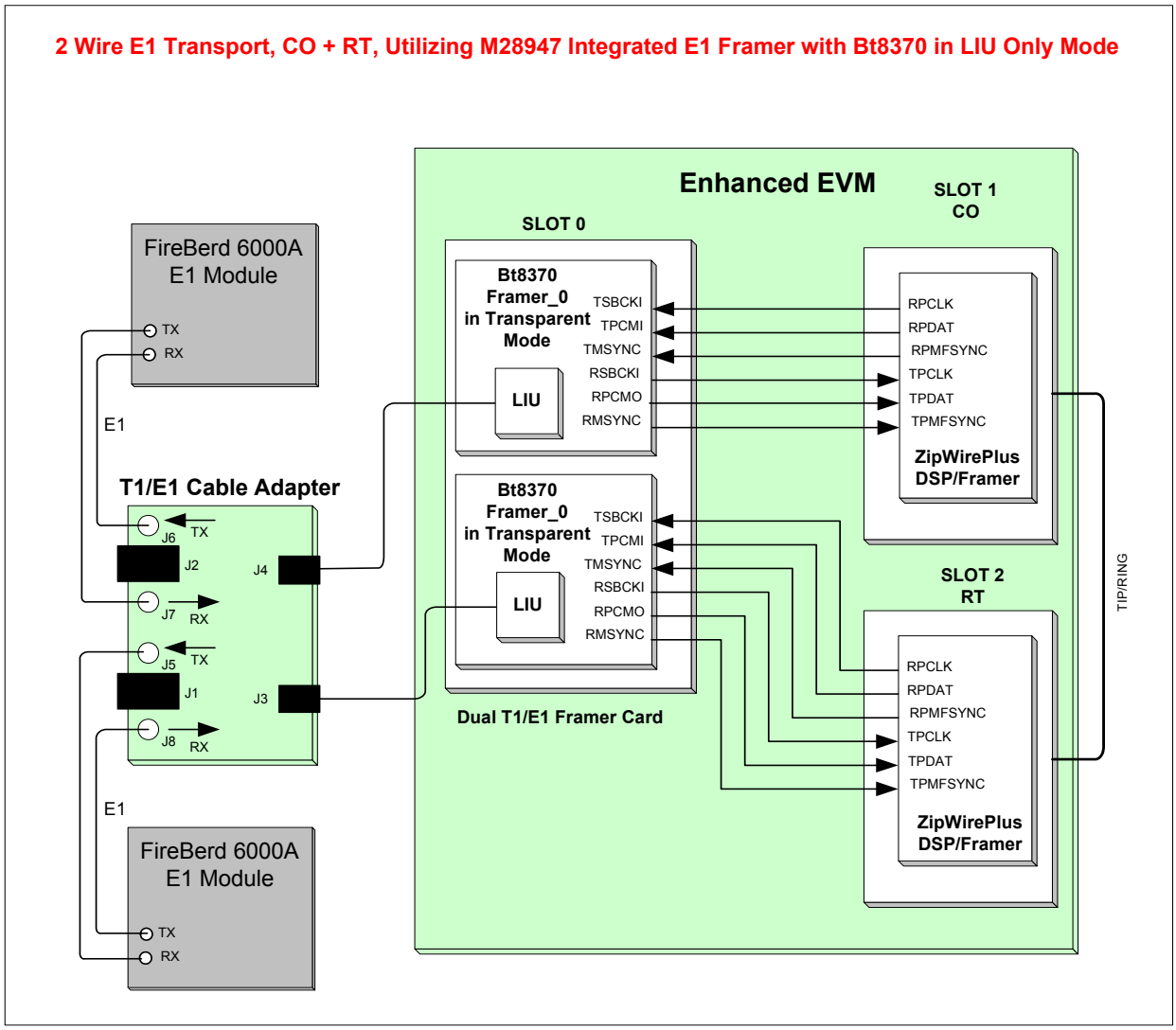
- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kHz
- INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
- INTF SETUP: 2M/n64: MODE: FULL2M
- Configure the Fireberd #2 E1 Module front panel the same way as above.

3.7.3 FPGA Configuration

The Host Code configures FPGA(U8) into one of the many possible configurations through the TestExec (UIP) GUI.

This configuration will connect the PCM bus of the ZipWirePlus device (slot 1) to the Framer #0 (slot 0) and the PCM bus of the ZipWirePlus device (slot 2) to the Framer #1 (slot 0). Please note the Framers will be in LIU only mode. Figure 3-87 explains the pin interconnections for this application.

Figure 3-88. Connections for Single-Pair E1 Transport using M28947 Integrated E1 Framer



3.7.4 Enhanced EVM Configuration

3.7.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28947 which supports internal E1 Framer (E1 PRA).

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.7.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.7.5 TestExec

3.7.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the EnhancedEvm design file for the Enhanced EVM.

3.7.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

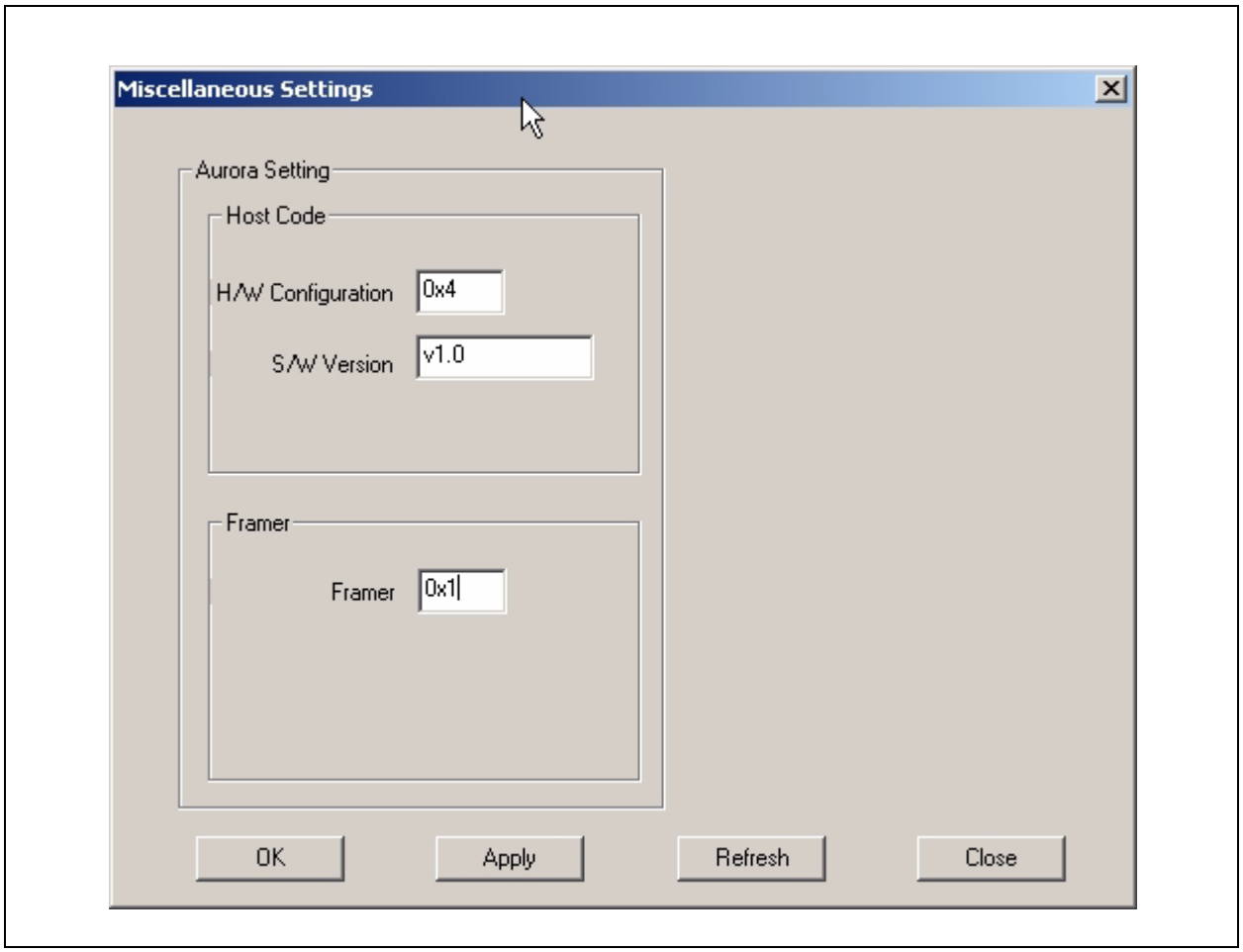
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**

3.7.5.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x4.
3. Enter the **Framer** value to be 0x1.This configures the T1/E1 Framer for the E1 LIU ONLY Mode.

Figure 3-89. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

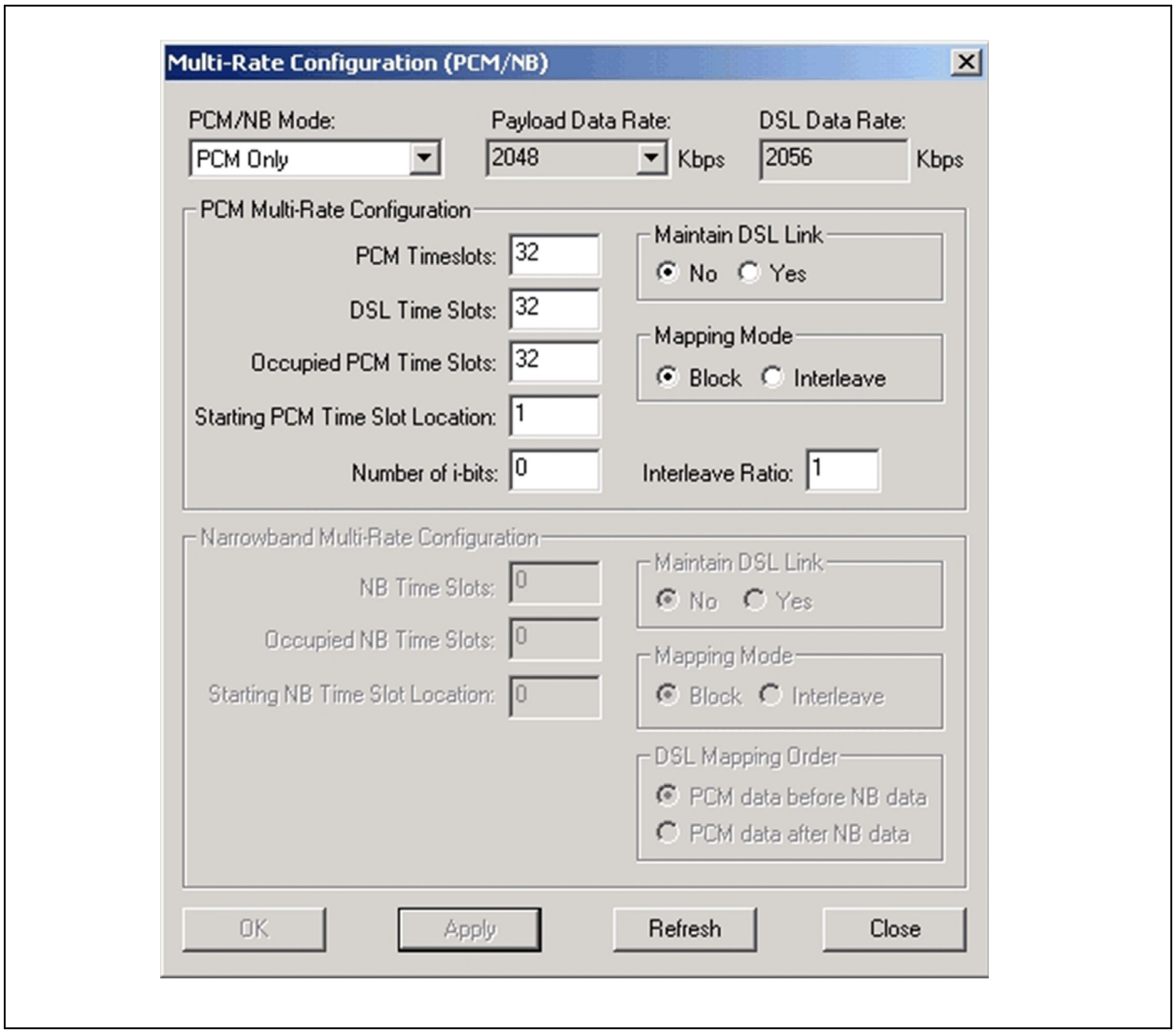


3.7.5.2.2 Slot 1 (HTU-C Side)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the Values:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

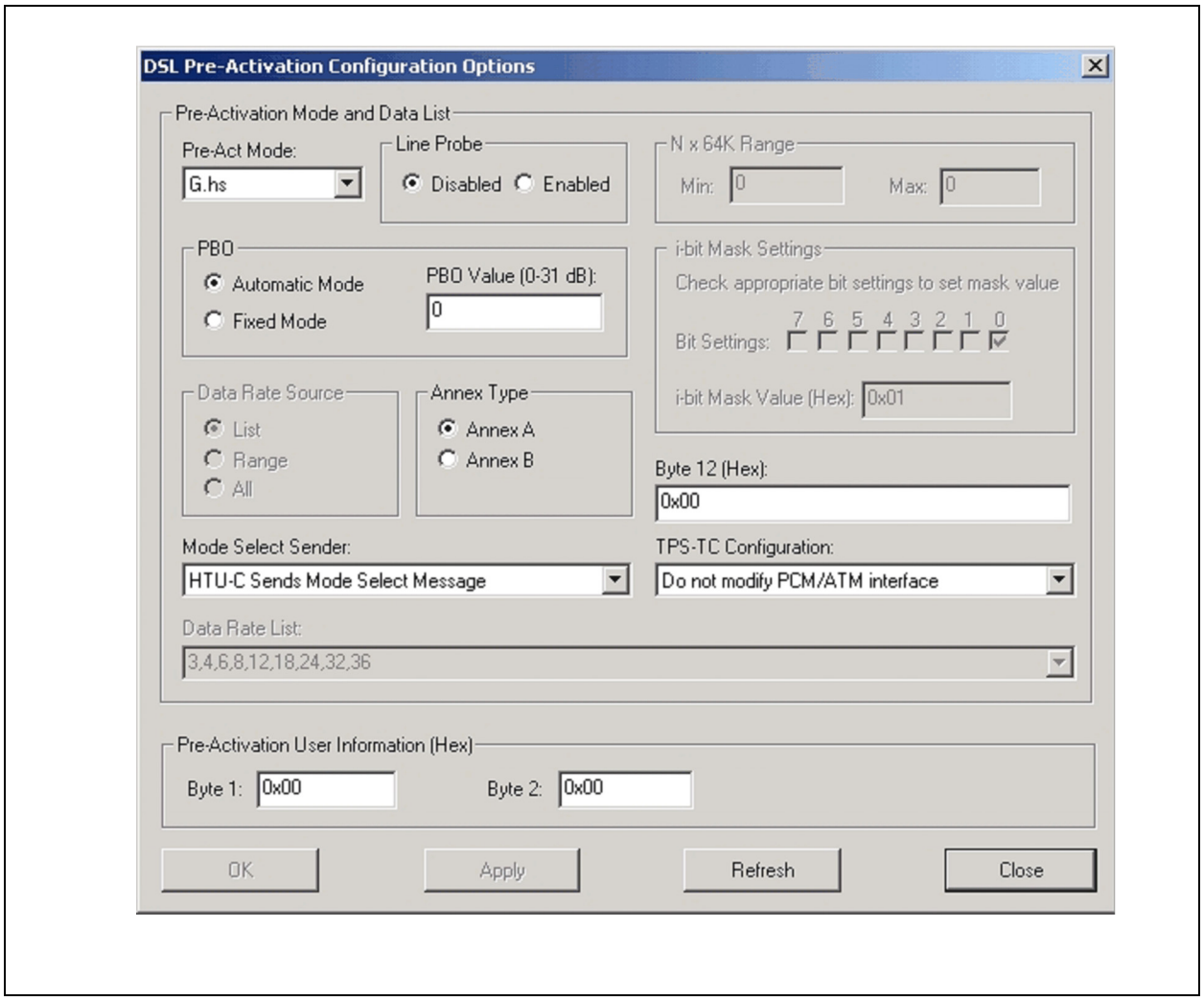
Figure 3-90. TestExec Multi-Rate Configuration for CO



Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.

5. Click on the **Pre-Activation** button.

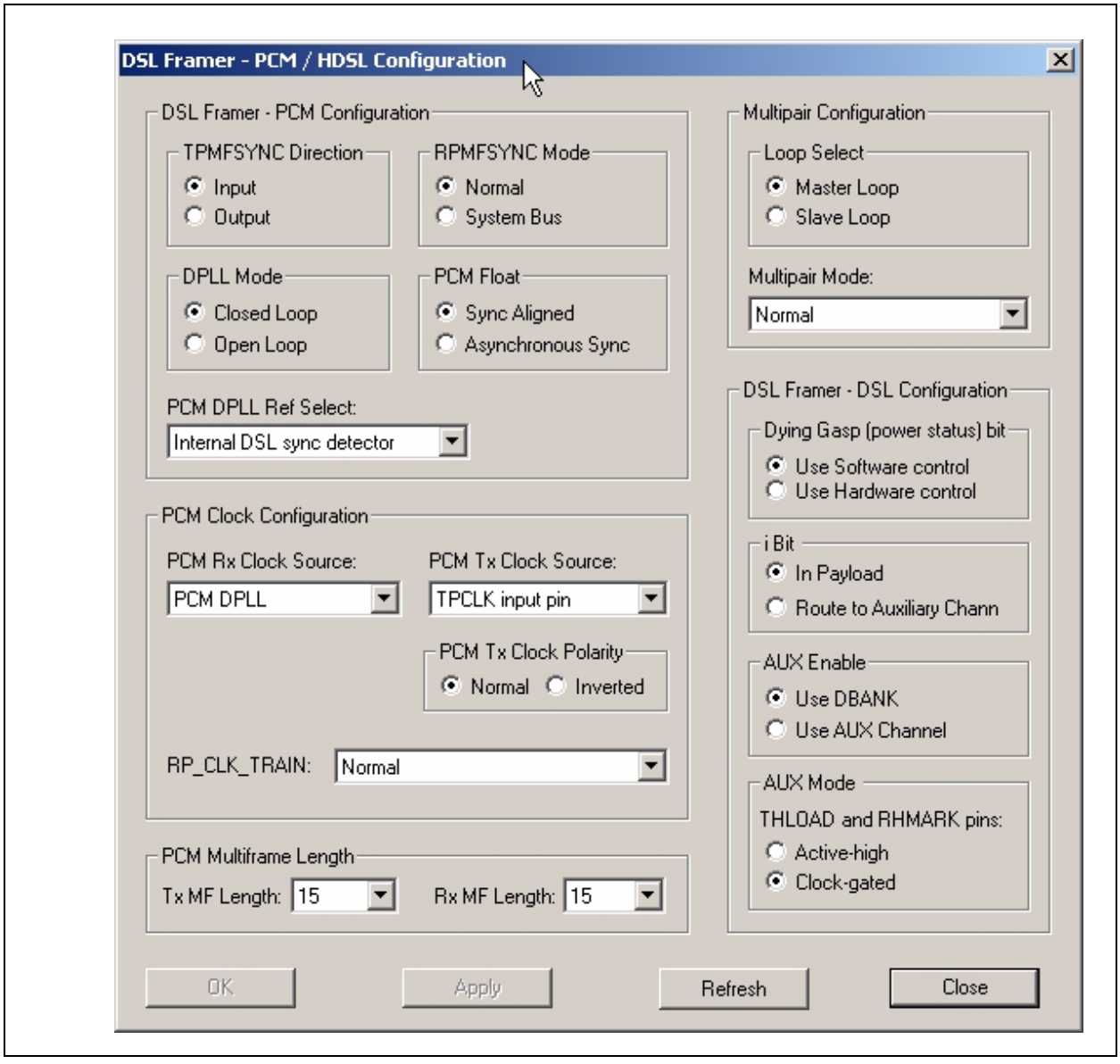
Figure 3-91. TestExec Preactivation Configuration for CO



6. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
7. Click on the **Apply** button and then click on the **Close** button.
8. Click on the **PCM/HDSL** button. Enter the following values:
   - DSL framer - PCM Configuration
     - TPMFSYNC Direction - **Input**
     - RPMFSYNC Mode - **Normal**
     - DPLL Mode - **Closed Loop**
     - PCM Float - **Sync Aligned**
     - PCM DPLL Ref Select - **Internal DSL Sync Detector**
   - PCM Clock Configuration
     - PCM Rx Clock Source - **PCM DPLL**
     - PCM Tx Clock Source - **TPCLK Input**
     - PCM Tx Clock Polarity - **Normal**
     - RP_CLK_TRAIN - **Normal**
   - PCM Multiframe Length

  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

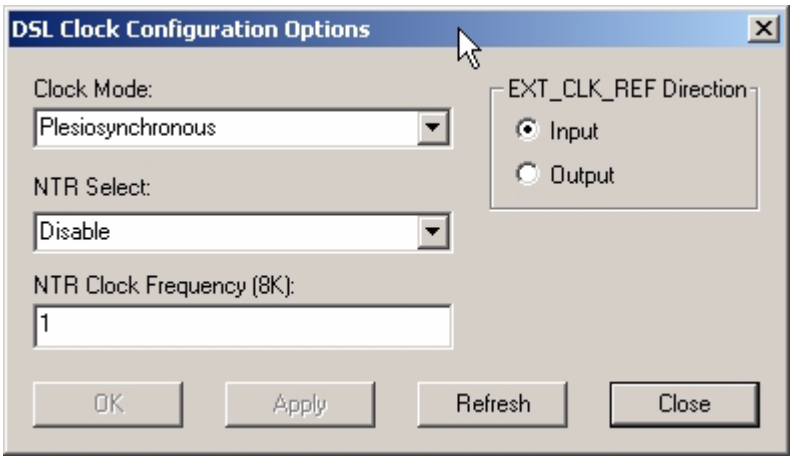
Figure 3-92. TestExec PCM/HDSL Configuration for CO



9. Click on the **Apply** button and then click on the **Close** button.

10. Click on the **DSL Clock** Button.
11. Enter the following values:

Figure 3-93. TextExec DSL Clock Configuration for CO



12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
13. Click on **Comm Spy** Tab.
14. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

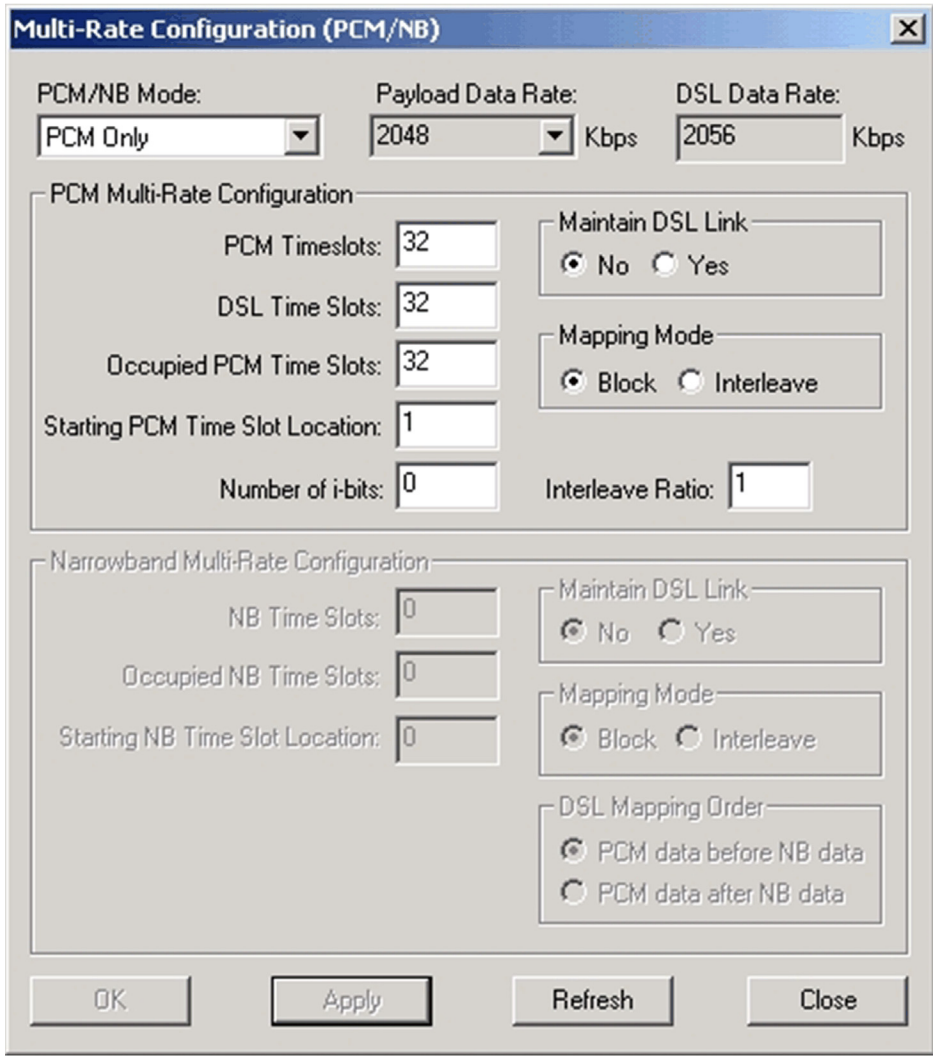
15. Change to Slot 2 by right clicking the mouse button and selecting **Slot 2.**

3.7.5.2.3 Slot 2 (HTU-R Side)

1. Click on the **System Configuration** tab.
2. Set the **Terminal Type** to **HTU-R**.
3. Set the **System State** to **In-Service**.
4. Click on **Multi-Rate Button**.
5. Enter the values:

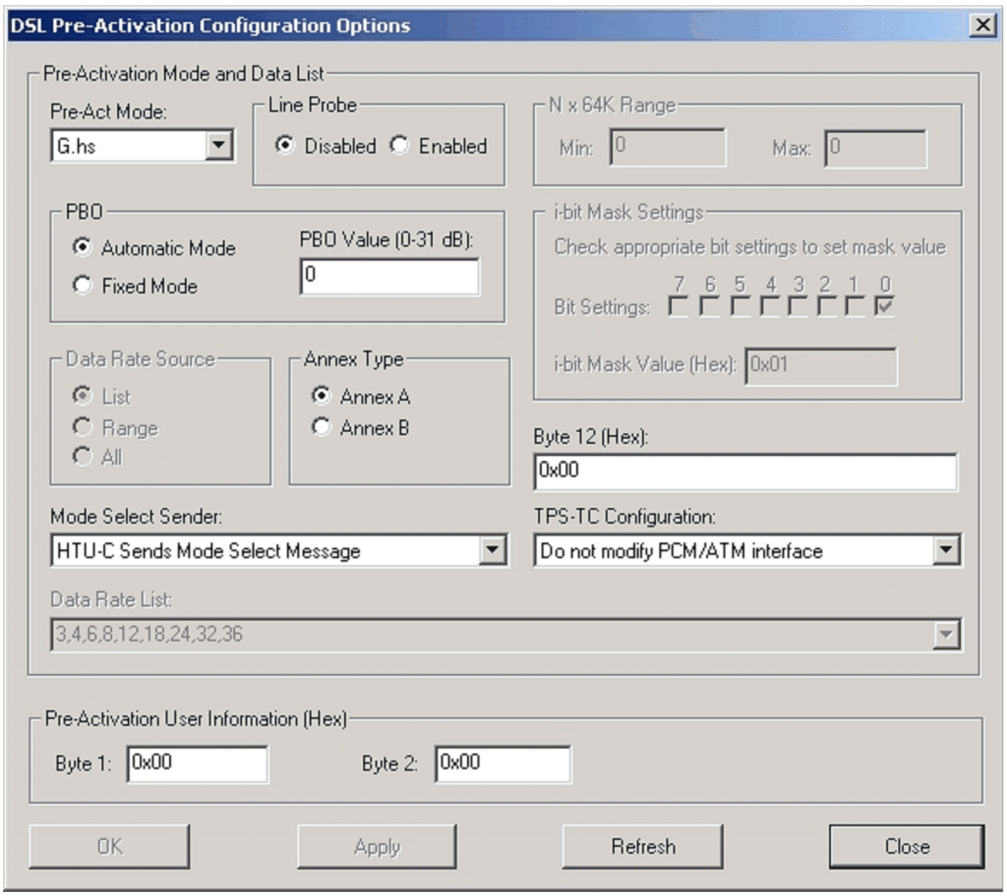
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-94. TestExec Multi Rate Configuration for RT



6. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

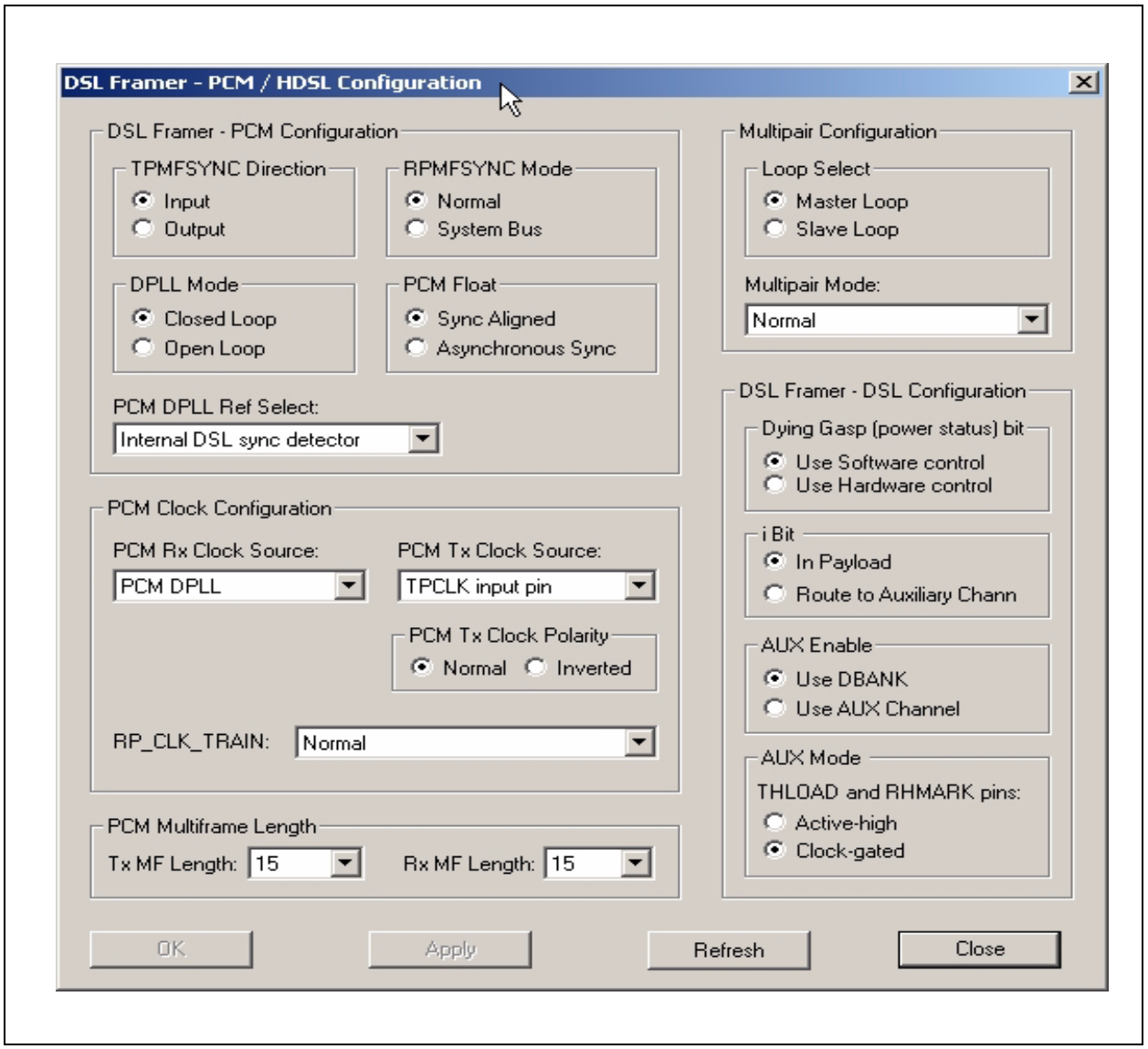
Figure 3-95. TestExec Preactivation Configuration for RT



8. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      - TPMFSYNC Direction - **Input**
      - RPMFSYNC Mode - **Normal**
      - DPLL Mode - **Closed Loop**
      - PCM Float - **Sync Aligned**
      - PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      - PCM Rx Clock Source - **PCM DPLL**
      - PCM Tx Clock Source - **TPCLK Input**
      - PCM Tx Clock Polarity - **Normal**
      - RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length
      - Tx MF Length - **15**

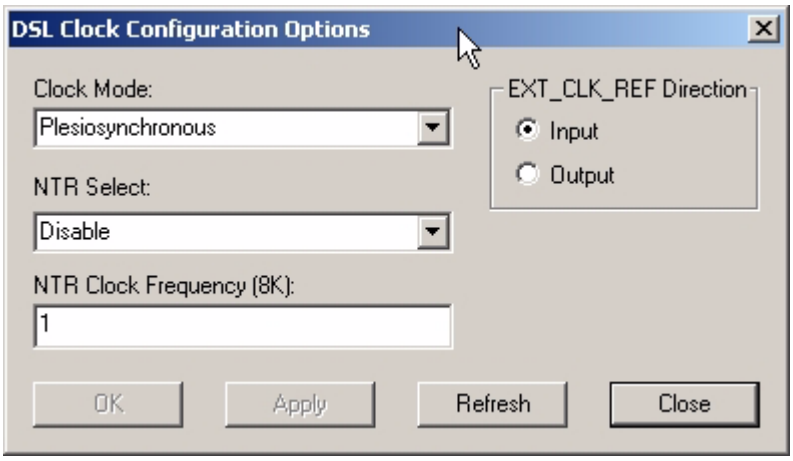
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gate**

Figure 3-96. TestExec PCM/HDSL Configuration for RT



11. Click the **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-97. TextExec DSL Clock Configuration for RT



14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
15. Click on **Comm Spy** Tab.
16. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

3.7.5.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.

3.7.5.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-87. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.8 Enhanced EVM Setup for Multi-pair E1 Transport utilizing M28947 Integrated E1 Framer

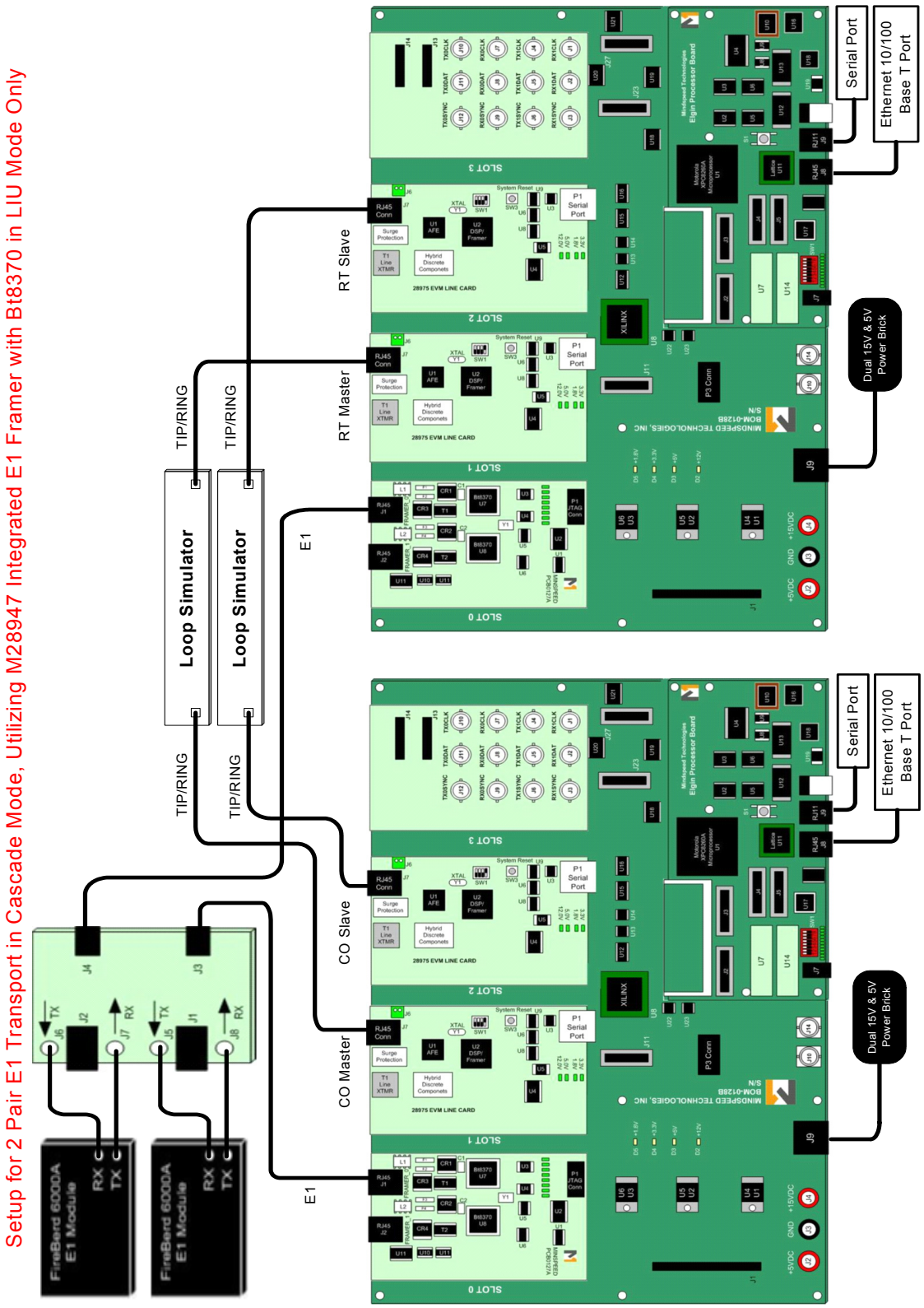
The following steps are required for running the ZipWirePlus Enhanced EVM for Multi-Pair E1 Transport application using the M28947 as the Integrated E1 Framer.. This setup needs two enhanced EVMs.

First, we shall use only the HTU-C EVM and put the DSL side is put into loopback. Then we shall perform end to end testing with two enhanced EVMs. The Hardware setup for this application is shown in Figure 3-98.

This application can be run only on the M28947 devices.

NOTE: The Fireberd must be equipped with a 2M/ nX64 interface (E1 Module) to proceed with the setup described in this section. Figure 3-98 illustrates the required interconnections.

Figure 3-98. Enhanced EVM Setup for Two-Pair E1 Transport Application using the M28947 integrated E1 Framer



3.8.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -
7. Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-C Master and HTU-C Slave cards.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.8.2 Fireberd Setup

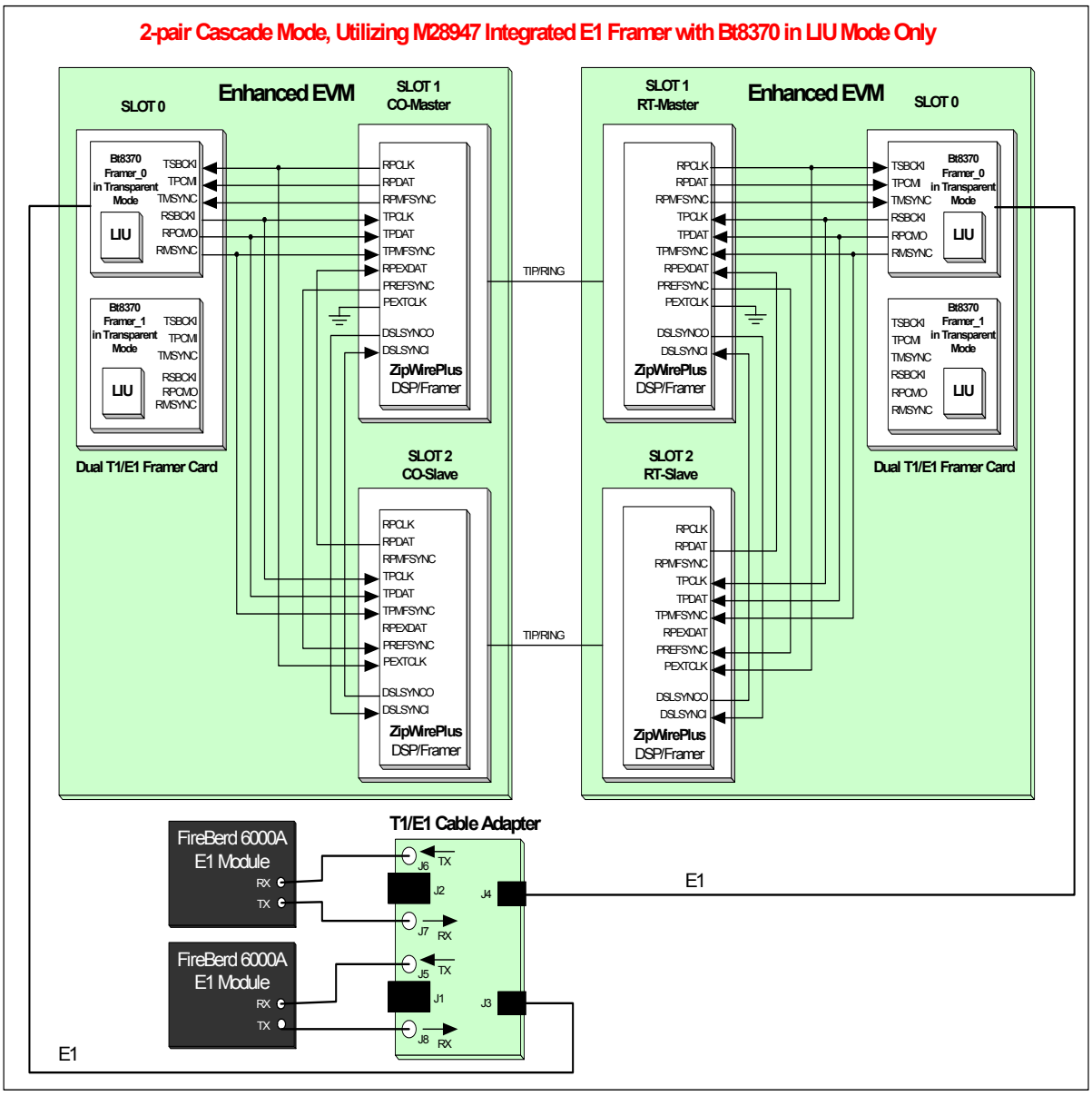
Configure the Fireberd #1 E1 Module front panel as follows:

- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kHz
- INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
- INTF SETUP: 2M/n64: MODE: FULL2M

3.8.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Framer #0 (slot 0). The Figure 3-99 explains the pin interconnections for this application.

Figure 3-99. Connections for Two-Pair E1 Transport Application using the M28947 integrated E1 Framer



3.8.4 Enhanced EVM Configuration

3.8.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- ZipWirePlus firmware image for M28947 which support Internal E1 Framer (E1 PRA).

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.8.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.8.5 TestExec

3.8.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software.

We will use the EnhancedEvm design file for the HTU-C Enhanced EVM.

3.8.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

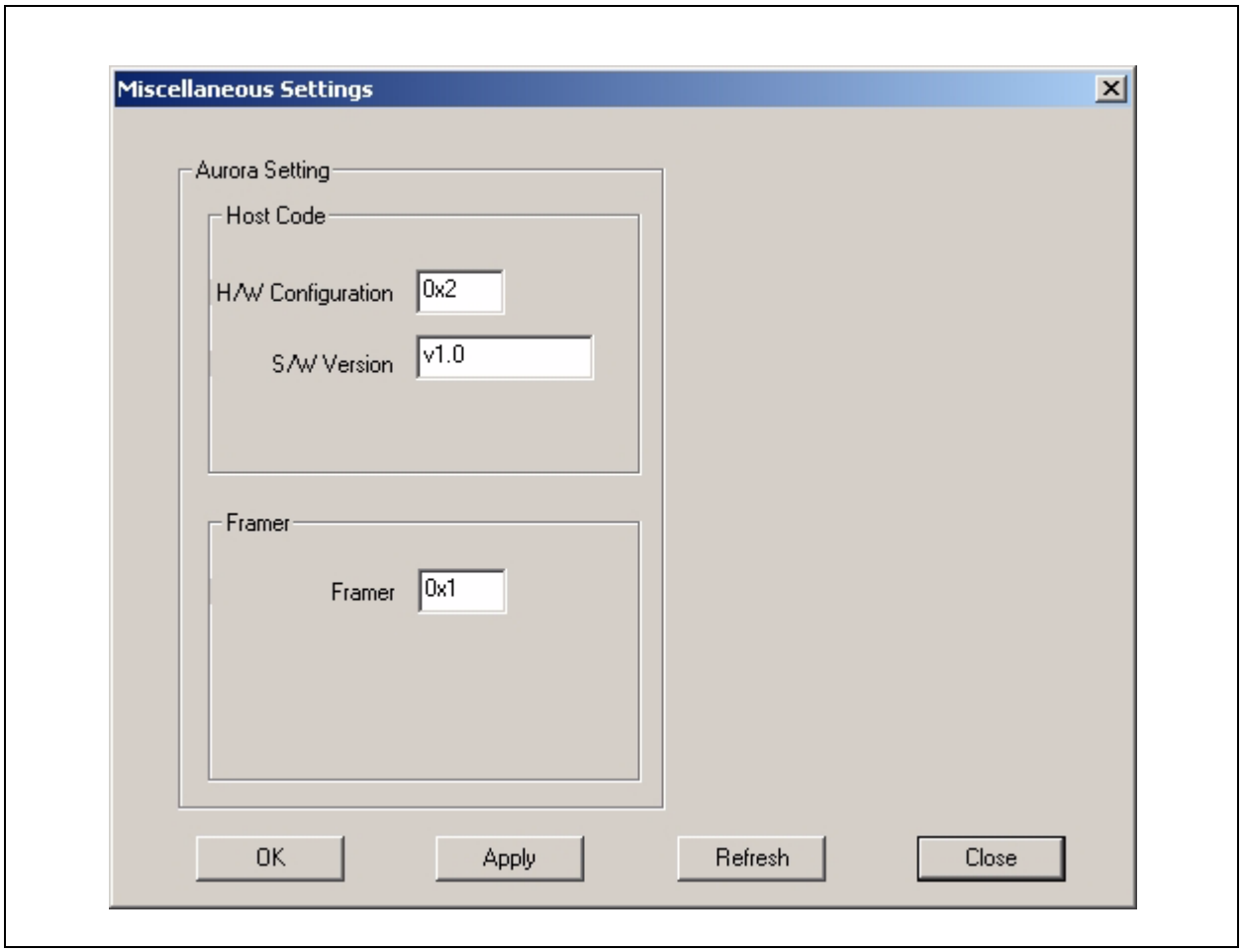
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file. Please note that for the HTU-C (CO) side EVM please select **EnhancedEvm** design file. For HTU-R (RT) side EVM please select the **EnhancedEvm2** design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Select **Slot 1**.

3.8.5.2.1 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0x2.
4. Enter the **Framer** value to be 0x1.This configures the T1/E1 Framer for the E1 LIU ONLY Mode

Figure 3-100. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

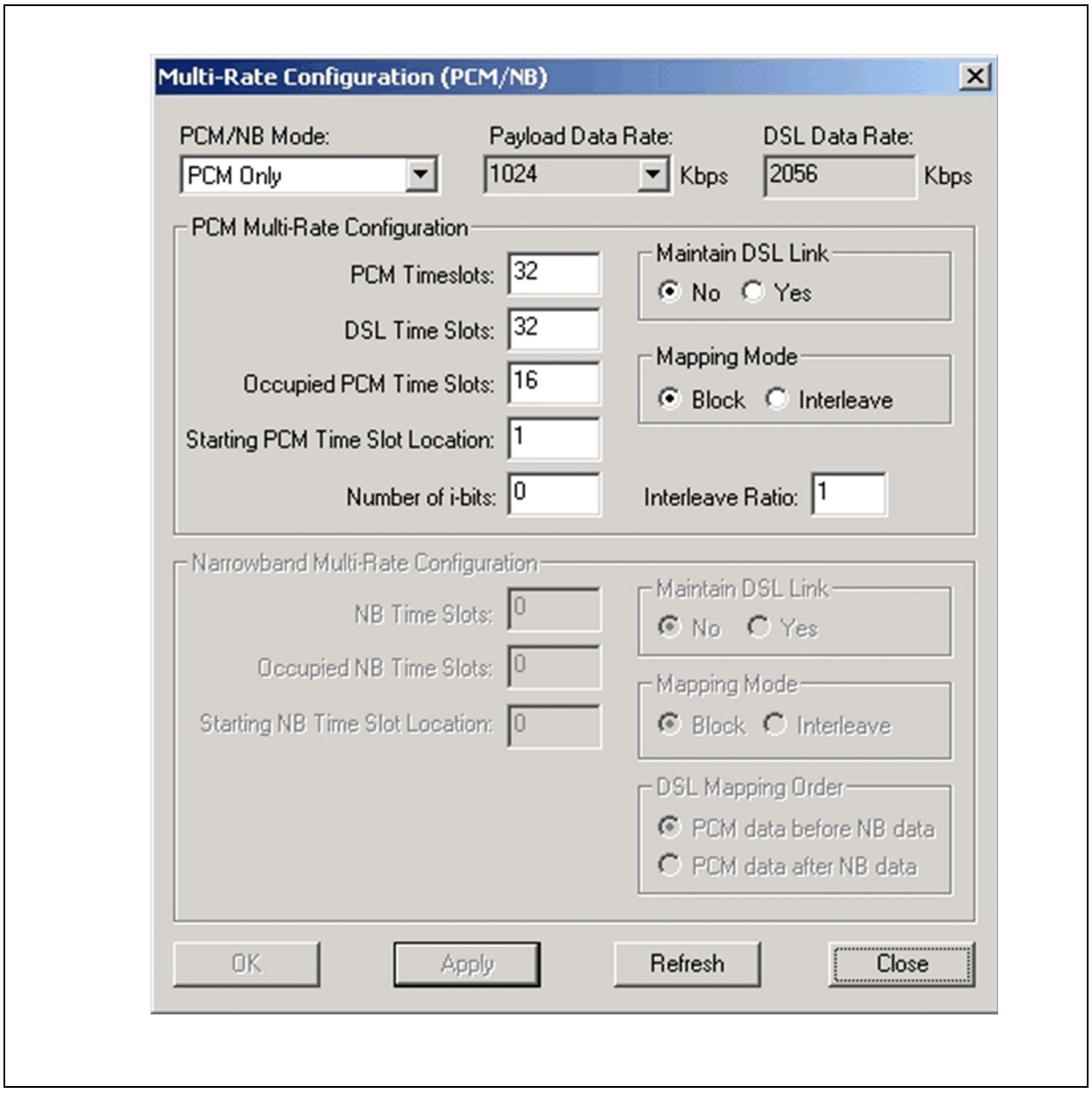


3.8.5.2.2 Slot 1 (HTU-C Master)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

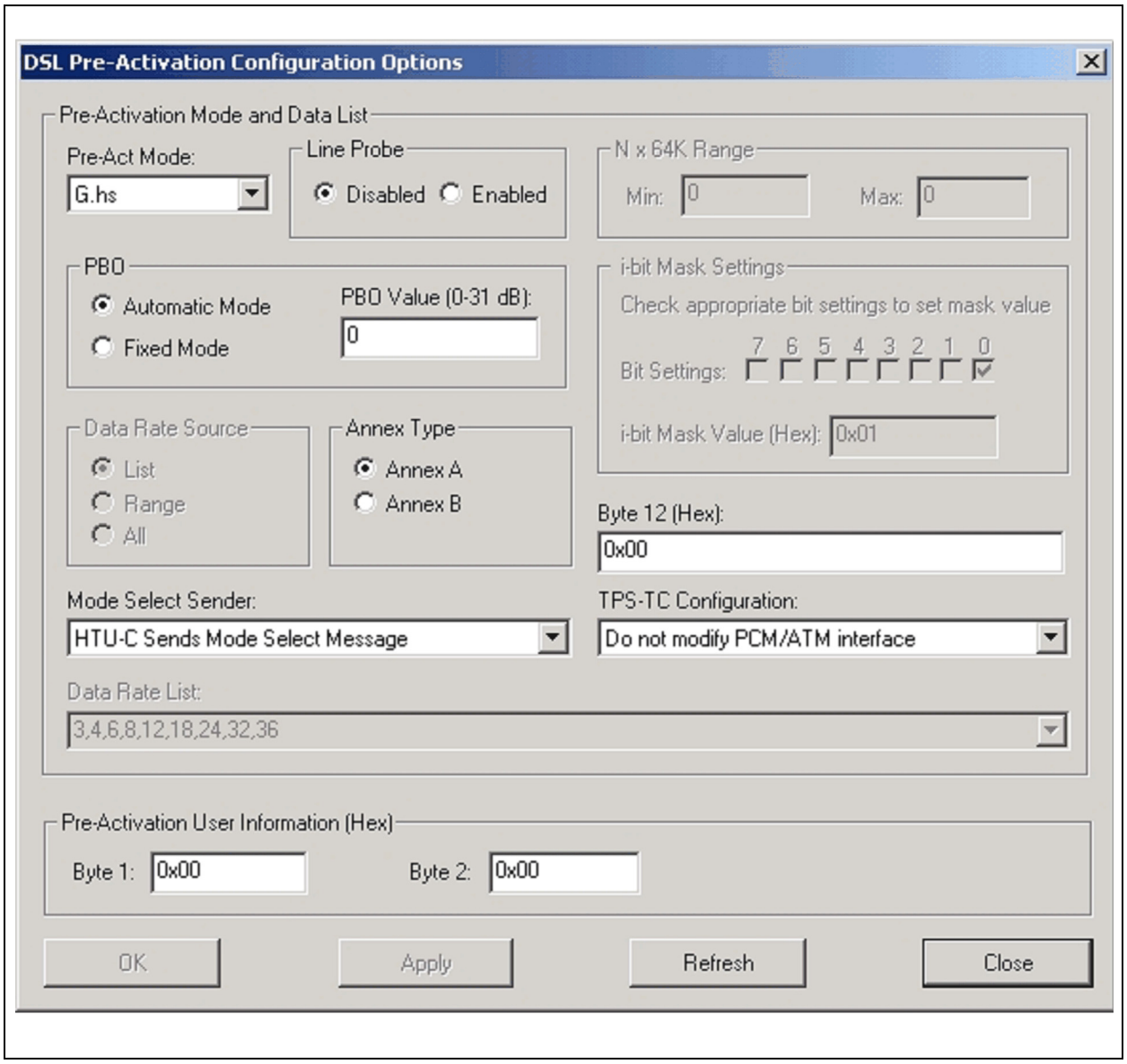
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-101. TestExec Multi-Rate Configuration for Master



5. Click the **Apply** button. The **Payload Data Rate** will change to 1024 Kbps and the **DSL Data Rate** will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-102. TestExec Preactivation Configuration for Master

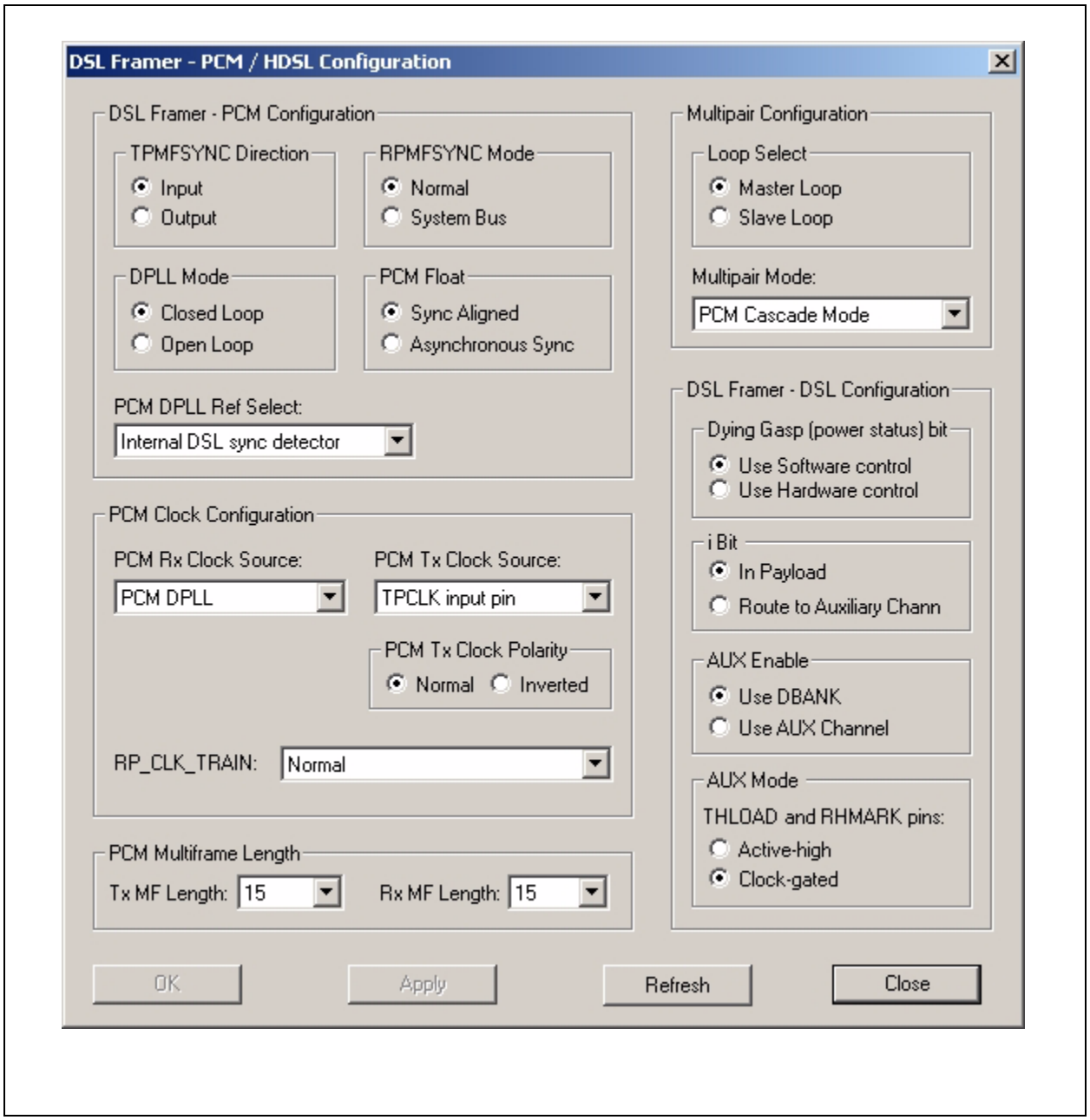


7. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration

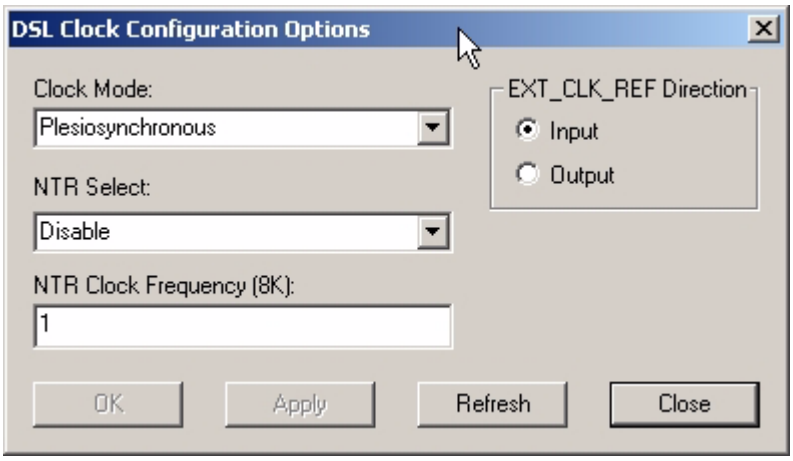
  - PCM Rx Clock Source - **PCM DPLL**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-103. TextExec PCM/HDSL Configuration for Master



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-104. TextExec DSL Clock Configuration for Master



14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
15. Click on **Comm Spy** Tab.
16. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

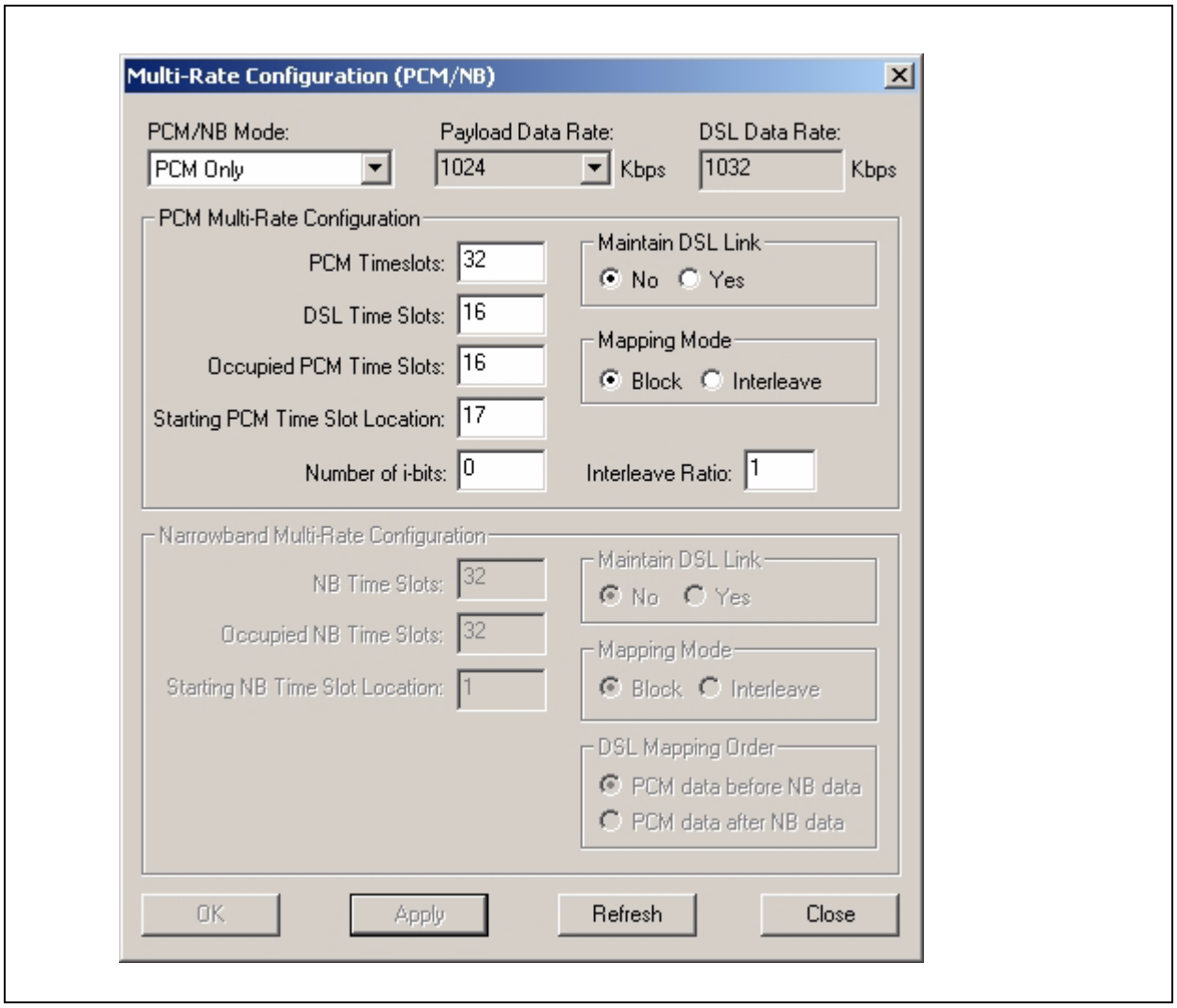
The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

17. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.8.5.2.3 Slot 2 (HTU-C Slave)

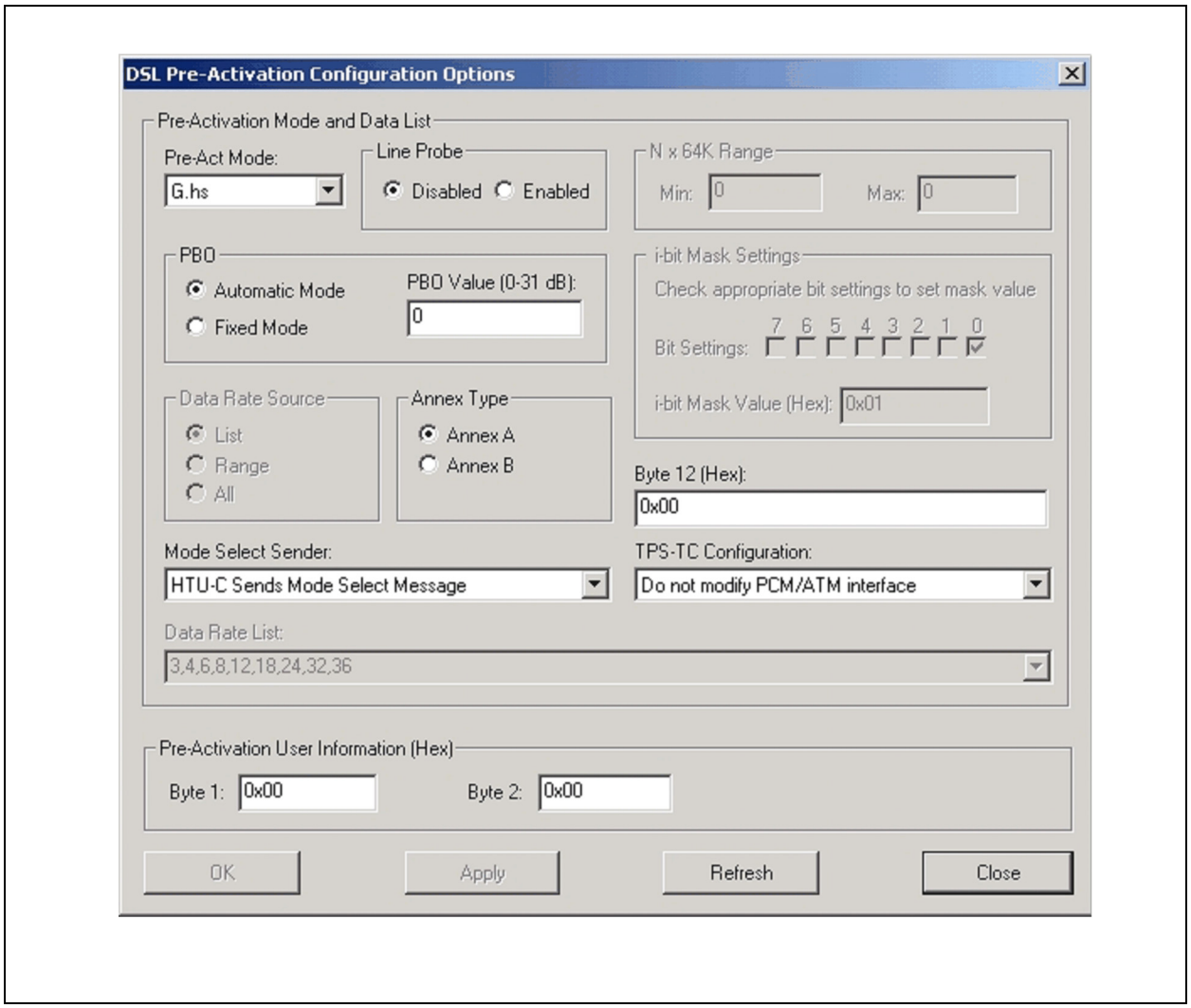
1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:
   - PCM/NB Mode - **PCM Only**
   - PCM Timeslots - **32**
   - DSL Time Slots - **32**
   - Occupied Time Slots - **16**
   - Starting PCM Time Slot Location - **17**
   - Number of i-bits - **0**

Figure 3-105. TestExec Multi Rate Configuration for Slave



5. Click the **Apply** button. The Payload Data Rate will change to 1024 Kbps and the DSL Data Rate will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-106. TestExec Preactivation Configuration for Slave

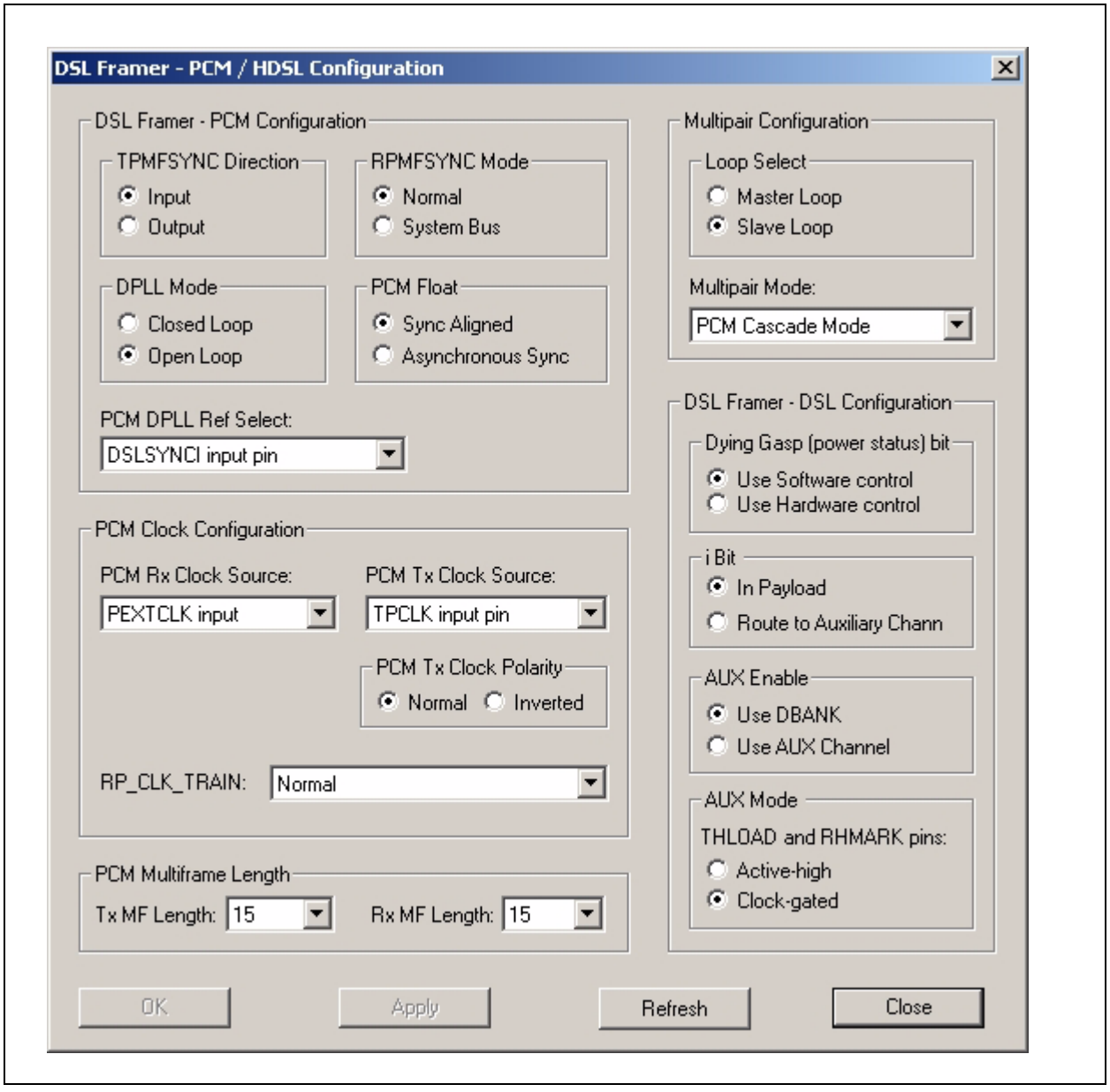


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **DSLSYNCI input pin**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PEXTCLK input**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**

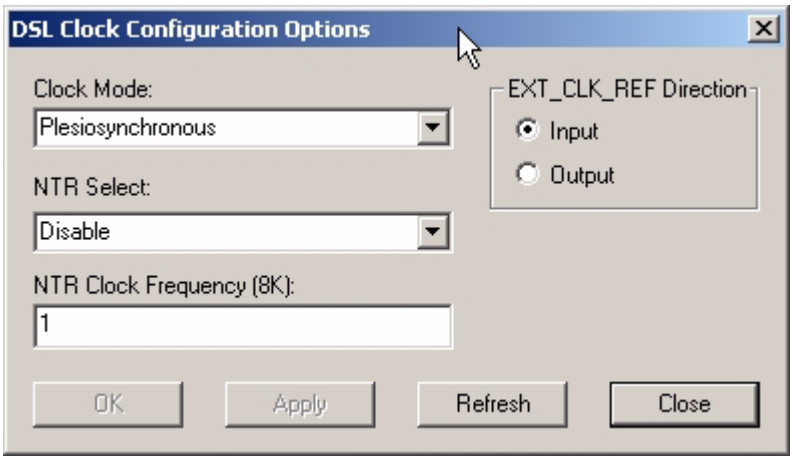
- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Slave Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-107. TextExec PCM/HDSL Configuration for Slave



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-108. TextExec DSL Clock Configurationfro Slave



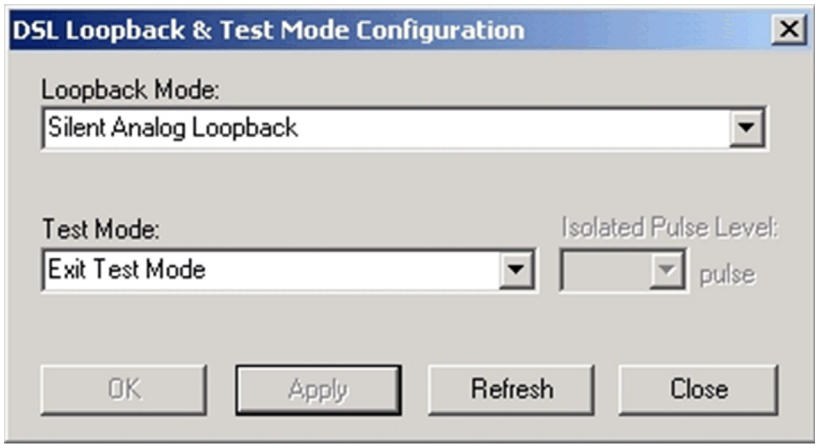
14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
15. Click on **Comm Spy** Tab.
16. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

3.8.5.2.4 Loopback

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Loopback/Test** button.
3. Set the **Loopback Mode** to **Silent Analog Loopback**.

Figure 3-109. Setting the ZipwirePlus Device into Loopback



4. Click on the **Apply** button and then click on the Close button.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Click on the **Loopback/Test** button.
7. Set the **Loopback Mode** to **Silent Analog Loopback**. Click on the **Apply** button and then click on the **Close** button.

3.8.5.2.5 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the Set button in the **Auto Update Timer** box.
4. Verify that the Training Status is **GREEN** and showing **IDLE** State.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2.**
6. Repeat Steps 2 - 4.
7. Verify the Fireberd is in SYNC with no Bit Errors.

3.8.6 End to End Testing Using Two Enhanced EVMs

For end to end testing, one additional Enhanced EVM is needed.

3.8.6.1 Enhanced EVM Setup

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-R) and Slot 2(Slave HTU-R) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings

should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.

4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-R and the ZipWirePlus LIC in Slot 2 as the Slave HTU-R. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -

   Fireberd #2 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter. This port shall feed PCM data into the HTU-R Master and HTU-R Slave cards.
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
8. Set up for Zero Loop Length

   a) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Master Slot 1) to J7 of the ZipWirePlus LIC(HTU-R Master Slot 1) of this Enhanced EVM.

   b) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Slave Slot 2) to J7 of the ZipWirePlus LIC(HTU-R Slave Slot 2) of this Enhanced EVM.

3.8.6.2 Fireberd #2 Setup

Configure the Fireberd as defined in Section 3.8.2

3.8.6.3 TestExec

3.8.6.3.1 Installation and Configuration

Please refer to Section 3.2.5.1 for detailed procedure for installing the configuring the TestExec(UIP) software.

Assuming the same PC is being used to control both HTU-C & HTU-R, we will use the **EnhancedEvm2** design file for the HTU-R Enhanced EVM.

3.8.6.3.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup and displays the following screen.
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

   c.**LegacyEvm**
5. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
6. Click on the **System Configuration** Tab.

7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. Select **Slot 1**i.e. Dual T1/E1 Framer card.

3.8.6.3.3 Slot 1 (HTU-R Master)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Master card. Please refer to Section 3.8.5.2.2.

3.8.6.3.4 Slot 2 (HTU-R Slave)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Slave card. Please refer to Section 3.8.5.2.3.

3.8.6.3.5 Loop Activation

1. Go to the TestExec GUI for HTU-C EVM.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Now take the HTU-C Master out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
4. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Master ZipWirePlus device and it will start training.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Now take the HTU-C Slave out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
7. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Slave ZipWirePlus device and it will start training.
8. Go to the TestExec GUI for HTU-R EVM.
9. Change to slot 1 by right clicking the mouse button and selecting Slot 1.
10. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Master ZipWirePlus device and it will start training.
11. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Slave ZipWirePlus device and it will start training.

3.8.6.3.6 Monitor the Link

1. Go the HTU-C TestExec GUI.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Click on the **Monitor Status** tab.
4. Click the **Set** button in the **Auto Update Timer** box.

5. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State.
6. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
7. Repeat Steps 2 - 4.
8. Verify the Fireberds are in SYNC with no Bit Errors.

3.8.6.4 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-98. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.9 Enhanced EVM Setup for Single-pair E1 Transport (using M28947 integrated Framer) and Unframed Narrowband Operation

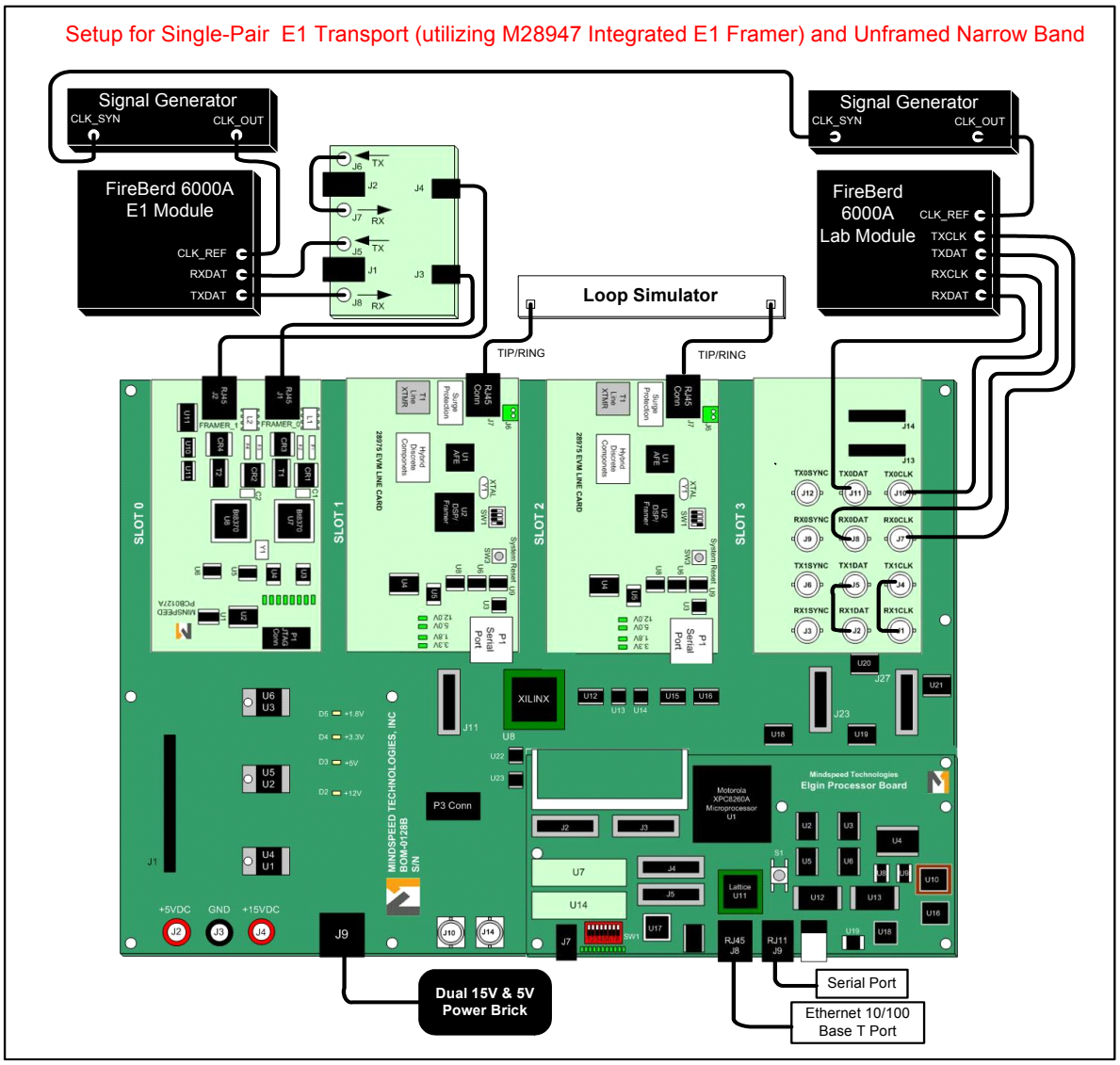
The following steps are required for running the ZipWirePlus Enhanced EVM in Single-Pair E1 Transport (using M28947 Integrated Framer) and Unframed Narrowband Operation. This setup needs one enhanced EVM.

This configuration is valid for M28947 device only.

The Hardware setup for this application is shown in Figure 3-110.

NOTE: This setup needs two(2) fireberds (one with 2M/nX64, one with Lab Interface Adapter). Please note that the Fireberds should have the same clock source. Two function generators have been used for that. Figure 3-110 illustrates the required interconnections.

Figure 3-110. Enhanced EVM Setup Single-Pair E1 Transport (using M28947 Integrated Framer) and Unframed Narrowband Operation



3.9.1 Enhanced EVM Setup

The setup procedure is defined in Section 3.5.1.

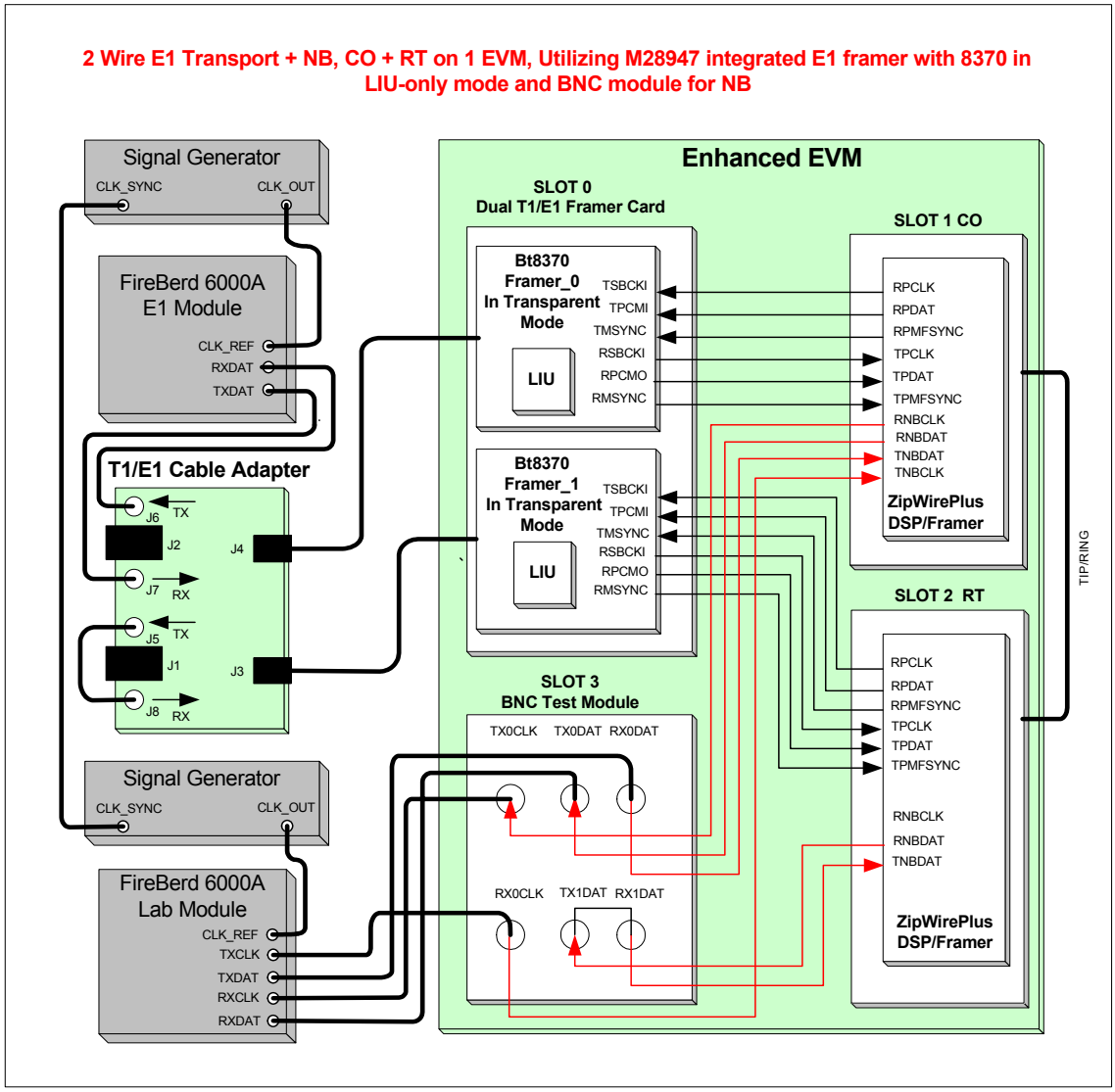
3.9.2 Fireberd Setup

The setup procedure is defined in Section 3.5.2.

3.9.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - HTU-C) to the Framer #0 (slot 0) and the Narrowband bus of ZipWirePlus device (HTU-C) to the Port 0 of the BNC Tester Card (Slot 3). Likewise on the RT side, it will connect the PCM bus of ZipWirePlus device (slot 2- HTU-R) to the Framer #1 (slot 0) and the Narrowband bus of ZipWirePlus device (HTU-R) to the Port 1of the BNC Tester Card (Slot 3). The Figure 3-112 explains the pin interconnections for this application.

Figure 3-111. Connections for Single-Pair E1 Transport (using M28947 Integrated Framer) and Unframed Narrowband Application



3.9.4 Enhanced EVM Configuration

3.9.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28947.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.9.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.9.5 TestExec

3.9.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the EnhancedEvm design file for the HTU-C Enhanced EVM.

3.9.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

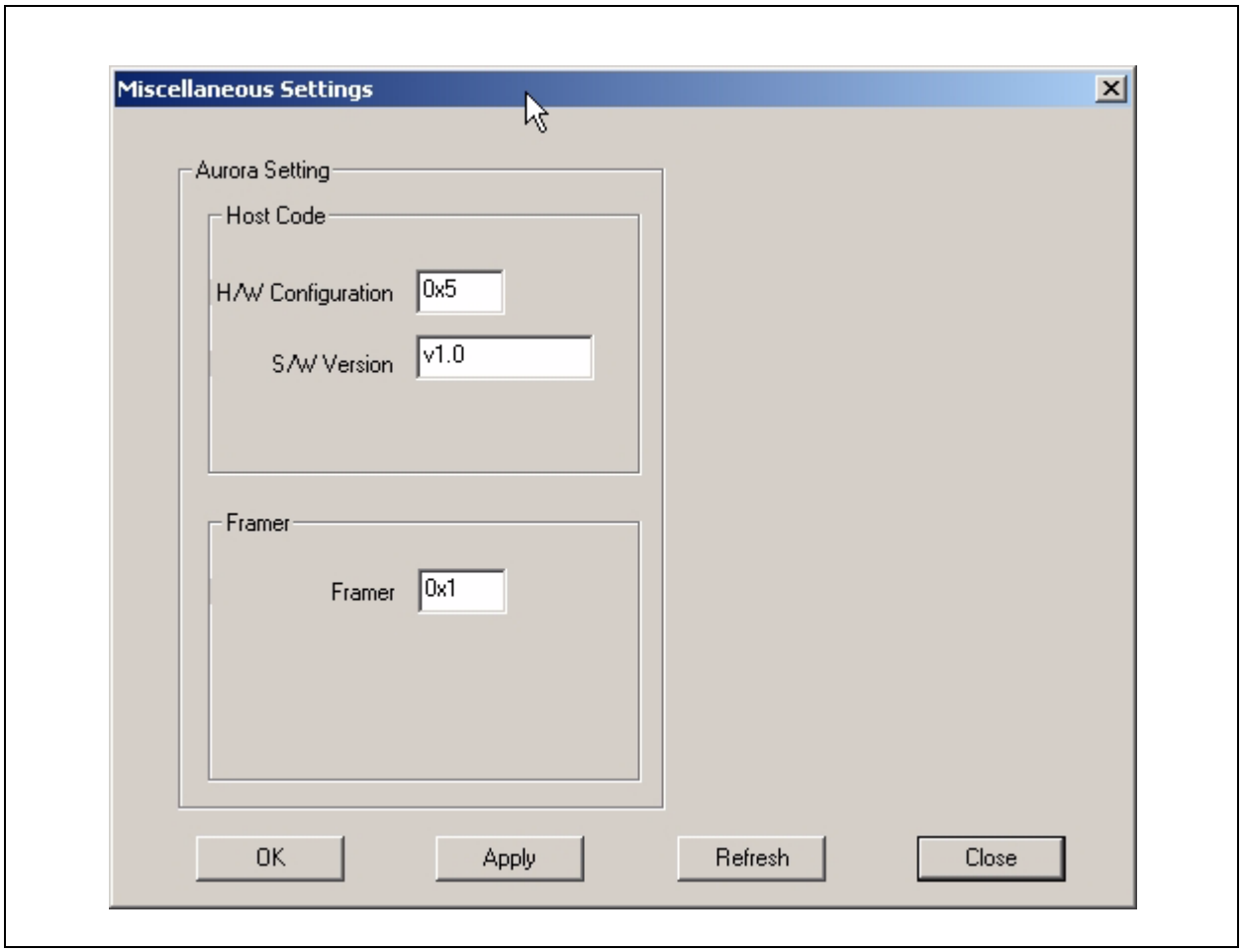
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Select **Slot1**

3.9.5.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x5.
3. Enter the **Framer** value to be 0x1.This configures the T1/E1 Framer for the E1 LIU ONLY Mode.

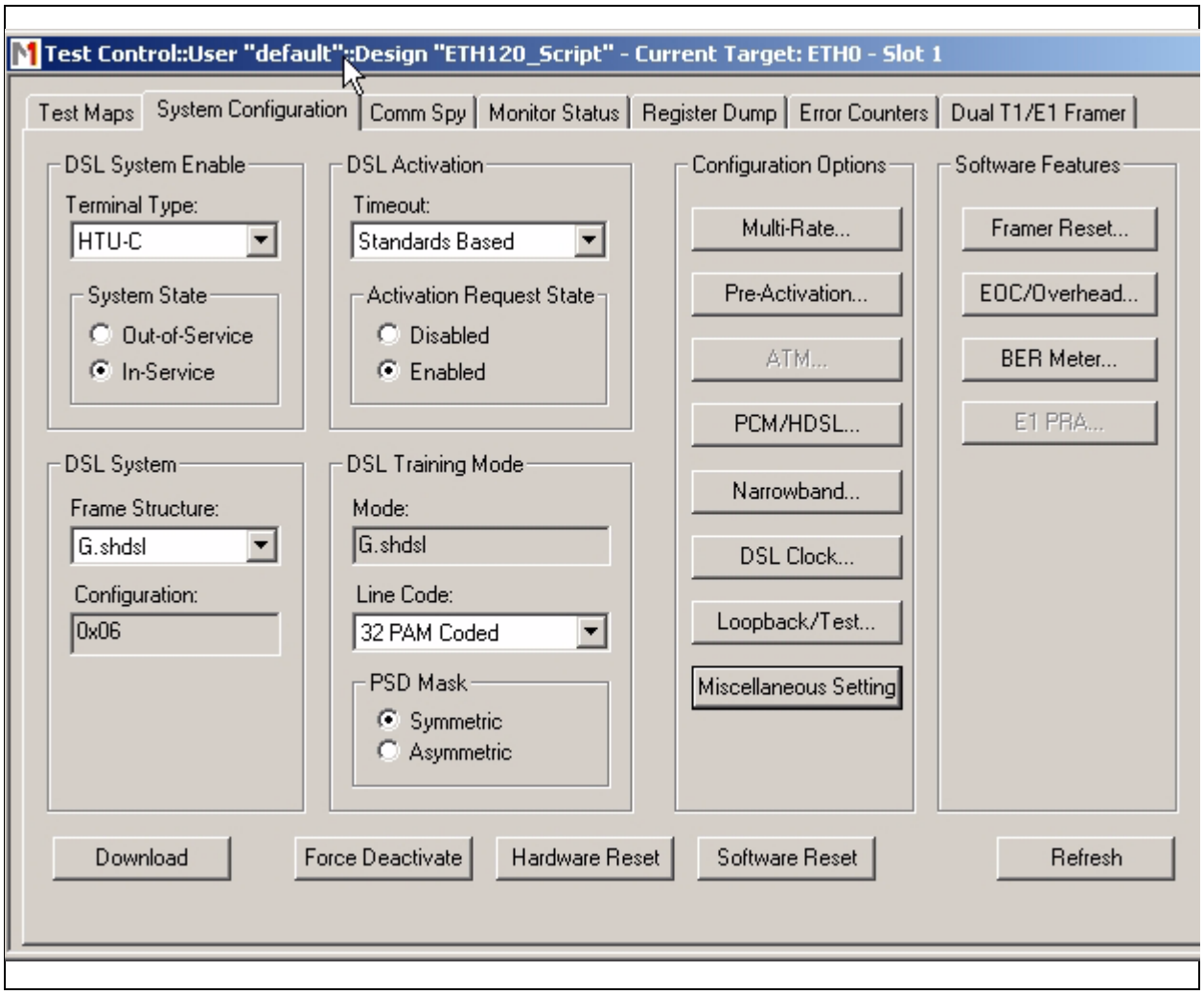
Figure 3-112. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM



3.9.5.2.2 Slot 1 (HTU-C)

1. Set the **System State** to **In-Service**.
2. Set the **Line Code** to be **32 PAM Coded**

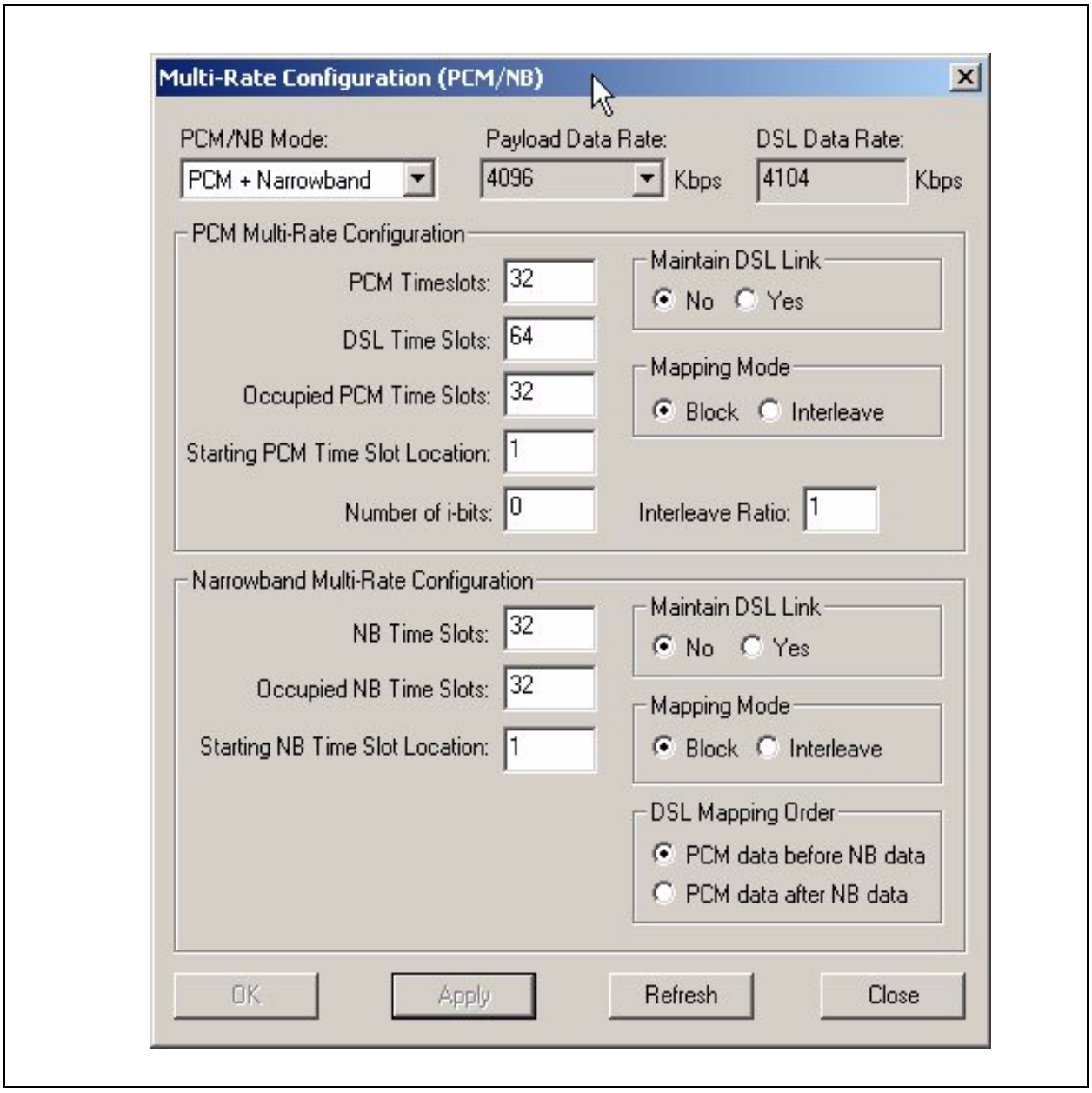
Figure 3-113. System Configuration Window for HTU-C



3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

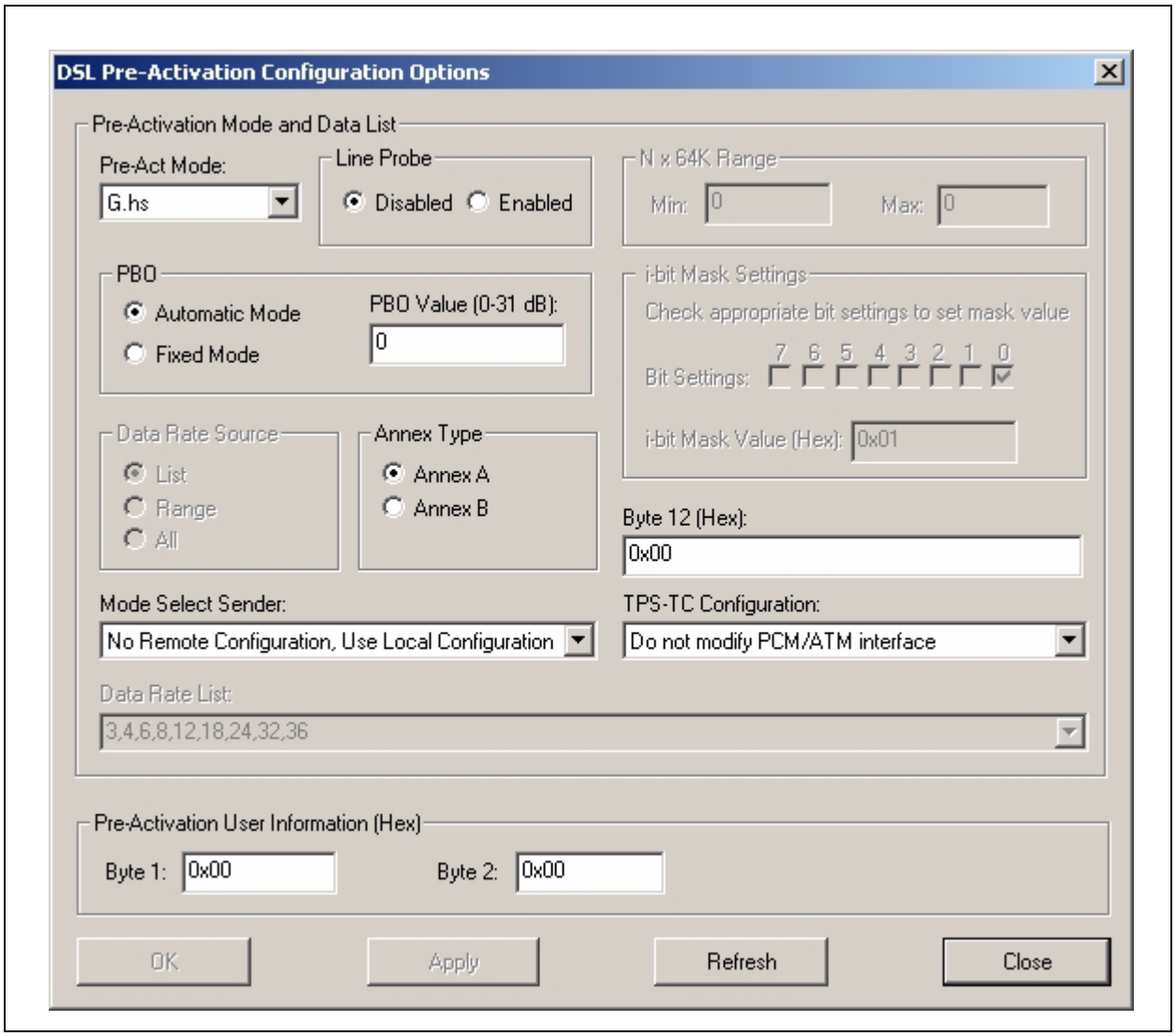
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **64**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **32**
- Starting NB Time Slot Location - **1**

Figure 3-114. TestExec Multi-Rate Configuration for HTU-C



5. Click the **Apply** button. The **Payload Data Rate** will change to 4096 Kbps and the **DSL Data Rate** will change to be 4104 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-115. TestExec Preactivation Configuration for HTU-C

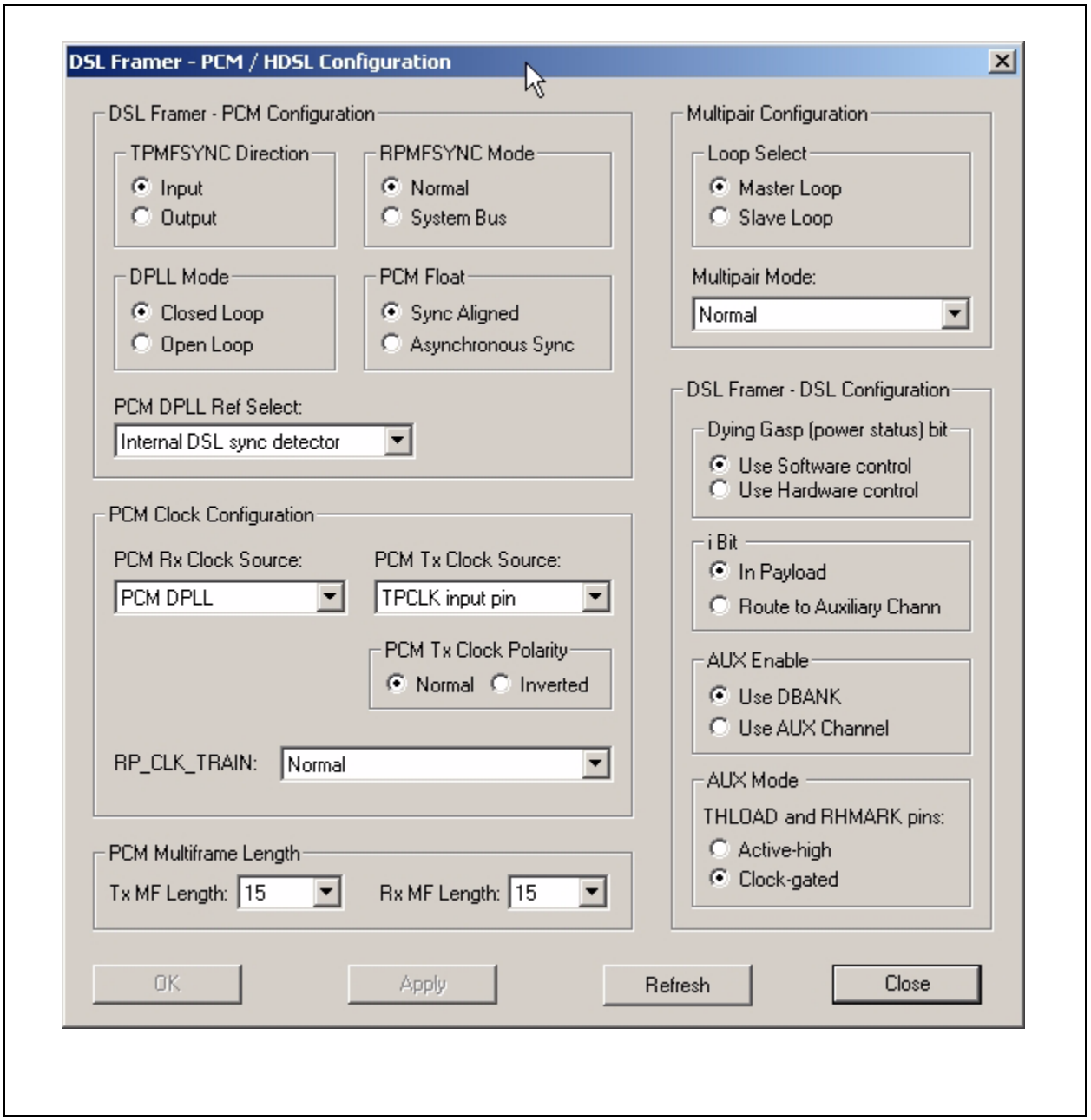


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Change the **Mode Select Sender** to **No Remote Configuration, Use Local Configuration**..
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **PCM/HDSL** button.
11. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PCM DPLL**

  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-116. TextExec PCM/HDSL Configuration for HTU-C



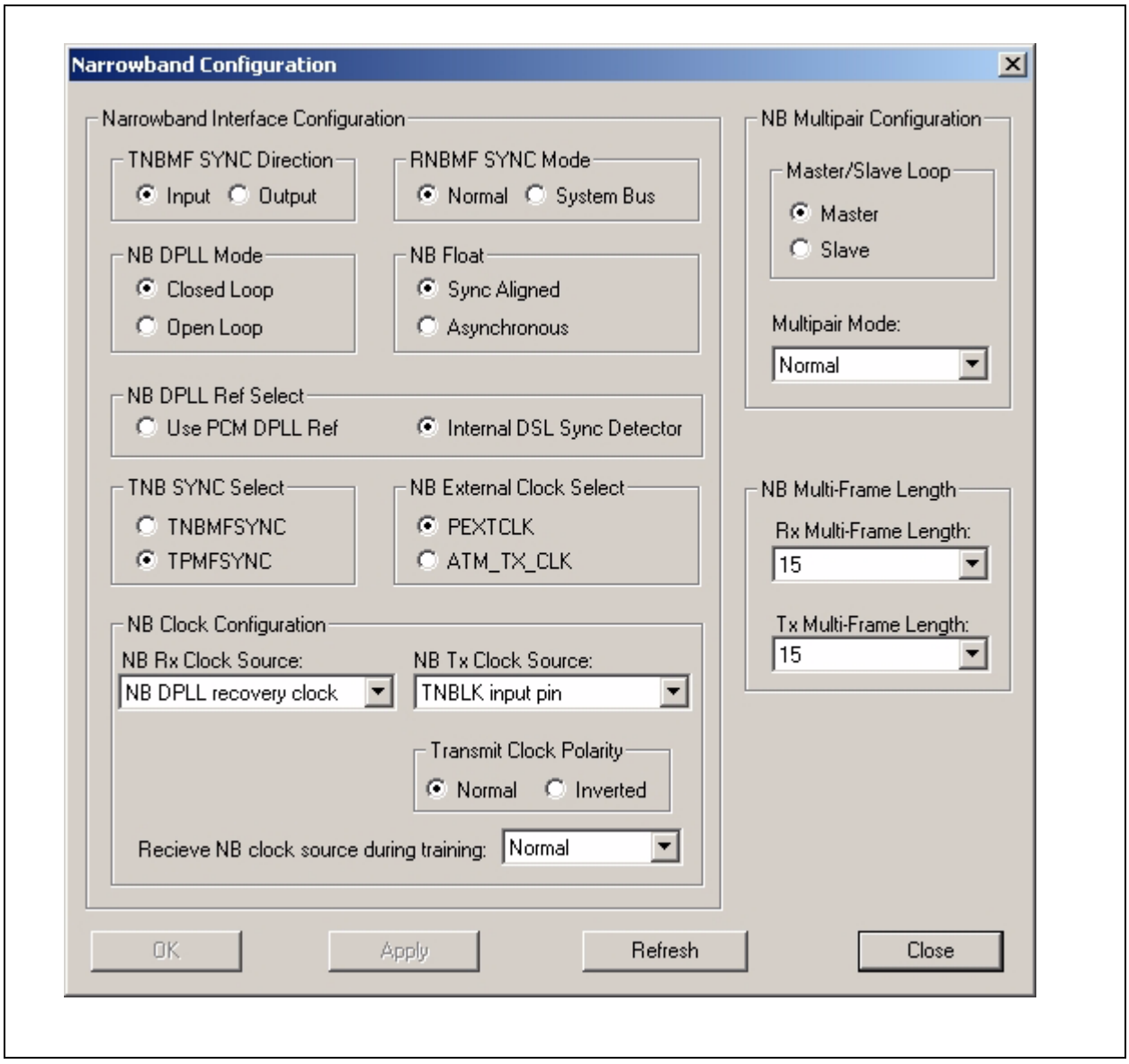
12. Click on **Apply** button and then click on the **Close** button.
13. Click on the **Narrowband** Button.
14. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**

- NB DPLL Ref Select - **Internal DSL Sync Detector**
- TNB Sync Select - **TPMFSYNC**
- NB External Clock Select - **PEXTCLK**

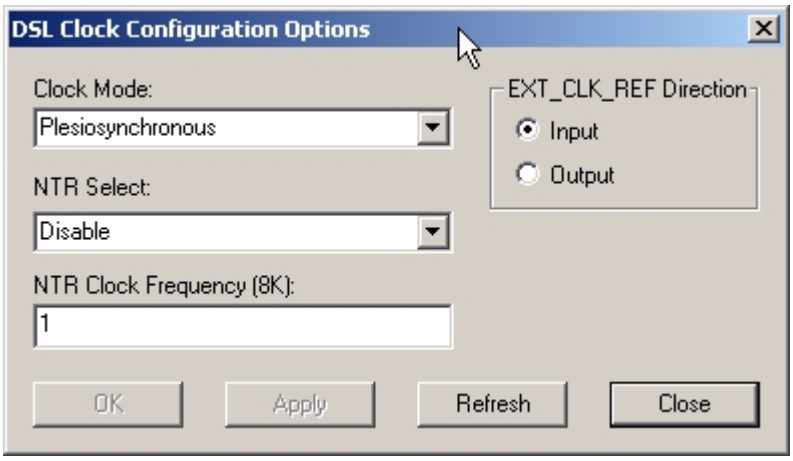
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**

Figure 3-117. TextExec Narrowband Configuration for HTU-C



15. Click on **Apply** button and then click on the **Close** button.
16. Click on the **DSL Clock** Button.
17. Enter the following values:

Figure 3-118. TextExec DSL Clock Configuration for HTU-C



18. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
19. Click on **Comm Spy** Tab.
20. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

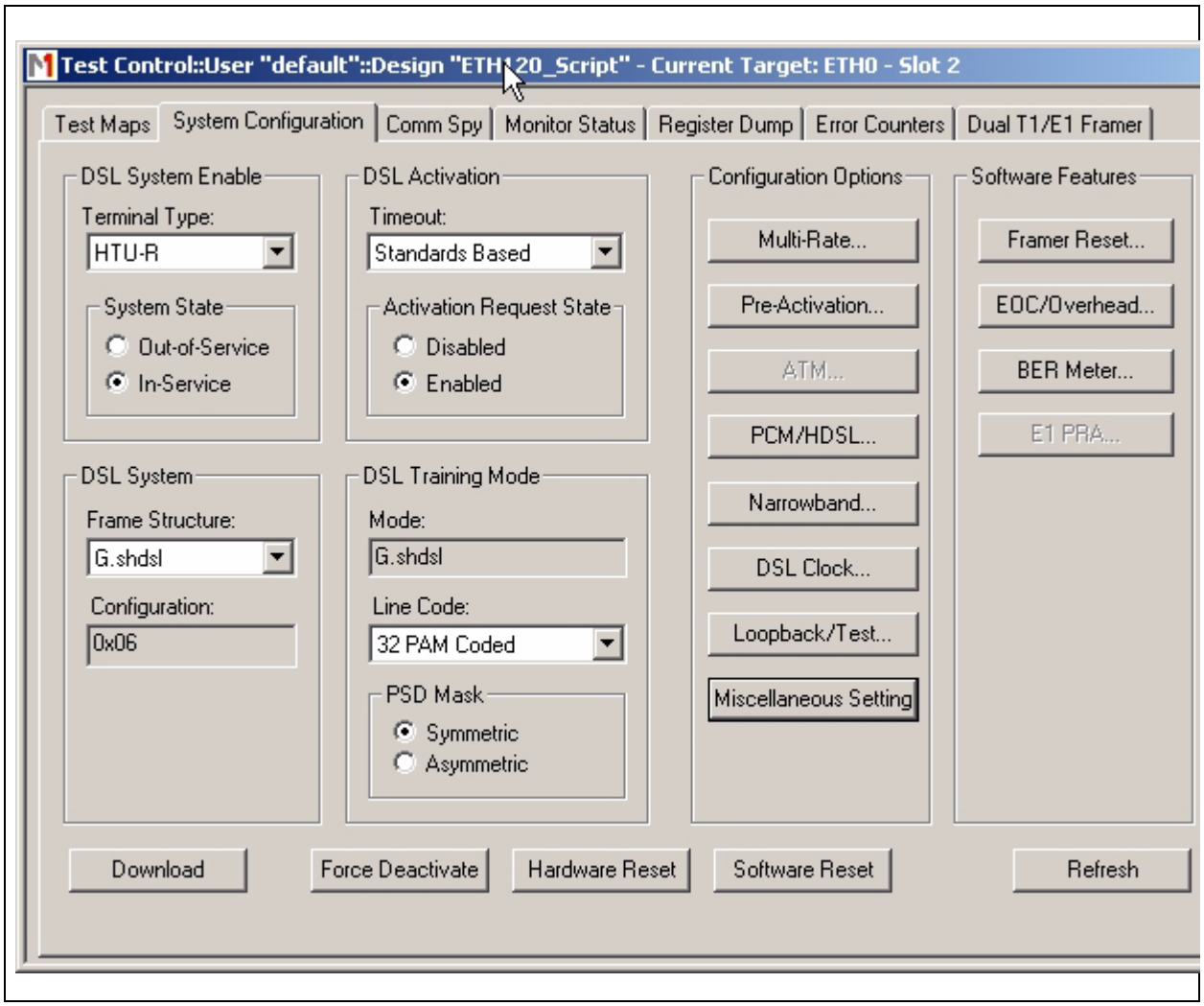
The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

21. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.9.5.2.3 Slot 2 (HTU-R)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Set the **Line Code** to be **32 PAM Coded**

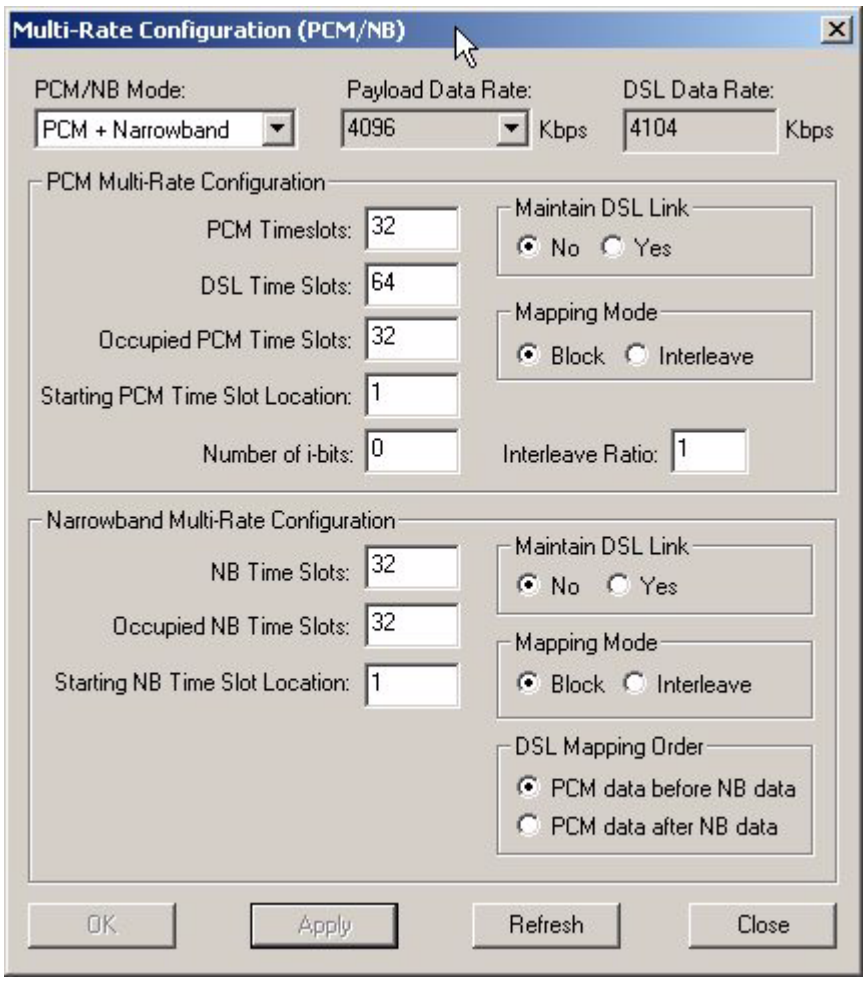
Figure 3-119. System Configuration for HTU-R



4. Click on the **Multi-Rate** Button.
5. Enter the values as follows:

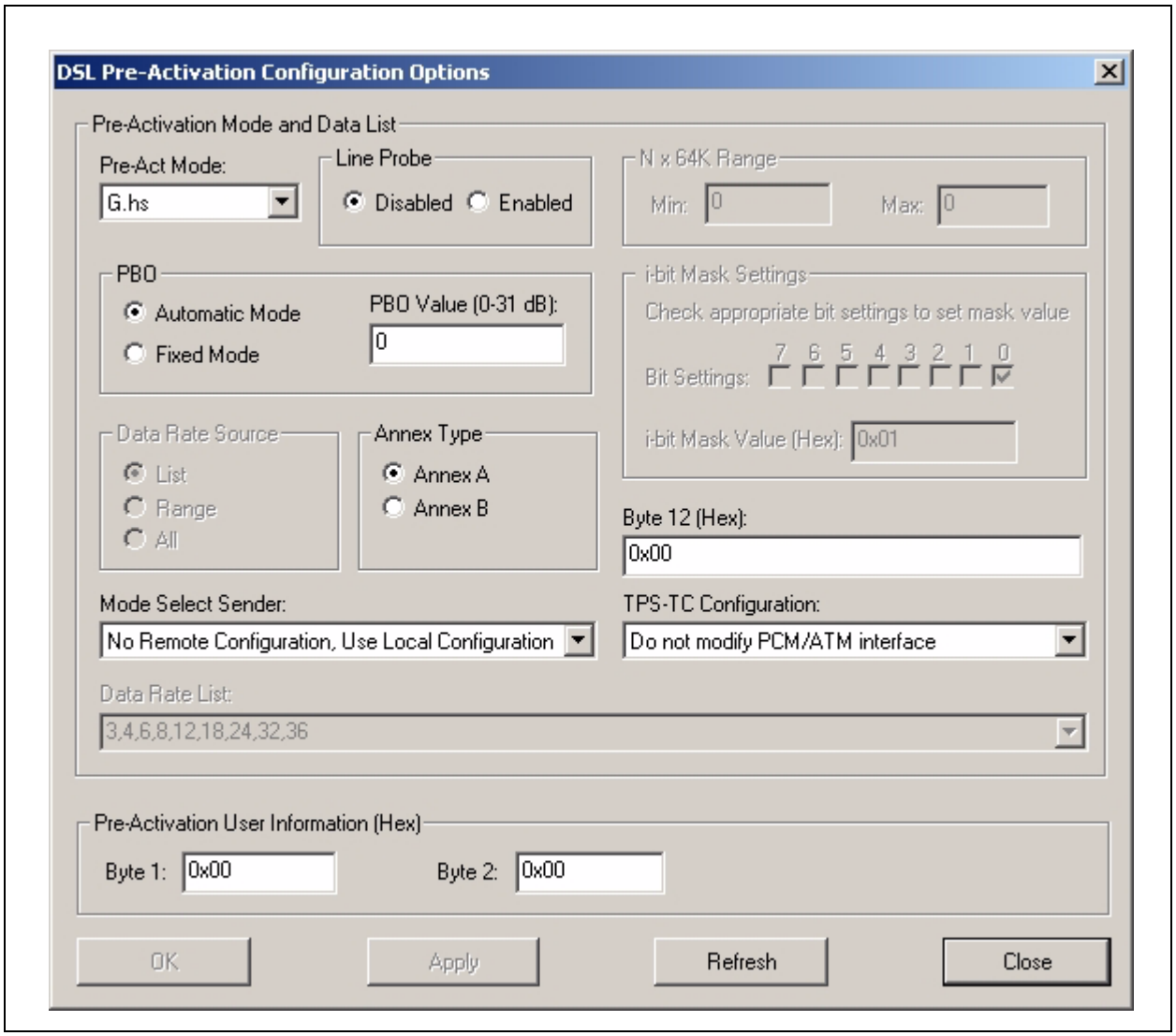
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **64**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **32**
- Starting NB Time Slot Location - **1**

Figure 3-120. TestExec Multi Rate Configuration for HTU-R



6. Click the **Apply** button. The Payload Data Rate will change to 4096 Kbps and the DSL Data Rate will change to be 4104 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

Figure 3-121. TestExec Preactivation Configuration for HTU-R



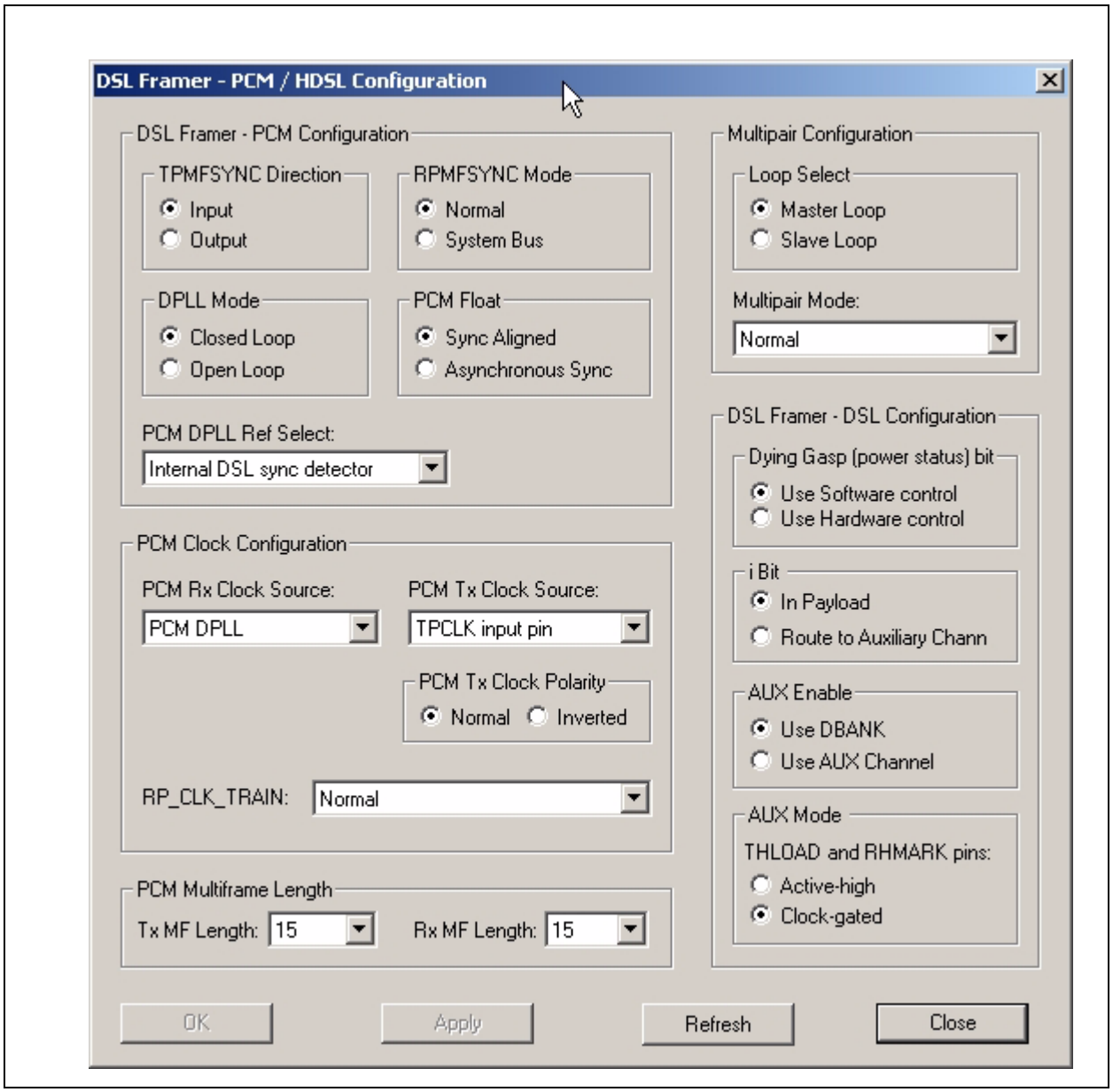
8. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
9. Change the **Mode Select Sender** to **No Remote Configuration, Use Local Configuration**.
10. Click on **Apply** button and then click on the **Close** button.
11. Click on the **PCM/HDSL** button.
12. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PCM DPLL**

- PCM Tx Clock Source - **TPCLK Input**
- PCM Tx Clock Polarity - **Normal**
- RP_CLK_TRAIN - **Normal**

- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-122. TestExec PCM/HDSL Configuration for HTU-R

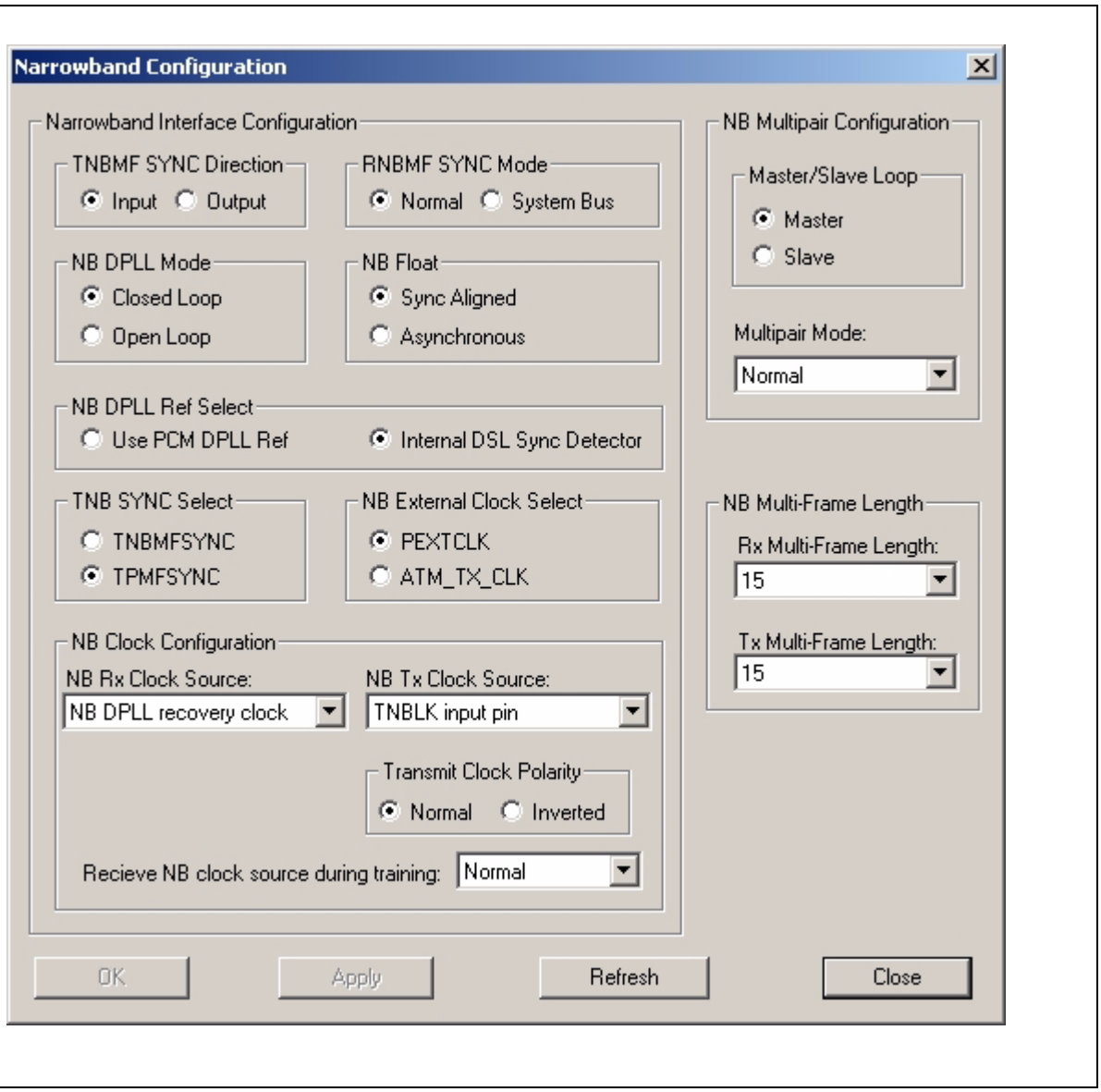


13. Click on **Apply** button and then click on the **Close** button.
14. Click on the **Narrowband** Button.
15. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**

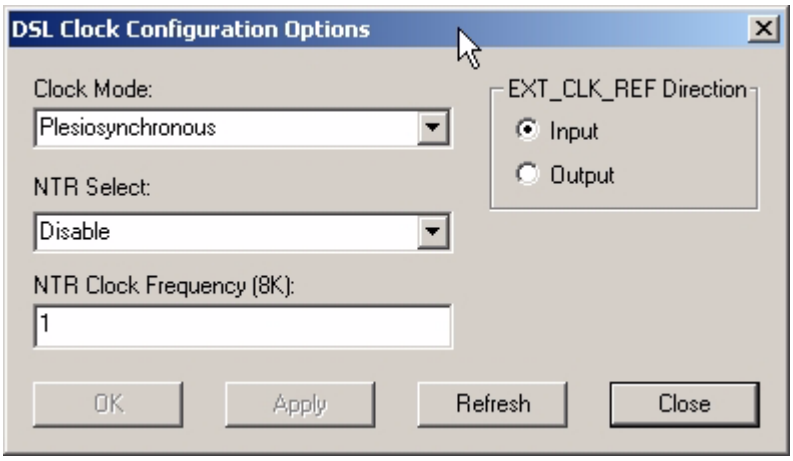
    - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
    - NB Rx Clock Source - **NB DPLL recovery clock**
    - NB Tx Clock Source - **TNBCLK Input Pin**
    - Transmit Clock Polarity - **Normal**
    - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
    - Master/Slave Loop - **Master**
    - Multipair Mode - **Normal**
- NB Multiframe Length
    - Tx MF Length - **15**
    - Rx MF Length - **15**

Figure 3-123. TextExec Narrowband Configuration for HTU-R



16. Click on **Apply** button and then click on the **Close** button.
17.
18. Click on the **DSL Clock** Button.
19. Enter the following values:

Figure 3-124. TextExec DSL Clock Configuration for HTU-R



20. Click on **Comm Spy** Tab.
21. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

    The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.
22. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.9.5.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.

3.9.5.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-110. The modems are configured to

automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.9.5.4 Varying the rates for PCM and Narrowband

The above configuration transports 32 timeslots of framed PCM data and 32 timeslorts of unframed Narrowband data. The user can vary the rates for PCM and Narrowband. Please note that the user would need to set the water level for the PCM and Narrowband traffic. This can be done through the Comm Spy window in the TestExec using the APIs _DSL_PCM_WATER_LEVEL (0x2C) and _DSL_NB_WATER+LEVEL (0x2D).

3.10 Enhanced EVM Setup for 4-wire Cascade Mode E1 Transport (using M28947 integrated Framer) and Unframed Narrowband Operation

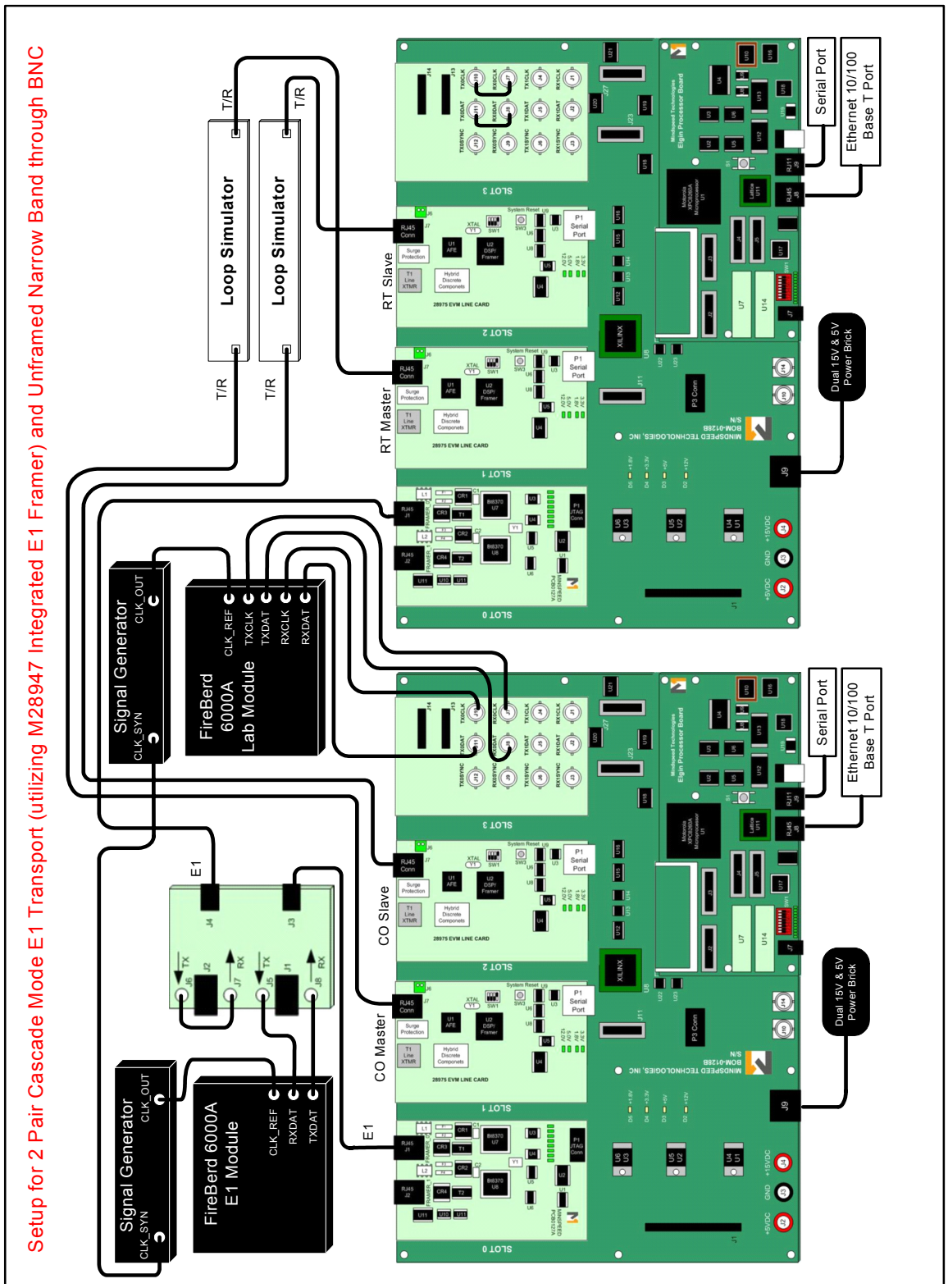
The following steps are required for running the ZipWirePlus Enhanced EVM in 4-wire Cascade Mode E1 Transport and Unframed Narrowband Operation. This setup needs two enhanced EVMs.

First, we shall use only the HTU-C EVM and put the DSL side is put into loopback. Then we shall perform end to end testing with two enhanced EVMs. The Hardware setup for this application is shown in Figure 3-125.

This application can be run on the M28947 device only.

NOTE: This setup needs two(2) fireberds (one with 2M/nX64, one with Lab Interface Adapter). Please note that the Fireberds should have the same clock source. Two function generators have been used for that. Figure 3-125 illustrates the required interconnections.

Figure 3-125. Enhanced EVM Setup for Two-Pair Cascade Mode E1 (using E1 Integrated Framer) and Narrowband (unframed) Transport



3.10.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Fireberd Connections -
   - Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-C PCM Ports. Connect the Function Generator #1 output (2048 khz signal) to the **GEN CLK IN** port on the Fireberd. Please note the reference signal from this Function Generator should be fed to Function Generator #2.
   - Fireberd #2 - Make the following connections
     – TX DATA (Fireberd) to RX0DAT (BNC Tester)
     – TX CLK OUT(Fireberd) to RX0CLK (BNC Tester)
     – RCV DATA (Fireberd) to TX0DAT (BNC Tester)
     – RCV CLK (Fireberd) to TX0CLK (BNC Tester)

   Connect the Function Generator #2 output (number of timeslots X 64 khz signal) to the **GEN CLK IN** port on the Fireberd.
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

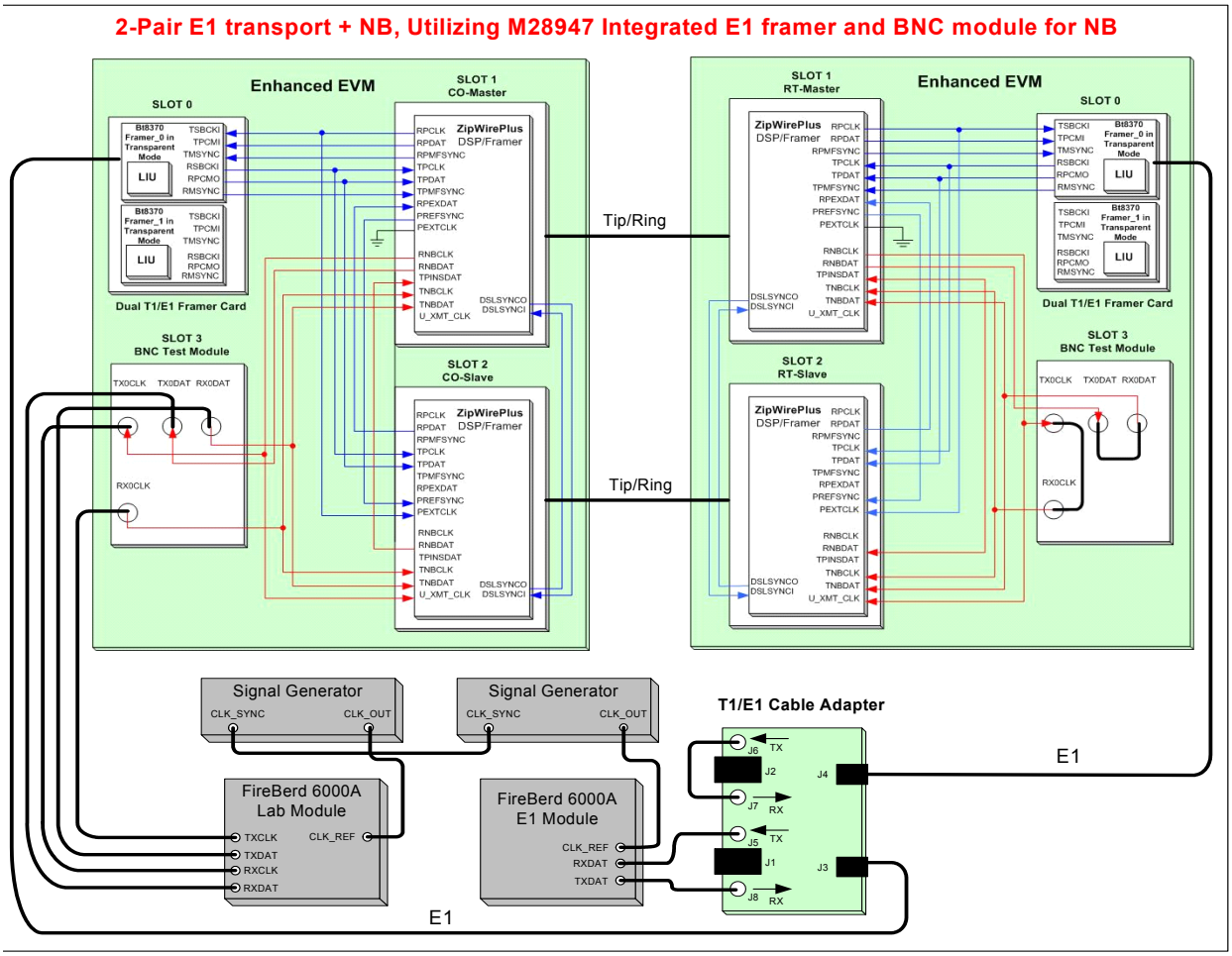
3.10.2 Fireberd Setup

1. Configure the Fireberd #1 E1 Module front panel as follows:
   - DATA: 2^{23}-1
   - GEN CLK: BNC
   - INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
   - INTF SETUP: 2M/n64: MODE: FULL2M
2. Configure the Fireberd#2 Lab Interface Adapter as follows
   - DATA: 2^{23}-1
   - GEN CLK: BNC

3.10.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Framer #0 (slot 0) and the Narrowband bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Port 0 of the BNC Tester Card(slot 3). The Figure 3-126 explains the pin interconnections for this application.

Figure 3-126. Two-Pair Cascade Mode E1 (using E1 Integrated Framer) and Narrowband (unframed) Transport



3.10.4 Enhanced EVM Configuration

3.10.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28947.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.10.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.10.5 TestExec

3.10.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software.

We will use the EnhancedEvm design file for the HTU-C Enhanced EVM.

3.10.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup.
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

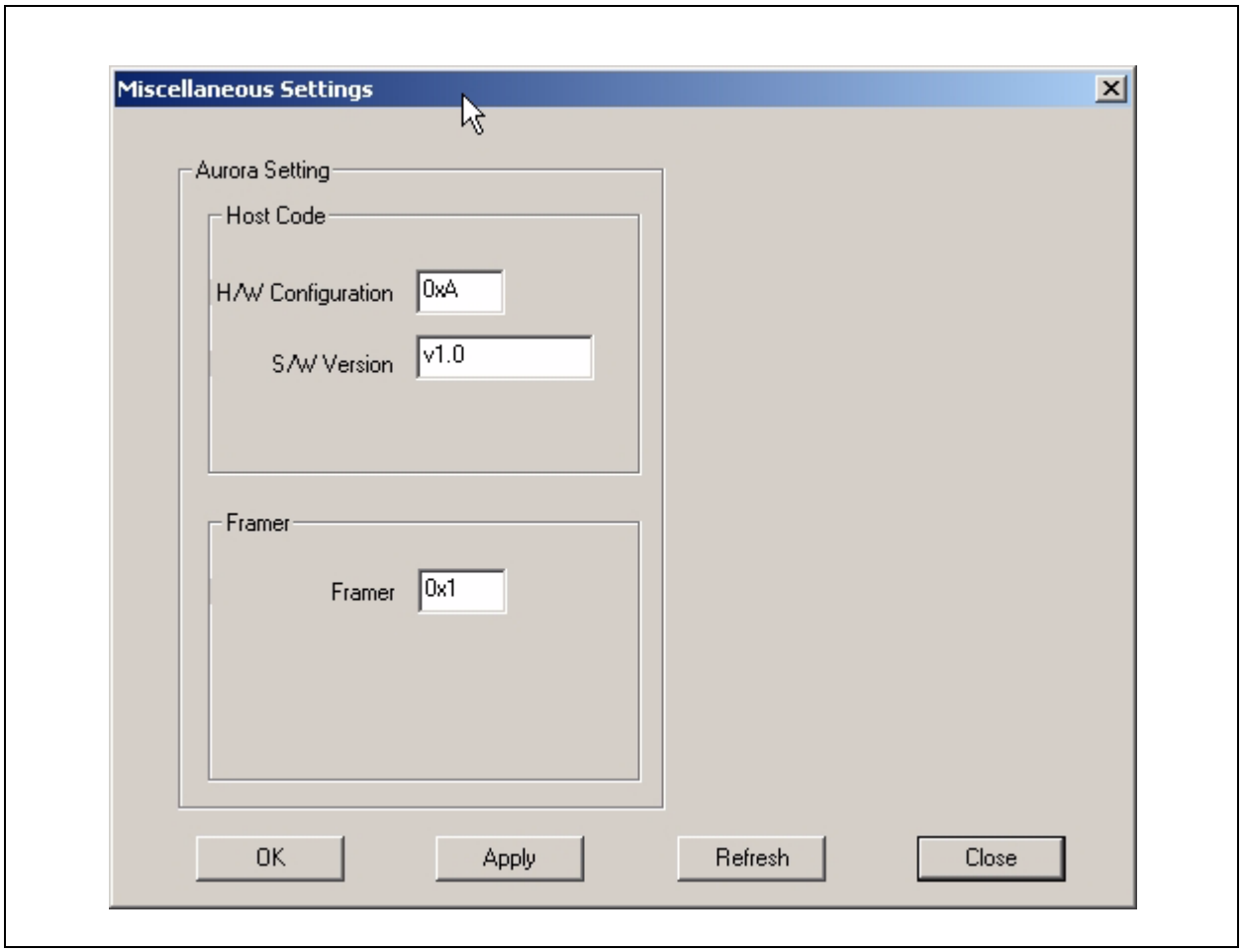
   b.**EnhancedEvm2**

   c.**LegacyEvm**
5. Select the **EnhancedEvm** design file. The TestExec will load the selected design file. Please note that for the HTU-C (CO) side EVM please select **EnhancedEvm** design file. For HTU-R (RT) side EVM please select the **EnhancedEvm2** design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. Select **Slot 1** by right clicking the mouse.

3.10.5.2.1 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0xA.
4. Enter the **Framer** value to be 0x1.This configures the T1/E1 Framer for the E1 LIU ONLY Mode.

Figure 3-127. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

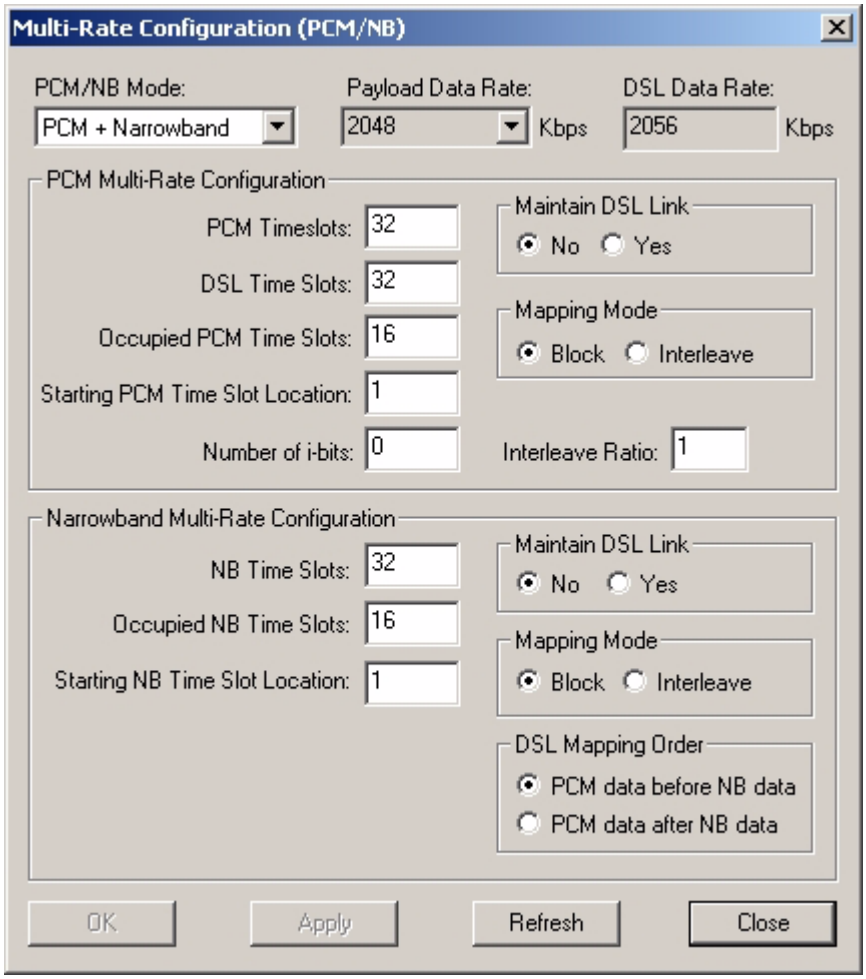


3.10.5.2.2 Slot 1 (HTU-C Master)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

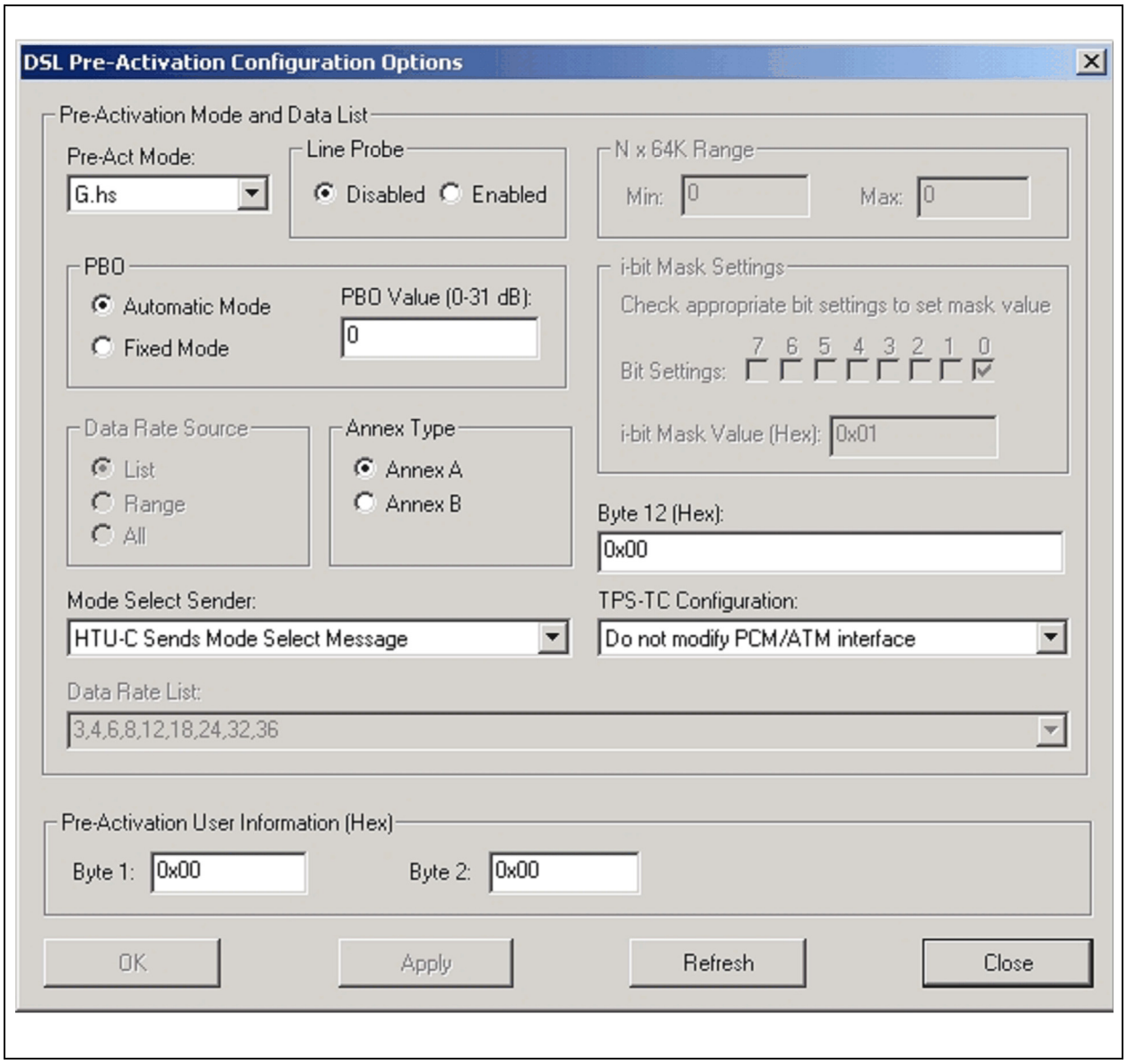
- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**
- Occupied NB Time Slots - **16**
- Starting NB Time Slot Location - **1**

Figure 3-128. TestExec Multi-Rate Configuration for Master



5. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-129. TestExec Preactivation Configuration for Master

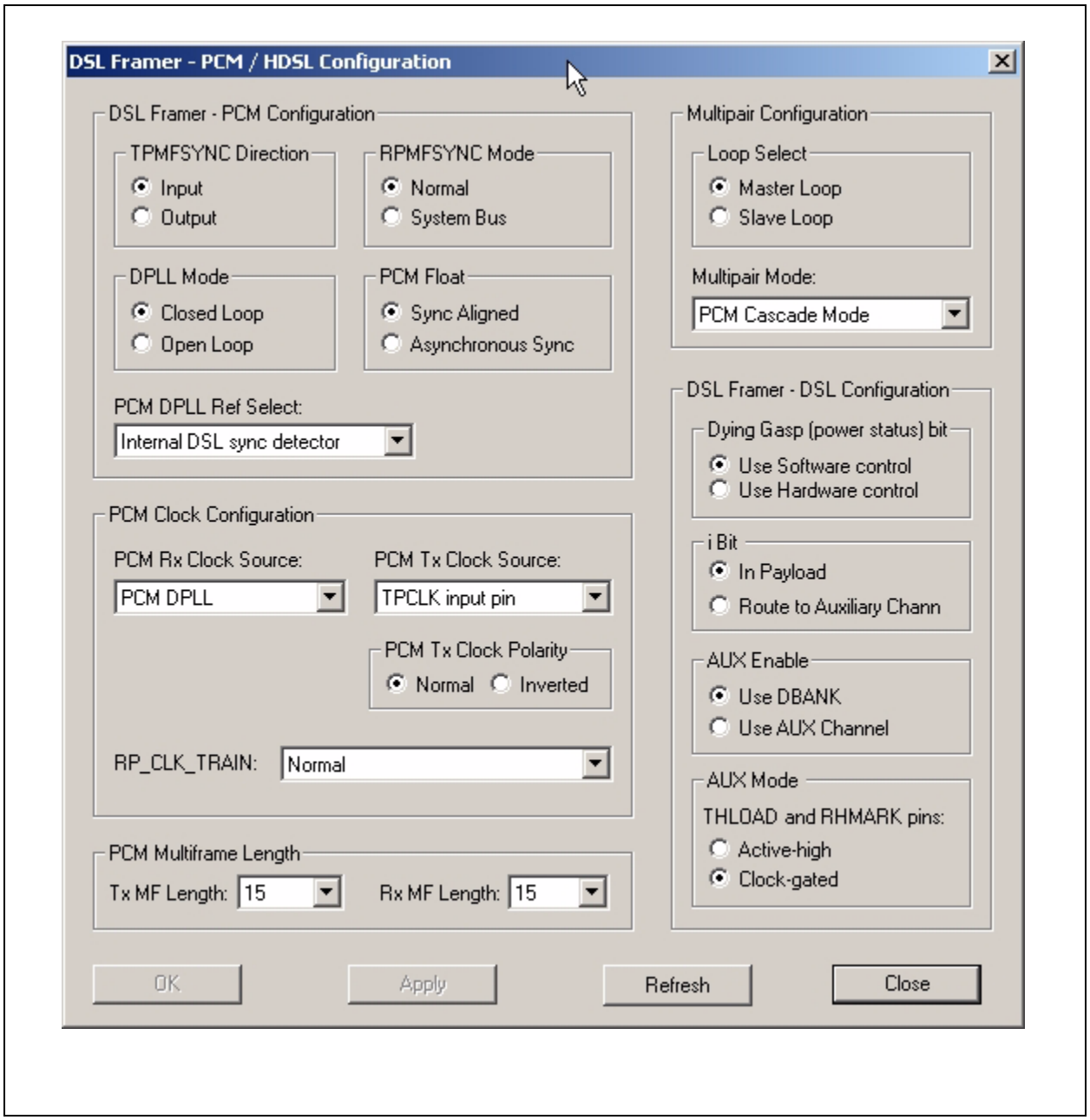


7. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration

  - PCM Rx Clock Source - **PCM DPLL**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-130. TextExec PCM/HDSL Configuration for Master

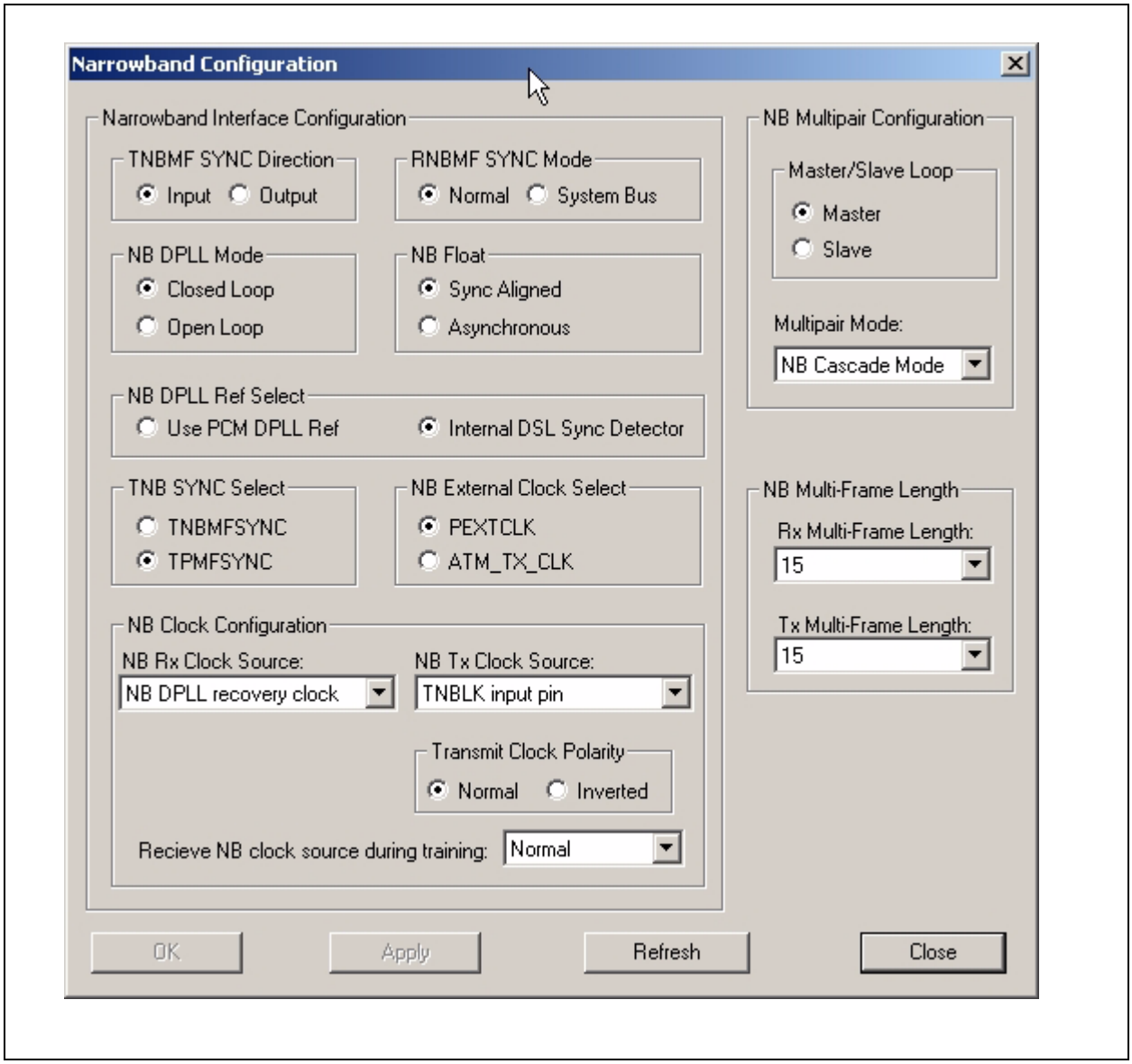


11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **Narrowband** Button.
13. Enter the following values:

- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Closed Loop**
  - NB Float - **Sync Aligned**

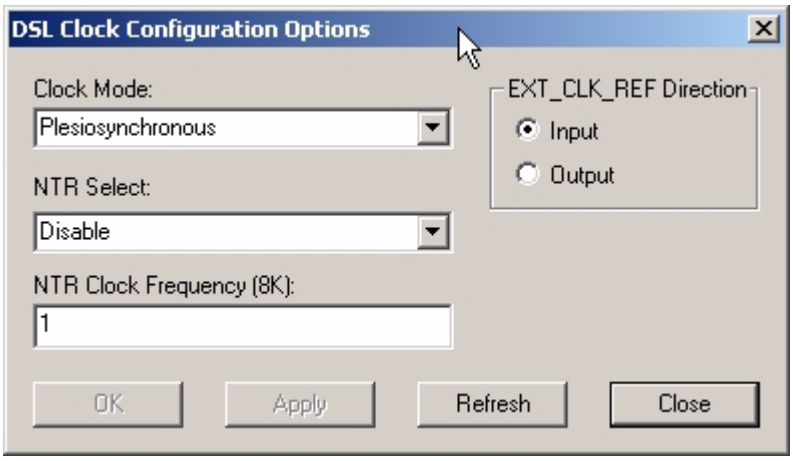
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**

Figure 3-131. TextExec Narrowband Configuration for Master



14. Click on **Apply** button and then click on the **Close** button.
15. Click on the **DSL Clock** Button.
16. Enter the following values:

Figure 3-132. TextExec DSL Clock Configuration for Master



17. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
18. For setting the water level for the Narrowband Interface, Click on **Comm Spy** Tab.
19. Enter the following values
    - Opcode (HEX) - **2D**
    - Data (HEX) - **00 A0 00 A0 00**
20. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**

The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode.

21. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
22. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

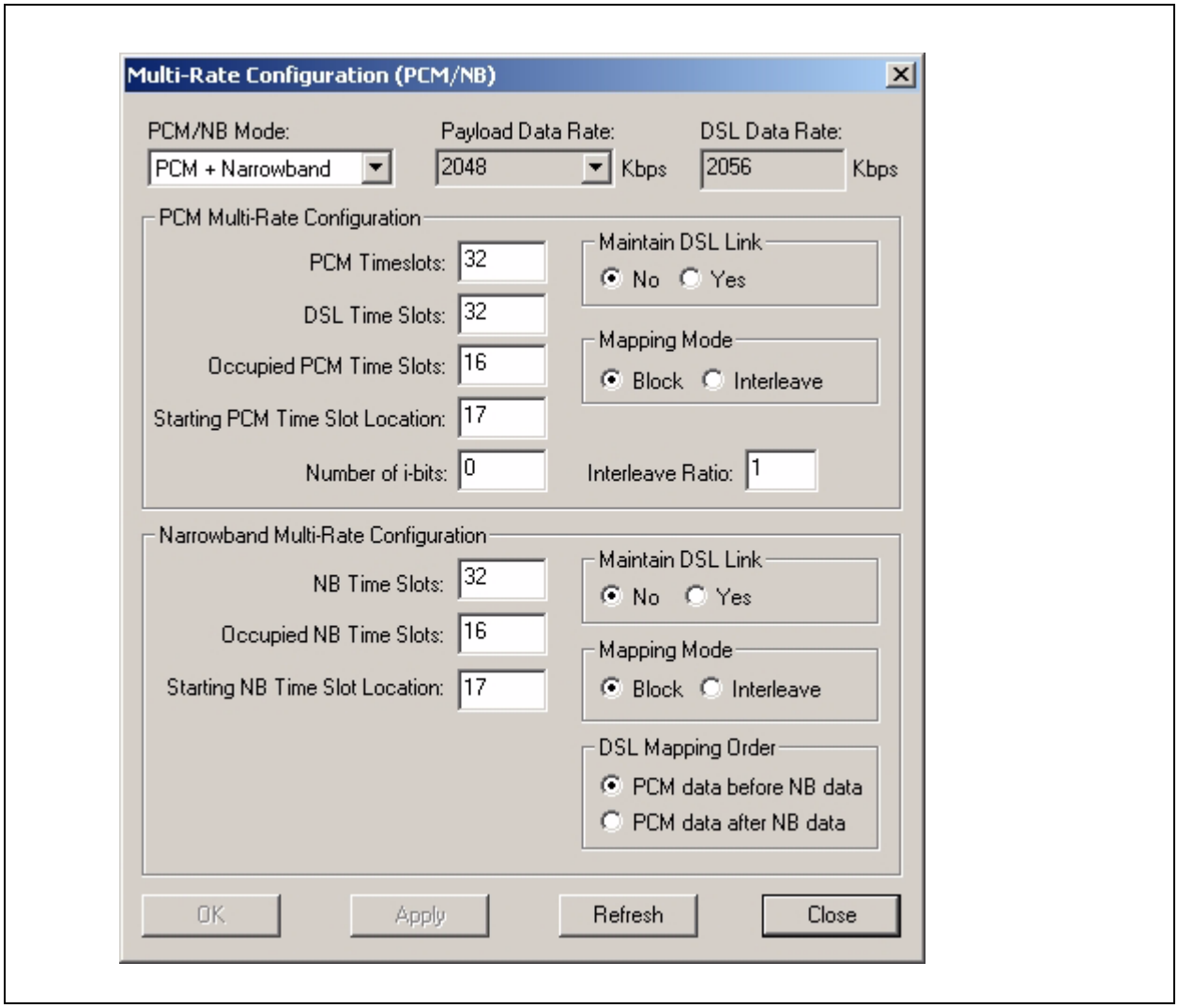
3.10.5.2.3 Slot 2 (HTU-C Slave)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

- PCM/NB Mode - **PCM + Narrowband**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**
- NB Time Slots - **32**

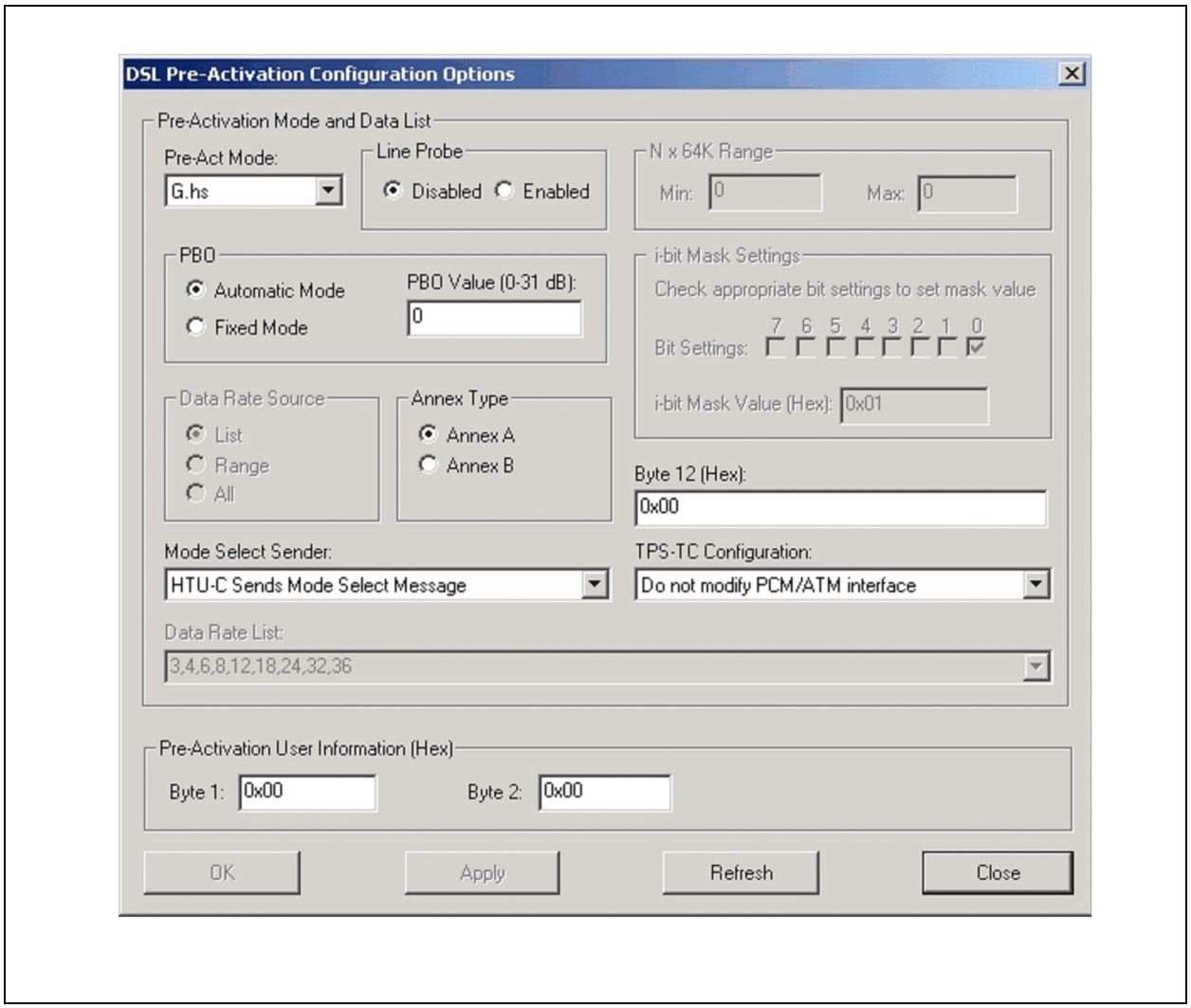
- Occupied NB Time Slots - **16**
- Starting NB Time Slot Location - **1**

Figure 3-133. TestExec Multi Rate Configuration for Slave



5. Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-134. TestExec Preactivation Configuration for Slave

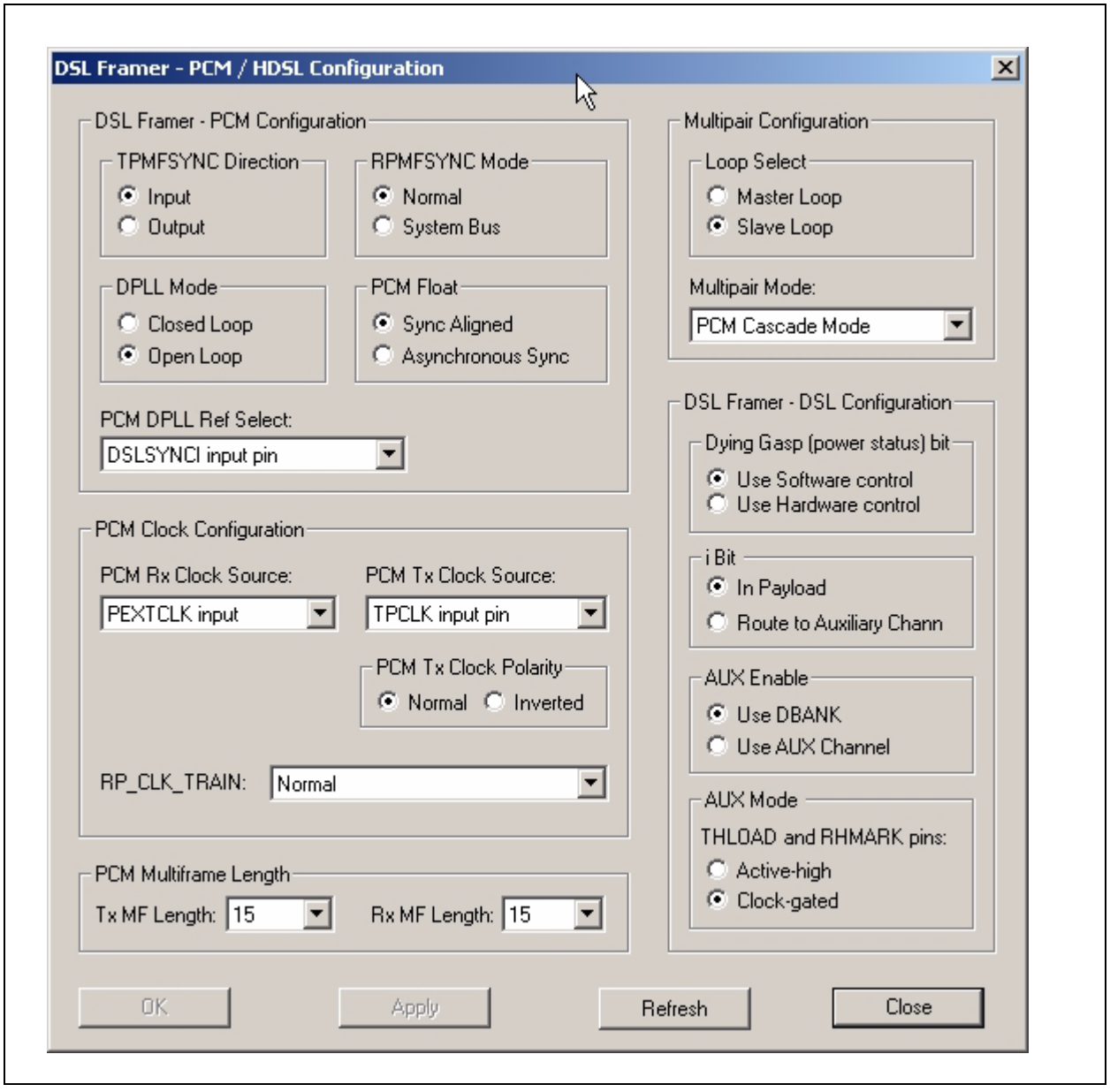


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **DSLSYNCI input pin**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PEXTCLK input**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**

- PCM Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**
- Multipair Configuration
  - Loop Select - **Slave Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

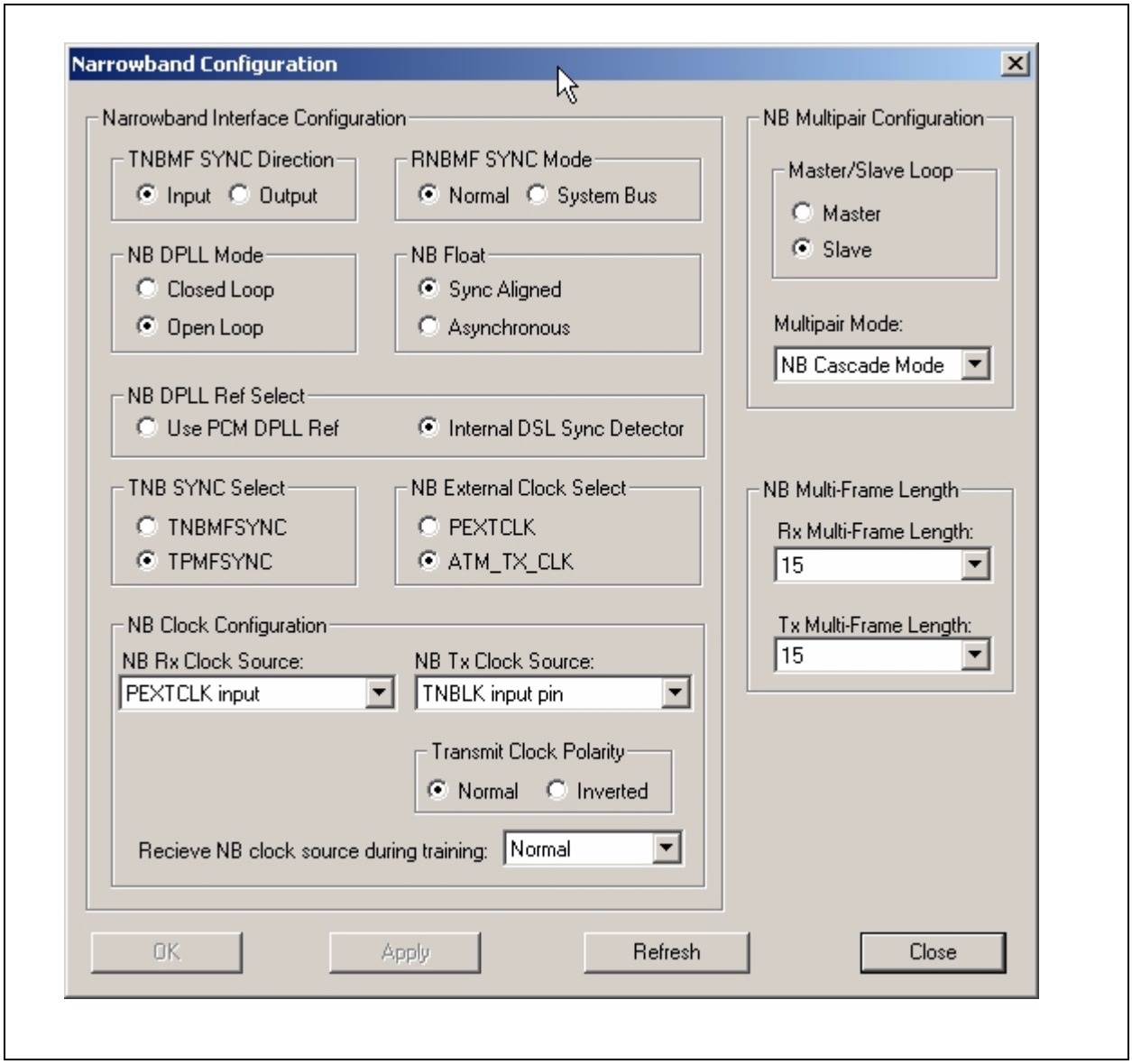
Figure 3-135. TextExec PCM/HDSL Configuration for Slave



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **Narrowband** Button.
13. Enter the following values:

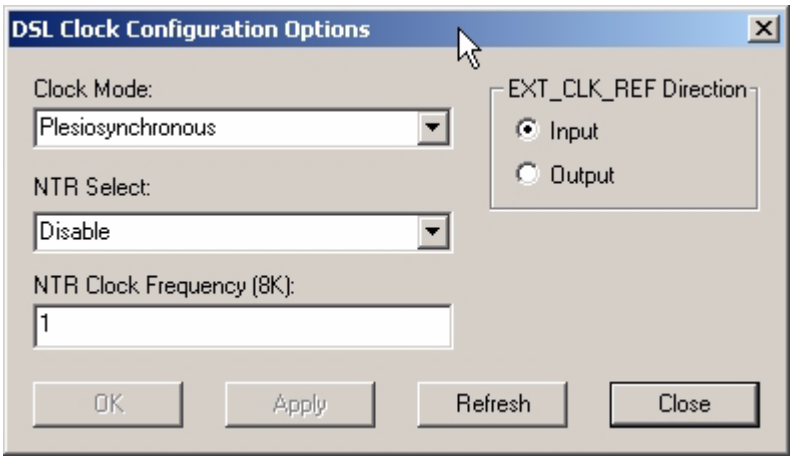
- Narrowband Interface Configuration
  - TNBFSYNC Direction - **Input**
  - RNBMFSYNC Mode - **Normal**
  - NB DPLL Mode - **Open Loop**
  - NB Float - **Sync Aligned**
  - NB DPLL Ref Select - **Internal DSL Sync Detector**
  - TNB Sync Select - **TPMFSYNC**
  - NB External Clock Select - **PEXTCLK**
- NB Clock Configuration
  - NB Rx Clock Source - **NB DPLL recovery clock**
  - NB Tx Clock Source - **TNBCLK Input Pin**
  - Transmit Clock Polarity - **Normal**
  - Receive NB clock source during training - **Normal**
- NB Multipair Configuration
  - Master/Slave Loop - **Master**
  - Multipair Mode - **Normal**
- NB Multiframe Length
  - Tx MF Length - **15**
  - Rx MF Length - **15**

Figure 3-136. TextExec Narrowband Configuration for Slave



14. Click on **Apply** button and then click on the **Close** button.
15. Click on the **DSL Clock** Button.
16. Enter the following values:

Figure 3-137. TextExec DSL Clock Configuration for Master

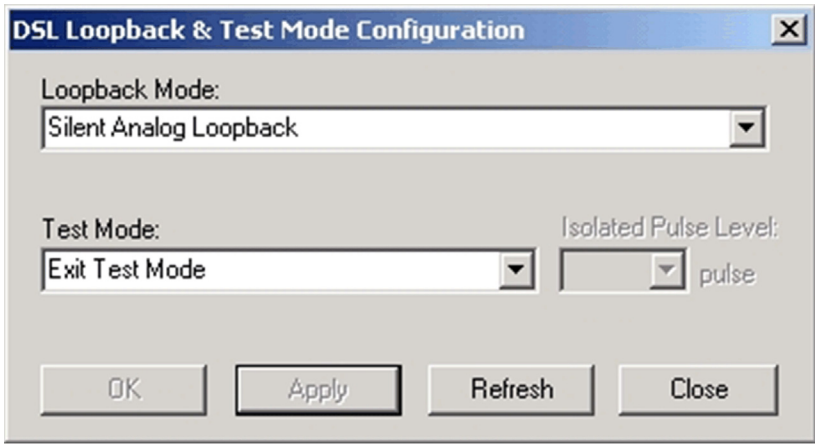


17. For setting the water level for the Narrowband Interface, Click on **Comm Spy** Tab.
18. Enter the following values
    - Opcode (HEX) - **2D**
    - Data (HEX) - **00 A0 00 A0 00**
19. Enter the following values for enabling the Internal E1 Framer Feature.
    - Opcode (HEX) - **44**
    - Data (HEX) - **07 00 00 00 00**
    - The API _E1_PRA_CONFIG will enable the Internal E1 framer, internally generate the Multi-frame syncs and set all the overhead bits handling into the Transparent Mode
20. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.10.5.2.4 Loopback

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Loopback/Test** button.
3. Set the **Loopback Mode** to **Silent Analog Loopback**.

Figure 3-138. Setting the ZipwirePlus Device into Loopback



4. Click on the **Apply** button and then click on the Close button.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Click on the **Loopback/Test** button.
7. Set the **Loopback Mode** to **Silent Analog Loopback**. Click on the **Apply** button and then click on the **Close** button.

3.10.5.2.5 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the Set button in the **Auto Update Timer** box.
4. Verify that the Training Status is **GREEN** and showing **IDLE** State.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2.**
6. Repeat Steps 2 - 4.

3.10.5.2.6 FIFO Resets

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on Framer Reset button under Software Features.
3. Issue FIFO resets for the Master Loop in the following sequence.
   - Click on **TX_WL_RESET**
   - Click on **TX_FIFO_RESET**
   - Click on **RX_WL_RESET**
   - Click on **RX_FIFO_RESET**
4. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
5. Repeat Steps 2-3.
6. Verify the Fireberd #1 is in SYNC with no Bit Errors.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
8. For issing FIFO resets for the Narrowband Interface, Click on **Comm Spy** Tab.
9. Enter the following values

- Opcode (HEX) - **75**
- Data (HEX) - **01 50 00 05**

10. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
11. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 35**
12. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
13. Click on Framer Reset button under Software Features.
14. Issue FIFO resets for the Master Loop in the following sequence.
    - Click on **TNB_WL_RESET**
    - Click on **TNB_FIFO_RESET**
    - Click on **RNB_WL_RESET**
    - Click on **RNB_FIFO_RESET**
15. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
16. Repeat Steps 13-14.
17. Verify the Fireberd #2 is in SYNC with no Bit Errors or else repeat Steps 12 - 16.
18. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**
19. Click on **Comm Spy** Tab.
20. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 04**
21. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**
22. Enter the following values
    - Opcode (HEX) - **75**
    - Data (HEX) - **01 50 00 34**

3.10.6 End to End Testing Using Two Enhanced EVMs

For end to end testing, one additional Enhanced EVM is needed.

3.10.6.1 Enhanced EVM Setup

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(Master HTU-C) and Slot 2(Slave HTU-C) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11 port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-R and the ZipWirePlus LIC in Slot 2 as the Slave HTU-R. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. BNC Tester Card Connections - Make the following connections

- TX1DAT to RX1DAT
- TX1CLK to RX1CLK

7. Loopback externally the FRAMER_1 of the Dual T1/E1 card using the T1/E1 cable adapter.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
9. Set up for Zero Loop Length

   a) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Master Slot 1) to J7 of the ZipWirePlus LIC(HTU-R Master Slot 1) of this Enhanced EVM.

   b) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Slave Slot 2) to J7 of the ZipWirePlus LIC(HTU-R Slave Slot 2) of this Enhanced EVM.

3.10.6.2 TestExec

3.10.6.2.1 Installation and Configuration

Please refer to Section 3.2.5.1 for detailed procedure for installing the configuring the TestExec(UIP) software.

Assuming the same PC is being used to control both HTU-C & HTU-R, we will use the **EnhancedEvm2** design file for the HTU-R Enhanced EVM.

3.10.6.2.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup.
3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

   c.**LegacyEvm**
5. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. Setup the Hardware Configuration as defined in Section 3.10.5.2.1.

3.10.6.2.3 Slot 1 (HTU-R Master)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Master card. Please refer to Section 3.10.5.2.2.

3.10.6.2.4 Slot 2 (HTU-R Slave)

1. Click on the **System Configuration** Tab.

2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Slave card. Please refer to Section 3.10.5.2.2.

3.10.6.2.5 Loop Activation

Please refer to Section 3.6.6.2.5.

3.10.6.2.6 Monitor the Link

1. Go the HTU-C TestExec GUI.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Click on the **Monitor Status** tab.
4. Click the **Set** button in the **Auto Update Timer** box.
5. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State.
6. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
7. Repeat Steps 2 - 4.

3.10.6.2.7 FIFO Resets

Please refer to Section 3.6.6.2.7.

3.10.6.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-125. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

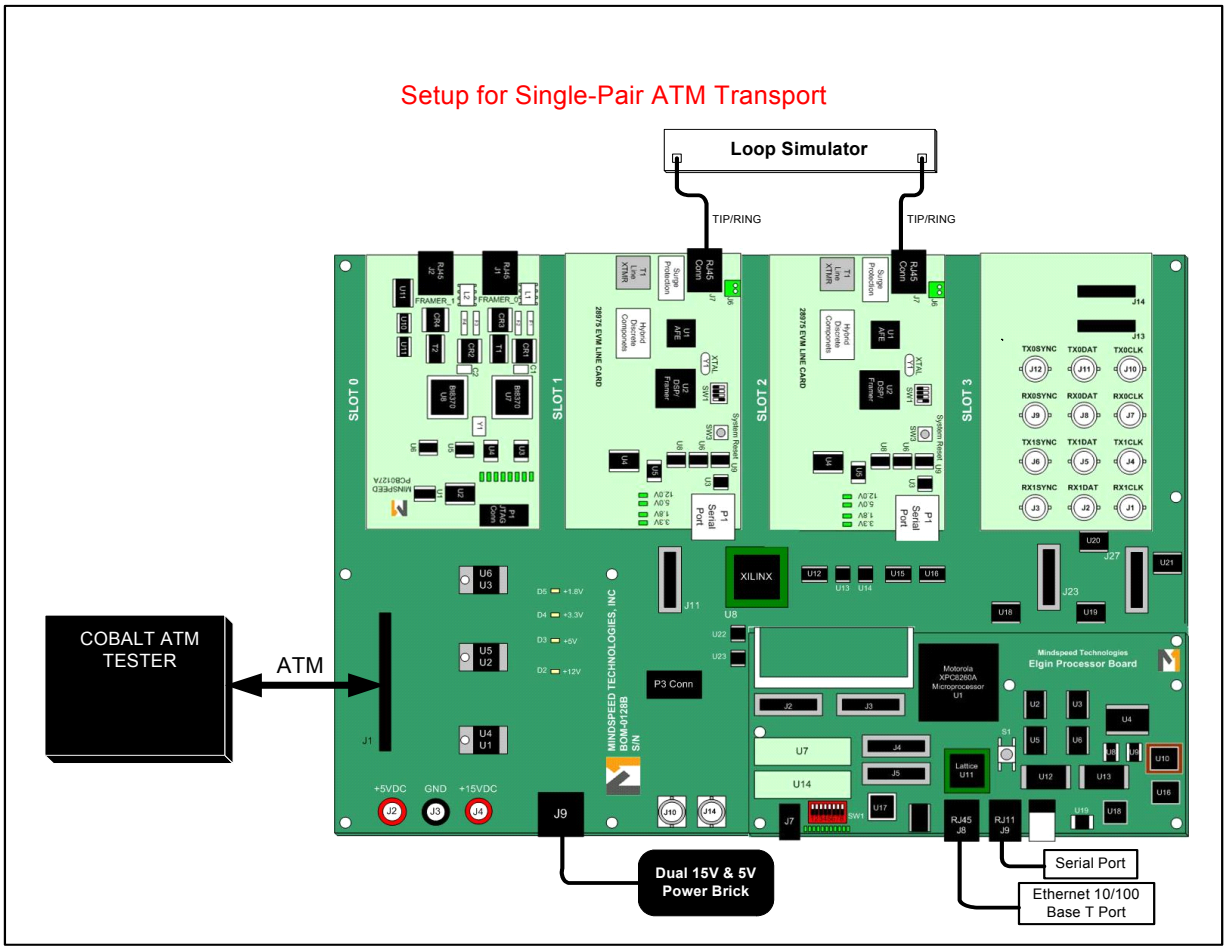
3.11 Enhanced EVM Setup for Single-pair ATM Transport .

The following steps are required for running the ZipWirePlus Enhanced EVM for Single-Pair ATM Application. This setup needs one enhanced EVM.

This configuration is valid for M28945, M28946 and M28947 devices only.

The Hardware setup for this application is shown in Figure 3-139.

Figure 3-139. Enhanced EVM Setup *Single-Pair ATM Transport Application*



3.11.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.

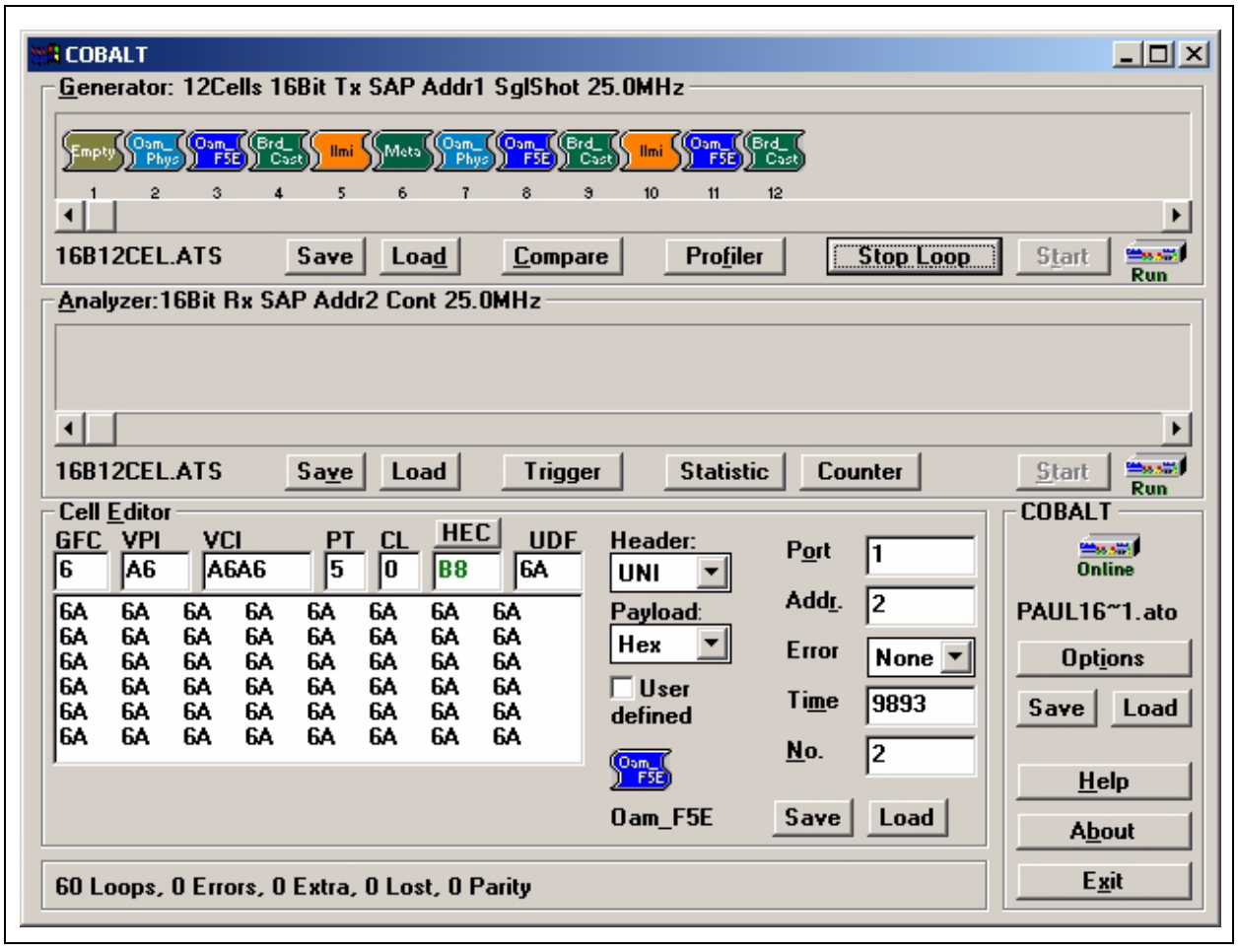
5. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. .
6. Connect the UTOPIA Header of the Cobalt ATM Utopia Emulator to the UTOPIA Test Connector J1. Both the ZipWirePlus devices are located on this UTOPIA bus. So the Cobalt ATM Tester can communicate with the UTOPIA PHYs on both the devices.
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM..

3.11.2 Cobalt ATM Setup

Configure the Cobalt ATM as follows

1. Connect the Cobalt ATM tester to the PC through the COM port.
2. Launch the Cobalt ATM GUI Application.

Figure 3-140. Cobalt ATM GUI Application - Main window

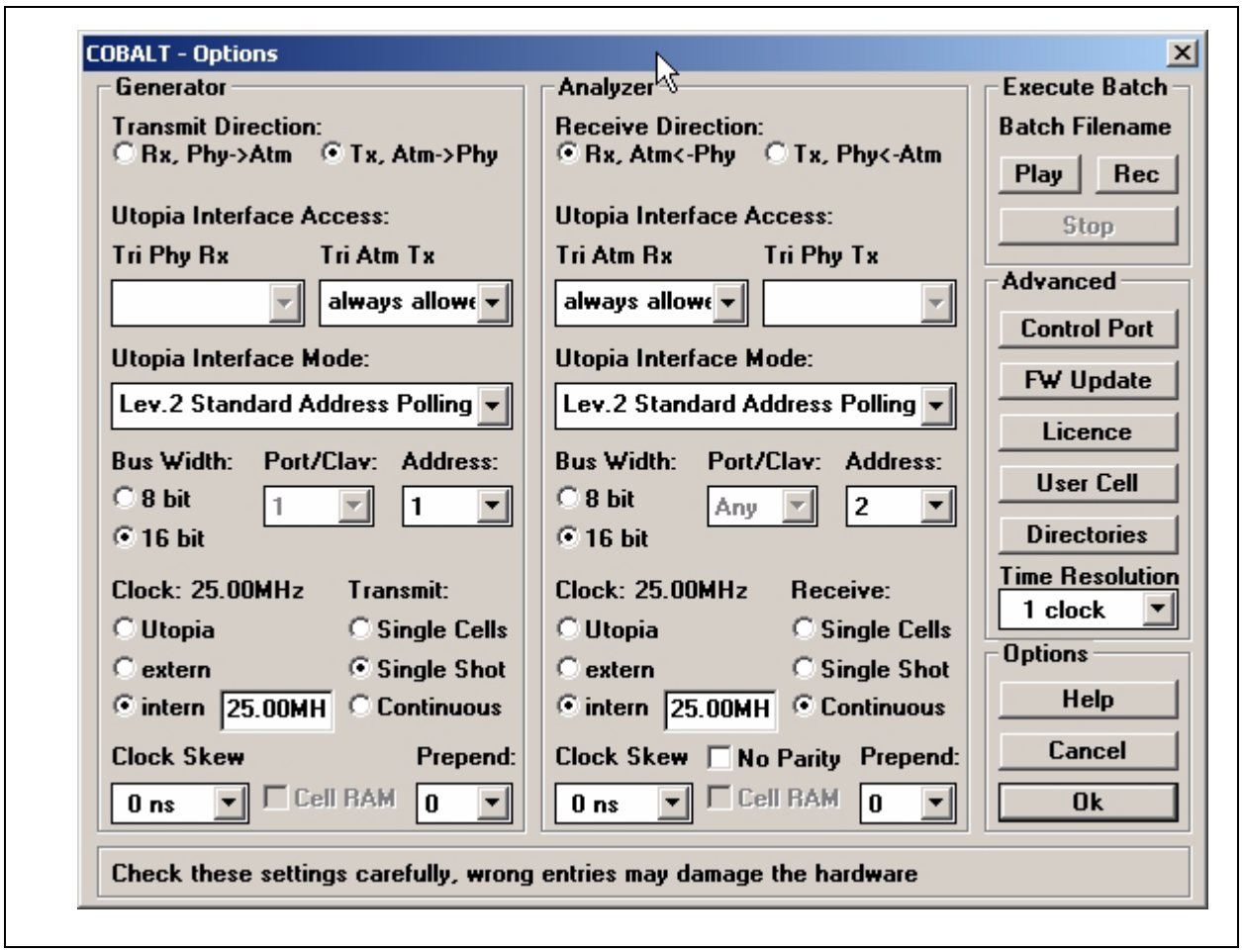


3. Click on the **Options** button.
4. Configure the GUI as defined in Figure 3-141.
   - The Transmit direction of the UTOPIA tester shall transmit to the ATM PHY of the ZipWirePlus device in Slot 1 and the receive direction of the UTOPIA

tester shall receive from the ATM PHY of the ZipWirePlus device in Slot 2.

- Configure the UTOPIA interface of the Tester as follows
  - UTOPIA Level 2
  - Bus Width - 16 bit
  - UTOPIA internal clock -25 Mhz

Figure 3-141. Cobalt ATM GUI Application - Options window



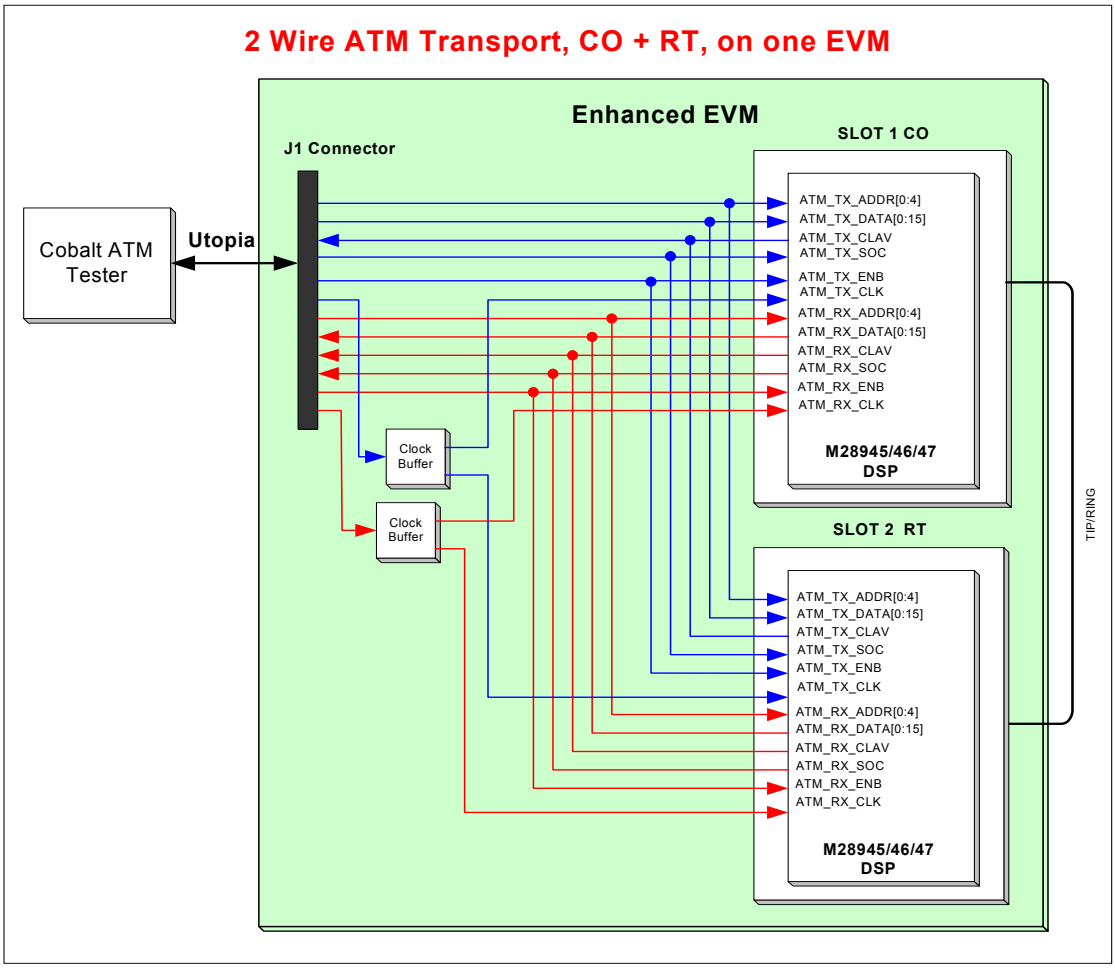
5. Configure the Generator and Analyzer of the Cobalt ATM application.

3.11.3 FPGA Configuration

The Host Code configures FPGA(U8) into one of the many possible configurations through the TestExec (UIP) GUI.

This configuration will enable the UTOPIA bus between the ZipWirePlus devices on Slot 1 & Slot 2 and the UTOPIA Connector J1. Figure 3-142 explains the pin interconnections for this application.

***Figure 3-142. Connections for** Single-Pair ATM Transport Application*



3.11.4 Enhanced EVM Configuration

3.11.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28945, M28946 or M28947 which supports ATM.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.11.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.11.5 TestExec

3.11.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the EnhancedEvm design file for the Enhanced EVM.

3.11.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

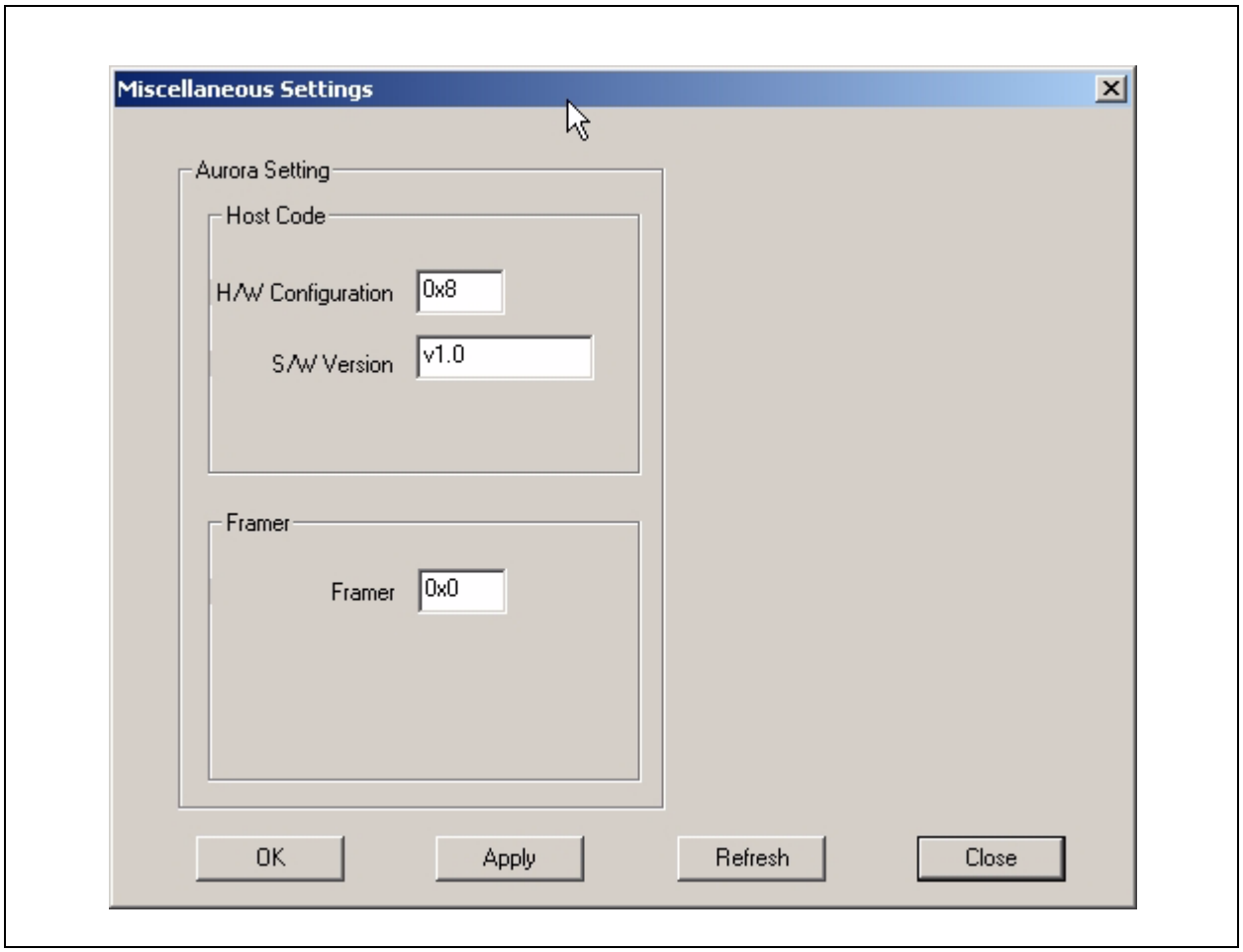
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**

3.11.5.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x8.
3. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-143. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

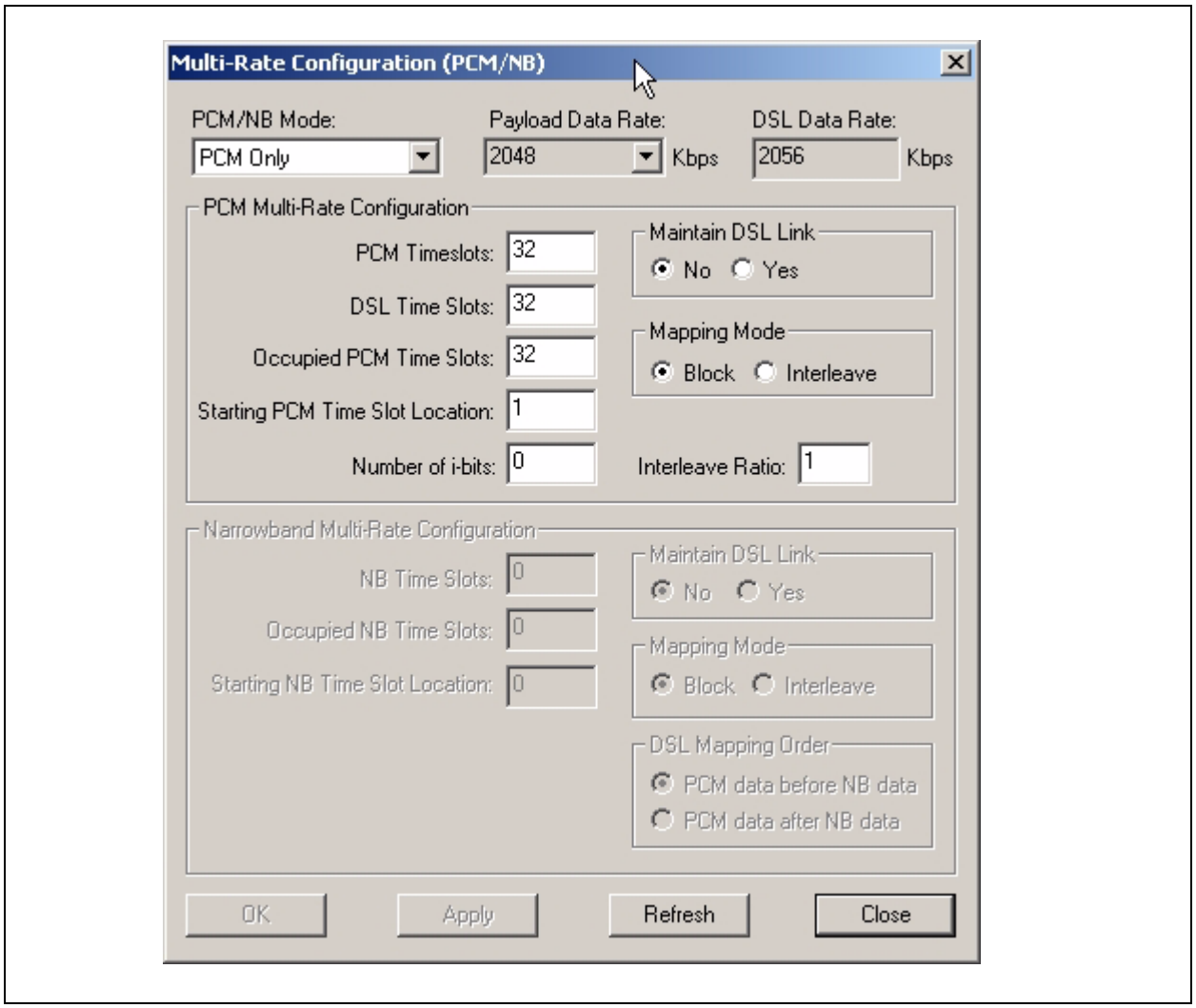


3.11.5.2.2 Slot 1 (HTU-C Side)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the Values:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

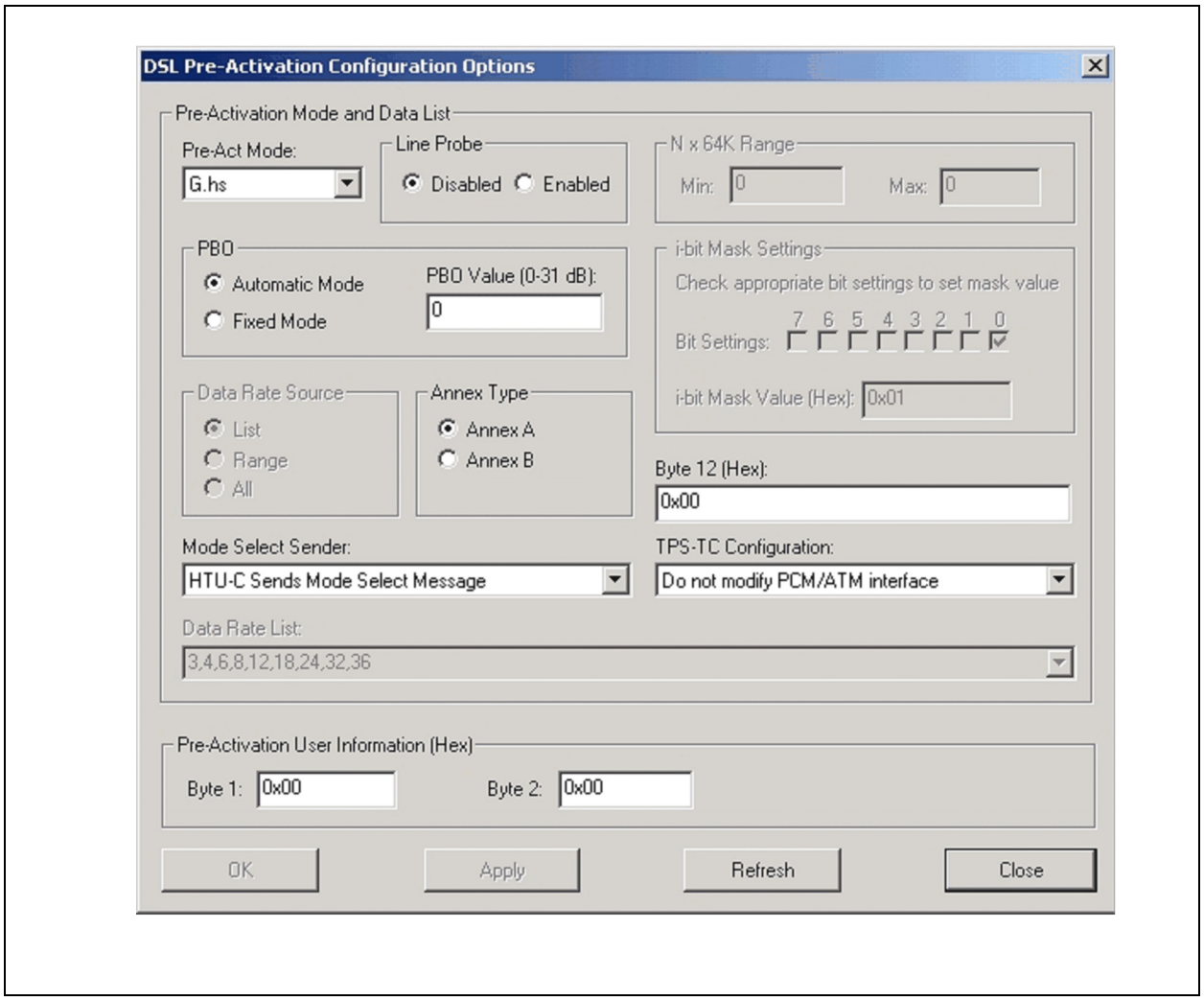
Figure 3-144. TestExec Multi-Rate Configuration for CO



Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.

5. Click on the **Pre-Activation** button.

Figure 3-145. TestExec Preactivation Configuration for CO

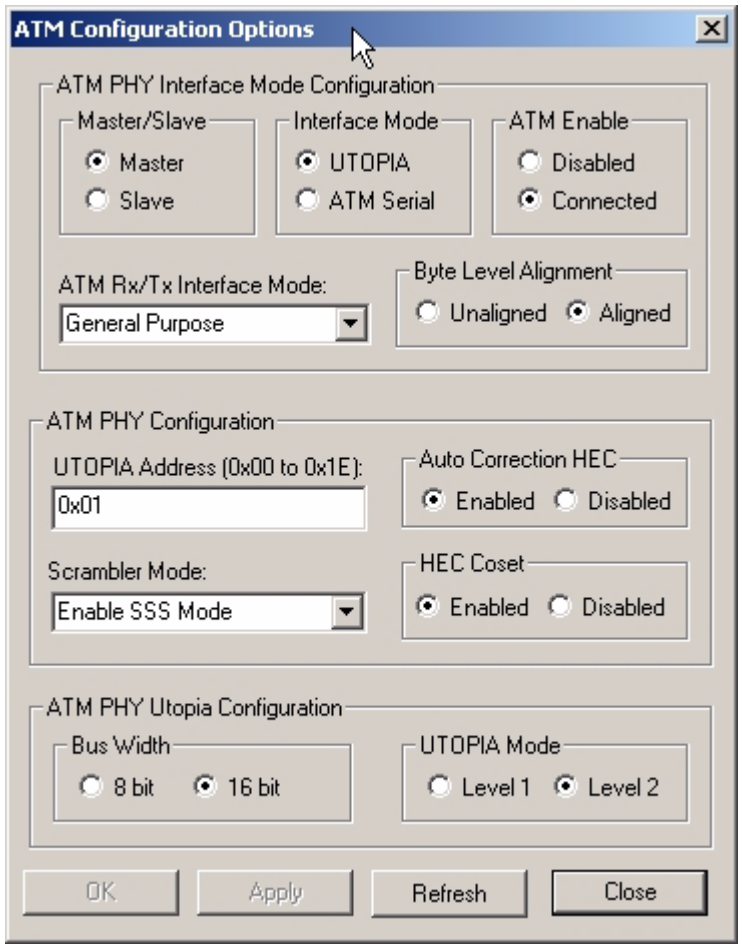


6. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
7. Click on the **Apply** button and then click on the **Close** button.
8. Click on the **ATM** button. Enter the following values.
   - ATM PHY Interface Mode Configuration
     - Master/Slave - **Master**
     - Interface Mode - **UTOPIA**
     - ATM Enable - **Connected**
     - ATM Rx/Tx Interface Mode - **General Purpose**
     - Byte Level Alignment - **Aligned**
   - ATM PHY Configuration
     - UTOPIA Address - **0x01**
     - Auto Correction HEC - **Enabled**
     - Scrambler Mode - **Enable SSS Mode**
     - HEC Closet - **Enabled**
   - ATM PHY Utopia Configuration
     - Bus Width - **16 bit**

– UTOPIA Mode - **Level 2**

9. Click on the **Apply** button and then click on the **Close** button.

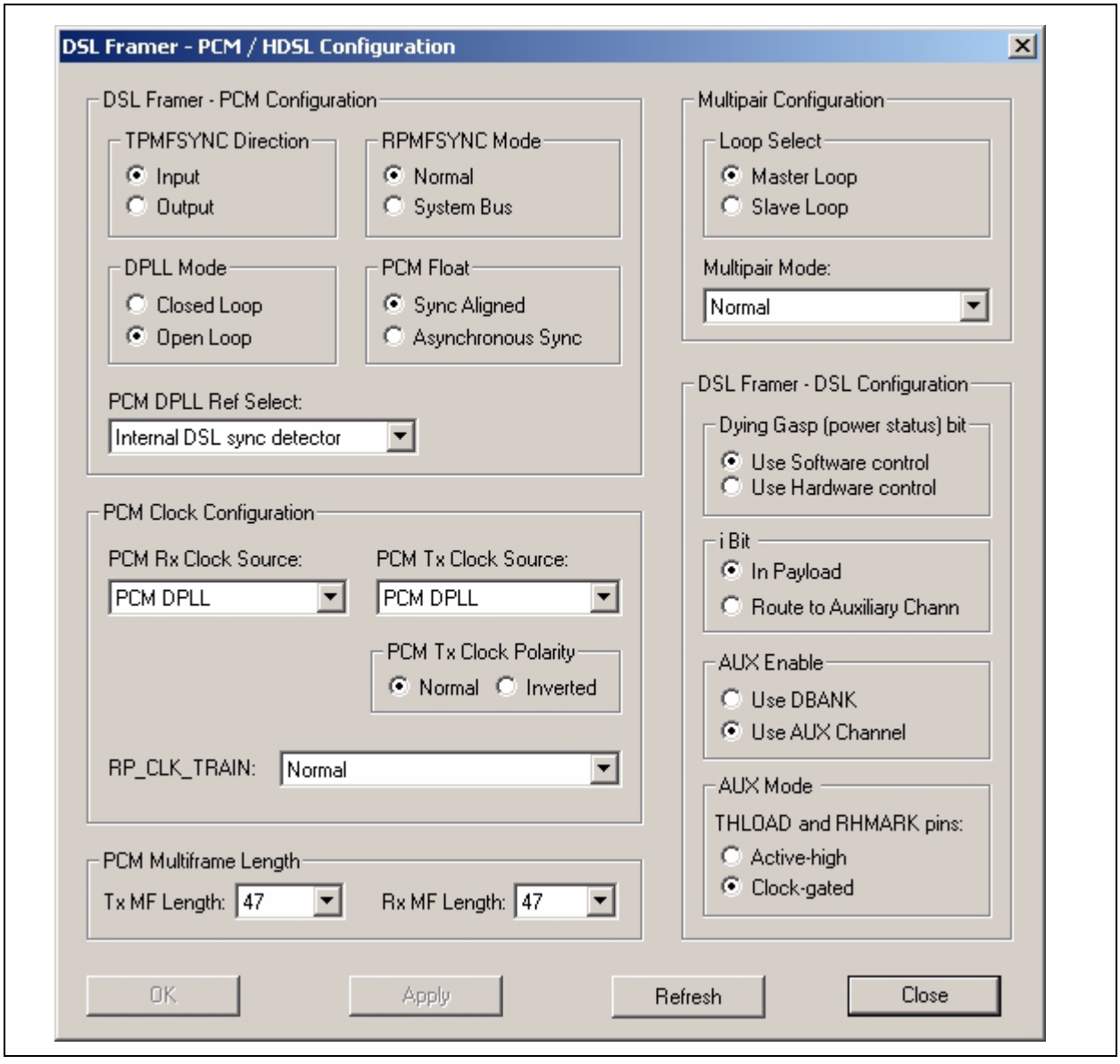
Figure 3-146. TestExec ATM Configuration for CO



10. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      – TPMFSYNC Direction - **Input**
      – RPMFSYNC Mode - **Normal**
      – DPLL Mode - **Open Loop**
      – PCM Float - **Sync Aligned**
      – PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      – PCM Rx Clock Source - **PCM DPLL**
      – PCM Tx Clock Source - **PCM DPLL**
      – PCM Tx Clock Polarity - **Normal**
      – RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length

  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use AUX channel**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

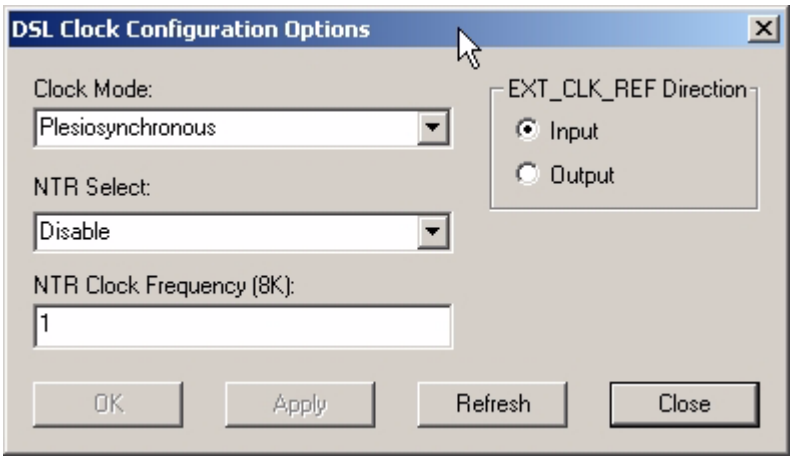
Figure 3-147. TestExec PCM/HDSL Configuration for CO



11. Click on the **Apply** button and then click on the **Close** button.

12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-148. TextExec DSL Clock Configuration for CO



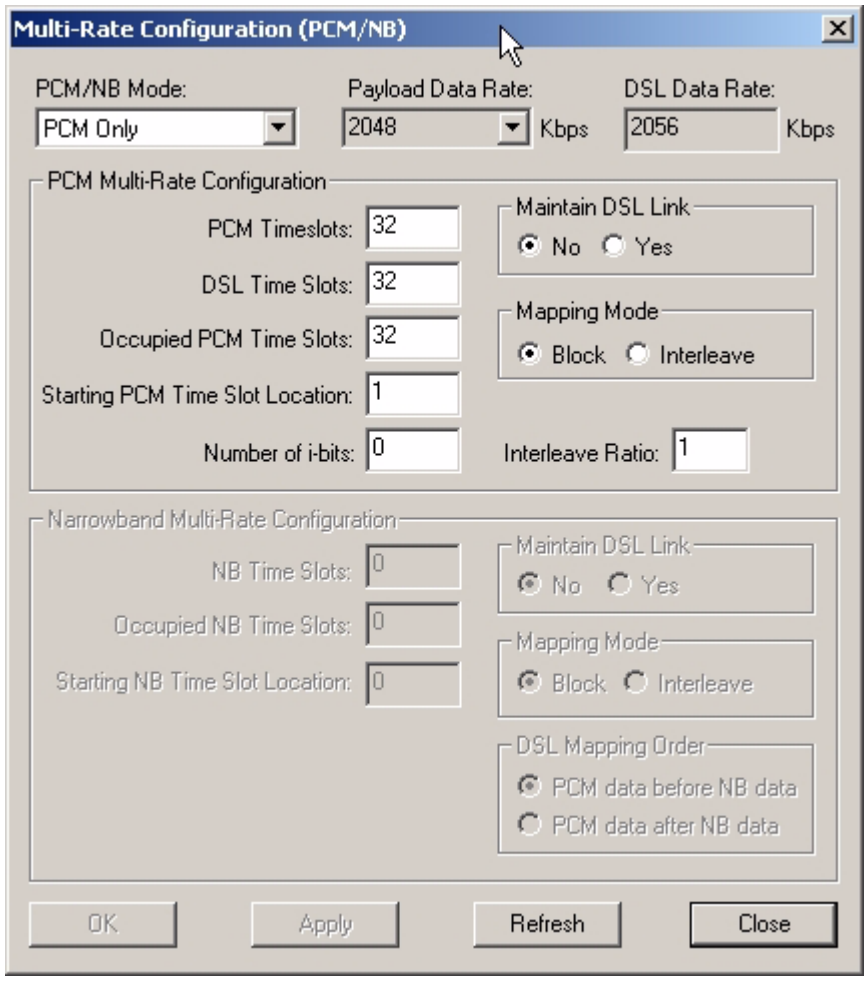
14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
15. Change to Slot 2 by right clicking the mouse button and selecting **Slot 2.**

3.11.5.2.3 Slot 2 (HTU-R Side)

1. Click on the **System Configuration** tab.
2. Set the **Terminal Type** to **HTU-R**.
3. Set the **System State** to **In-Service**.
4. Click on **Multi-Rate Button**.
5. Enter the values:

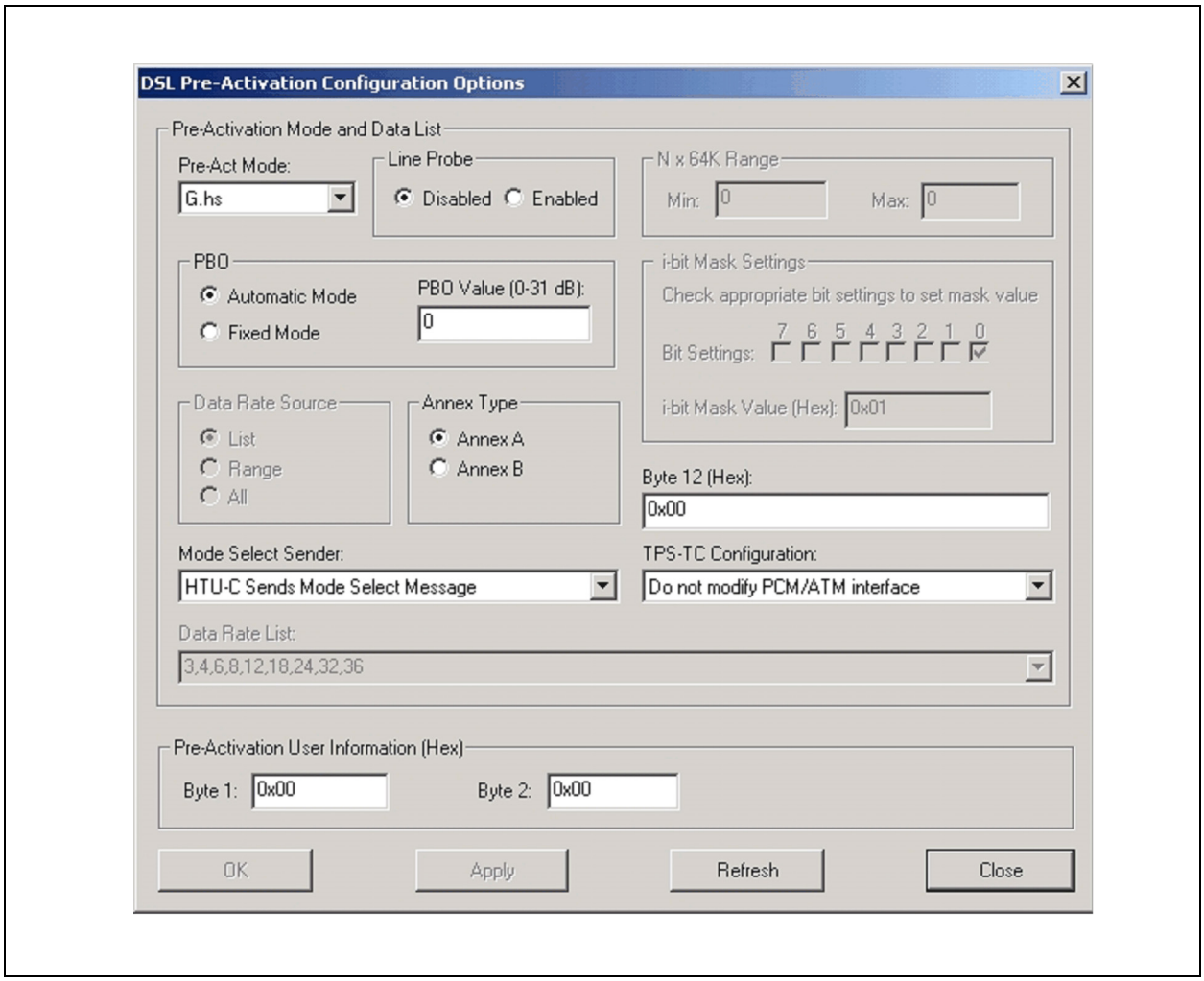
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-149. TestExec Multi Rate Configuration for RT



6. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

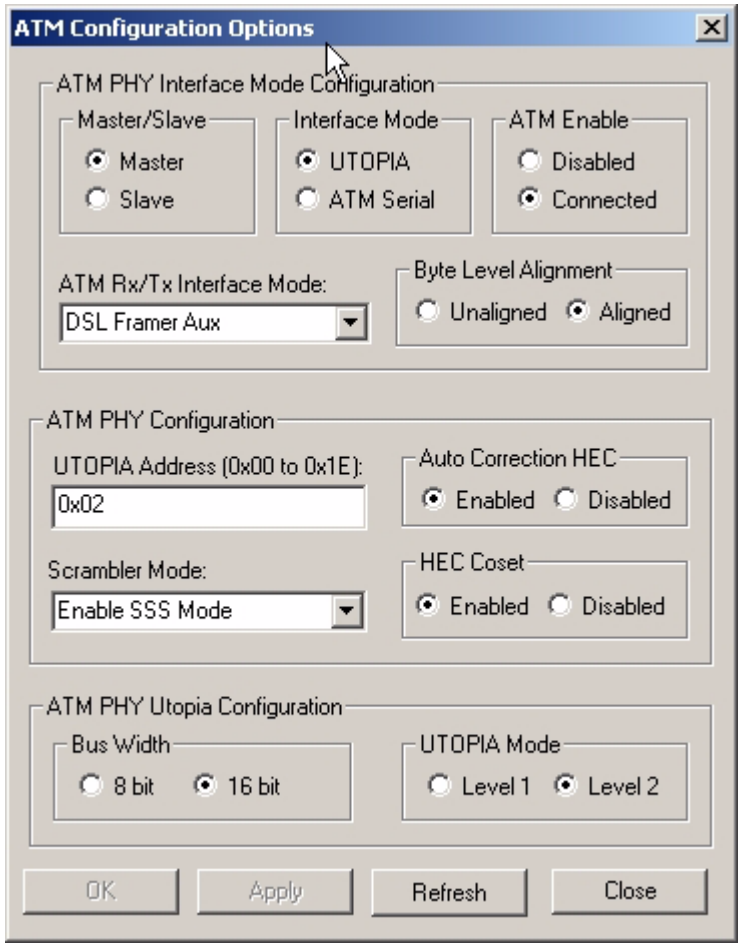
Figure 3-150. TestExec Preactivation Configuration for RT



8. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **ATM** button. Enter the following values.
    - ATM PHY Interface Mode Configuration
      - Master/Slave - **Master**
      - Interface Mode - **UTOPIA**
      - ATM Enable - **Connected**
      - ATM Rx/Tx Interface Mode - **General Purpose**
      - Byte Level Alignment - **Aligned**
    - ATM PHY Configuration
      - UTOPIA Address - **0x02**
      - Auto Correction HEC - **Enabled**
      - Scrambler Mode - **Enable SSS Mode**
      - HEC Closet - **Enabled**
    - ATM PHY Utopia Configuration
      - Bus Width - **16 bit**
      - UTOPIA Mode - **Level 2**

11. Click on the **Apply** button and then click on the **Close** button.

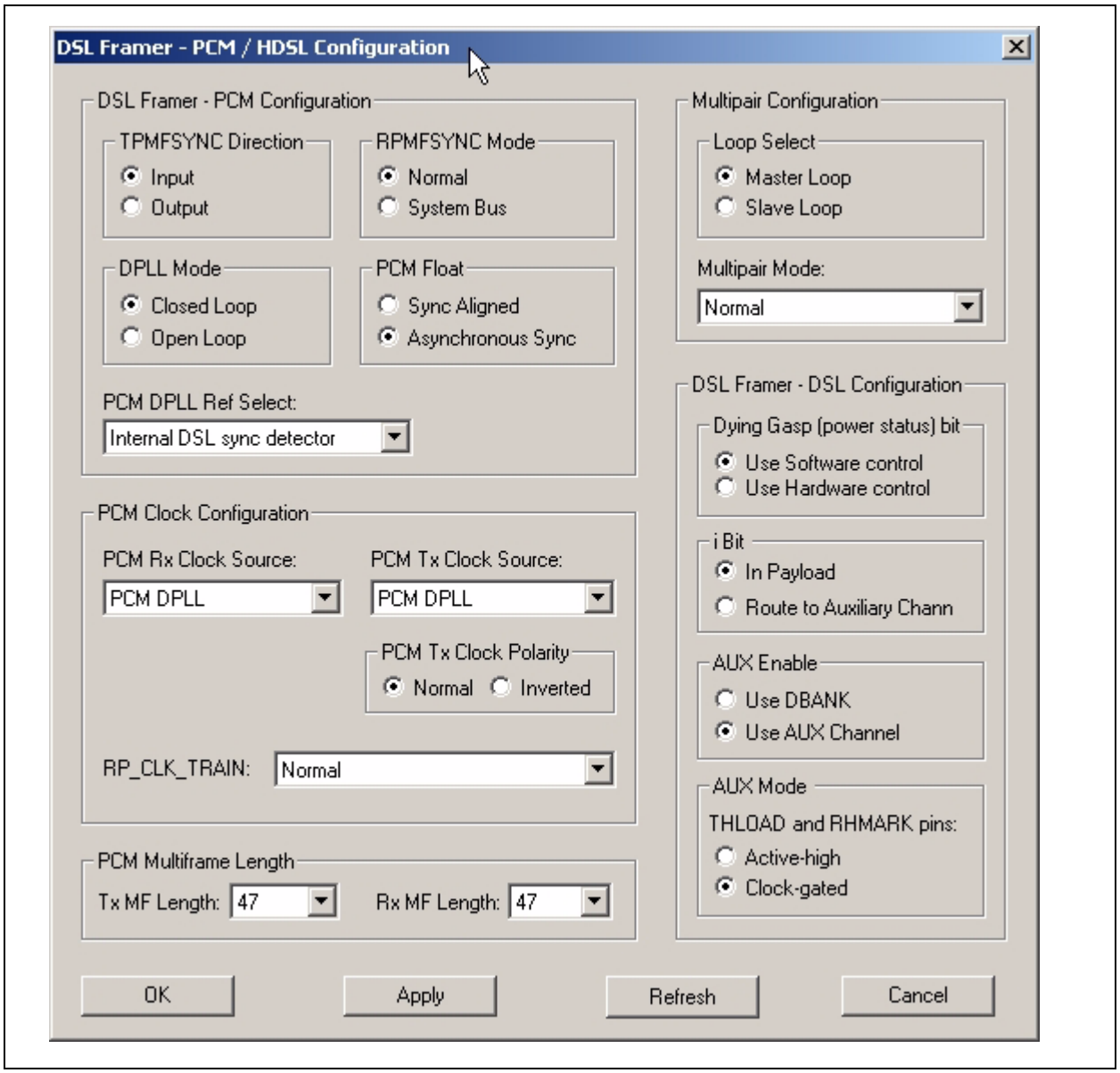
Figure 3-151. TestExec ATM Configuration for RT



12. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      - TPMFSYNC Direction - **Input**
      - RPMFSYNC Mode - **Normal**
      - DPLL Mode - **Closed Loop**
      - PCM Float - **Sync Aligned**
      - PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      - PCM Rx Clock Source - **PCM DPLL**
      - PCM Tx Clock Source - **PCM DPLL**
      - PCM Tx Clock Polarity - **Normal**
      - RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length
      - Tx MF Length - **47**

  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use AUX Channel**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

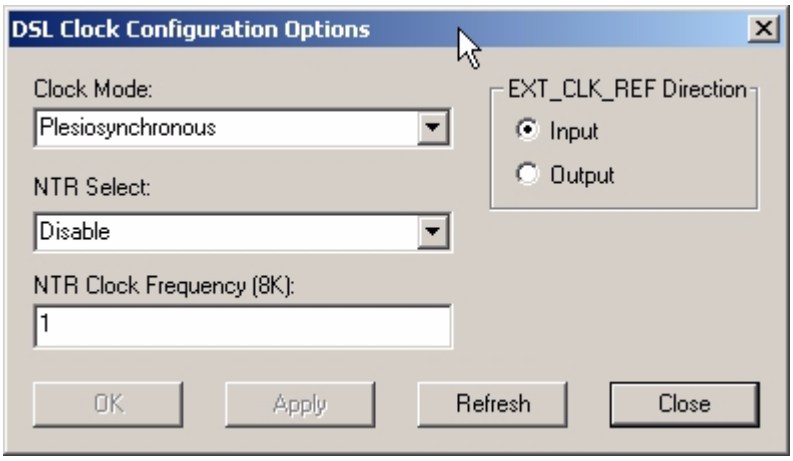
Figure 3-152. TestExec PCM/HDSL Configuration for RT



13. Click the **Apply** button and then click on the **Close** button.

14. Click on the **DSL Clock** Button.
15. Enter the following values:

Figure 3-153. TextExec DSL Clock Configuration for RT



16. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.11.5.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.
6. Go to the Cobalt ATM GUI. Click on the **Active Loop** button.
7. Verify that the Tester is running errorfree.

3.11.5.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-139. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.12 Enhanced EVM Setup for Single-pair ATM and PCM Transport .

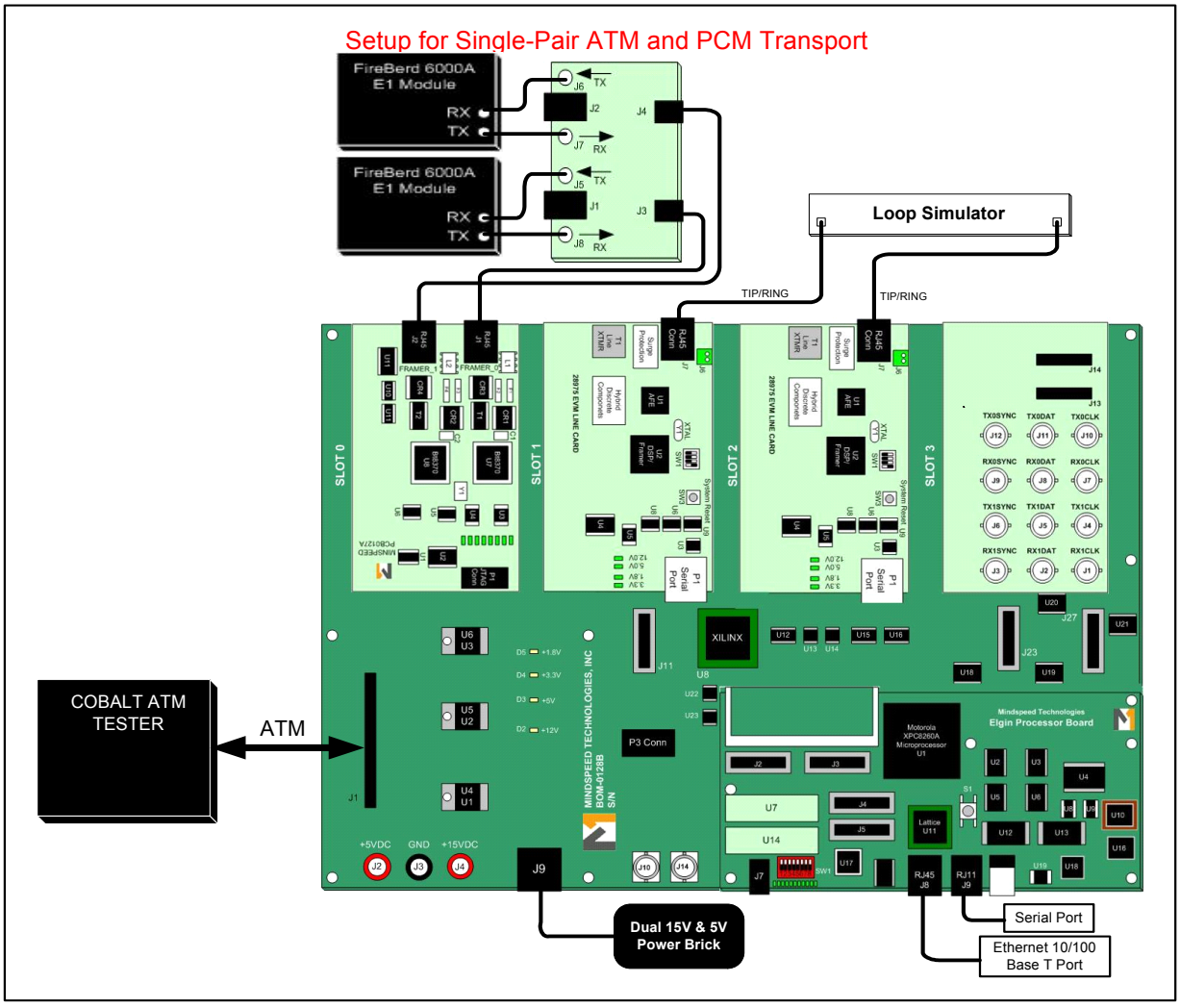
The following steps are required for running the ZipWirePlus Enhanced EVM for Single-Pair ATM and E1 Transport Application. This setup needs one enhanced EVM.

This configuration is valid for M28945, M28946 and M28947 devices only.

The Hardware setup for this application is shown in Figure 3-154.

NOTE: The Fireberd must be equipped with a 2M/ nX64 interface (E1 Module) to proceed with the setup described in this section. Figure 3-154 illustrates the required interconnections.

Figure 3-154. Enhanced EVM Setup *Single-Pair ATM and E1 Transport Application*



3.12.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the Dual T1/E1 Framer Line Card is plugged into Slot 0, and the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. .
6. Fireberd Connections -
   - Fireberd #1 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_0 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-C card.
   - Fireberd #2 - Connect the Fireberd's XMTR & RCVR ports to the RJ-45 port FRAMER_1 on the Dual T1/E1 card using the T1/E1 Cable Adapter . This port shall feed PCM data into the HTU-R card.
7. Connect the UTOPIA Header of the Cobalt ATM Utopia Emulator to the UTOPIA Test Connector J1. Both the ZipWirePlus devices are located on this UTOPIA bus. So the Cobalt ATM Tester can communicate with the UTOPIA PHYs on both the devices.
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.12.2 Fireberd Setup

Configure the Fireberd #1 E1 Module front panel as follows:

- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kHz
- INTF SETUP: 2M/n64: CONFIG: FRAME = FRAMED, CRC4 = OFF, TS 16 = OFF
- INTF SETUP: 2M/n64: MODE: nX64:TS01 : RX/TX,
- INTF SETUP: 2M/n64: MODE: nX64:TS01 : RX/TX, TS01 : RX/TX, TS02 : RX/TX, TS03 : RX/TX, TS04 : RX/TX, TS05 : RX/TX, TS06 : RX/TX, TS07 : RX/TX, TS08 : RX/TX, TS09 : RX/TX, TS01 : RX/TX, TS10 : RX/TX, TS11 : RX/TX, TS12 : RX/TX, TS13 : RX/TX, TS14 : RX/TX, TS15 : RX/TX
- Configure the Fireberd #2 E1 Module front panel the same way as above.

3.12.3 Cobalt ATM Setup

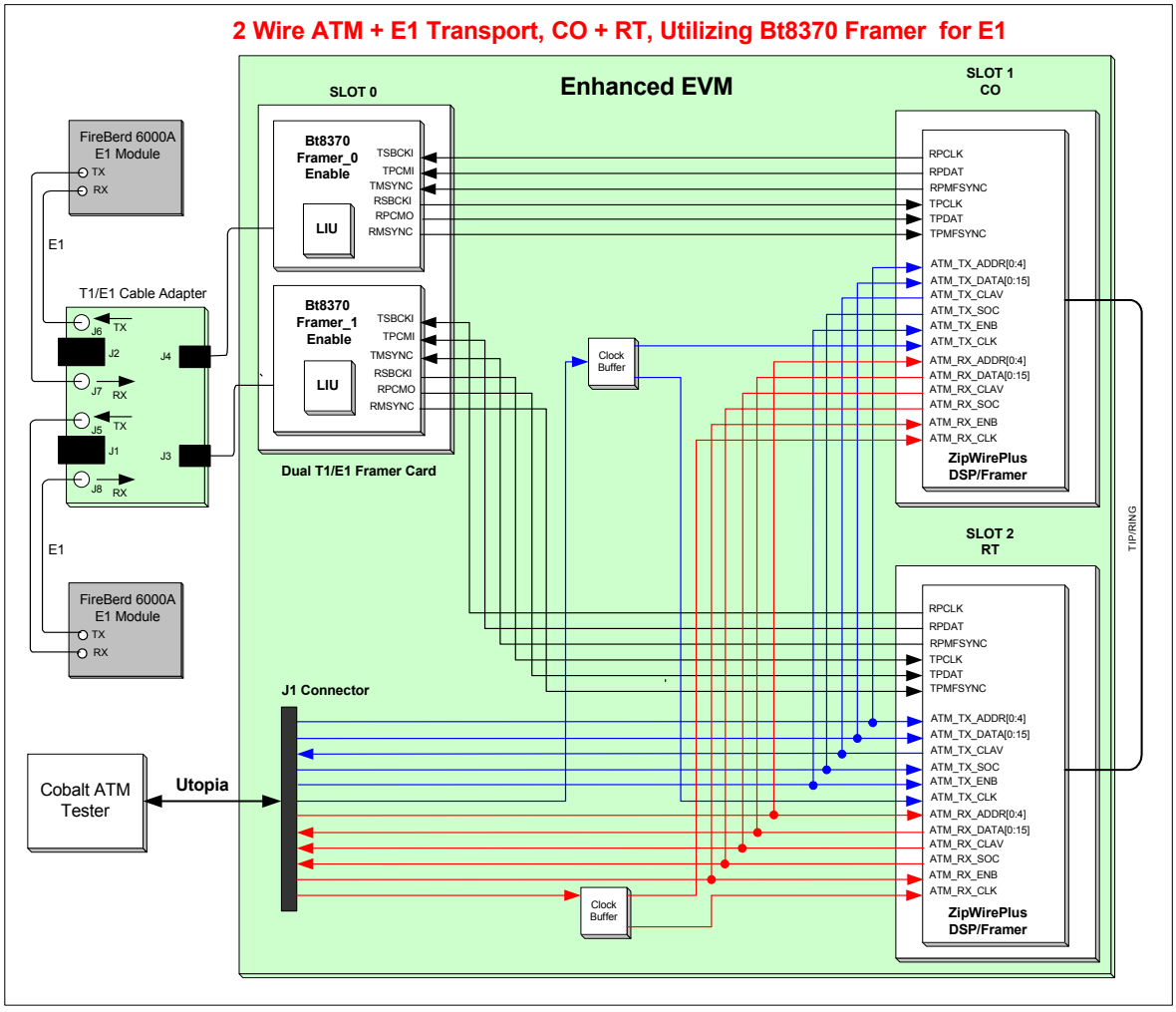
Please refer to Section 3.11.2.

3.12.4 FPGA Configuration

The Host Code configures FPGA(U8) into one of the many possible configurations through the TestExec (UIP) GUI.

This configuration will connect the PCM bus of the ZipWirePlus device (slot 1) to the Framer #0 (slot 0) and the PCM bus of the ZipWirePlus device (slot 2) to the Framer #1 (slot 0). In addition it will enable the UTOPIA bus between the ZipWirePlus devices on Slot 1 & Slot 2 and the UTOPIA Connector J1. Figure 3-155 explains the pin interconnections for this application.

***Figure 3-155. Connections for** Single-Pair ATM and E1 Transport Application*



3.12.5 Enhanced EVM Configuration

3.12.5.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- firmware image for the M28945, M28946 or M28947 which supports ATM.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.12.5.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.12.6 TestExec

3.12.6.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the EnhancedEvm design file for the Enhanced EVM.

3.12.6.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

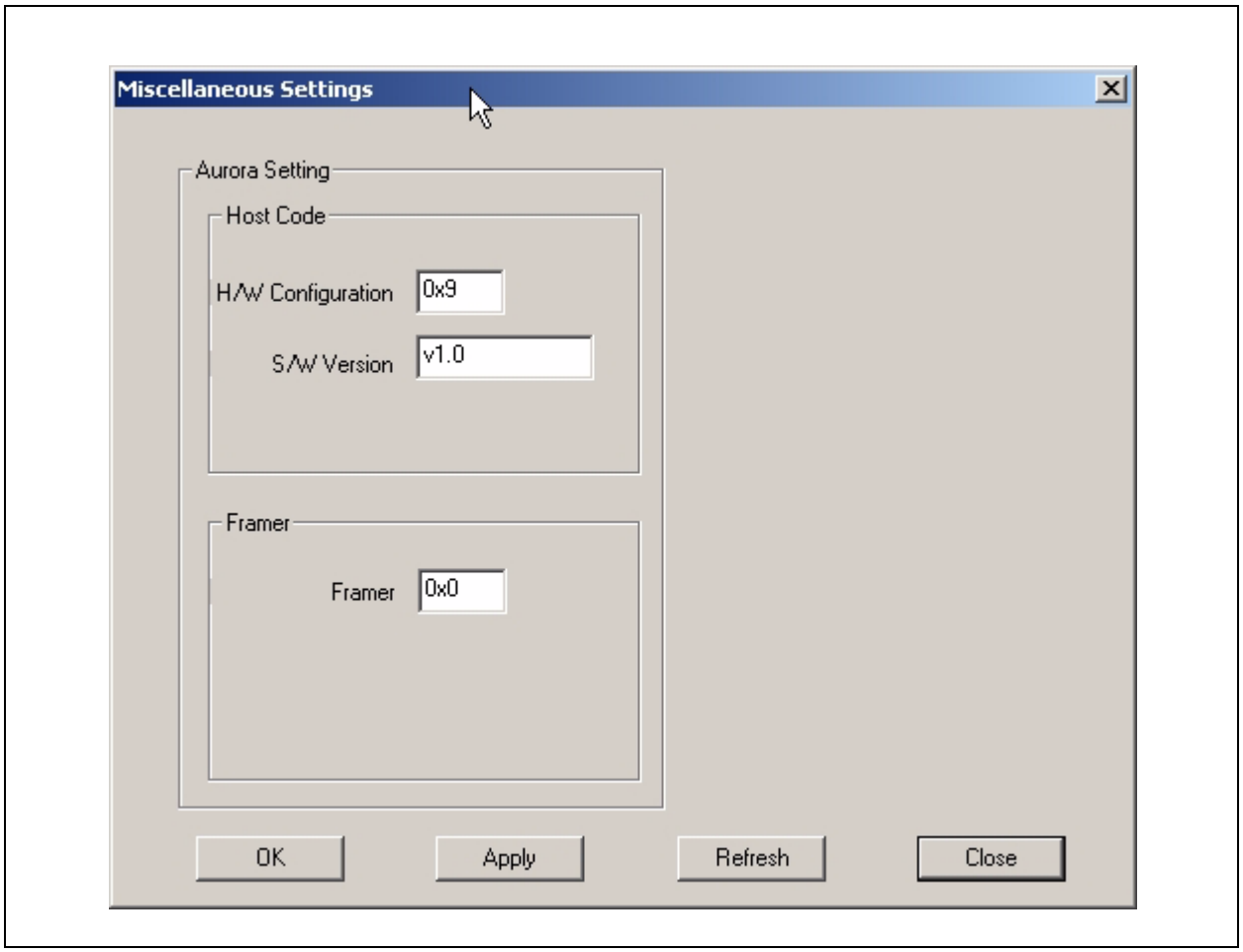
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**

3.12.6.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x9.
3. Enter the **Framer** value to be 0x0.This configures the T1/E1 Framer for the E1 Mode.

Figure 3-156. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

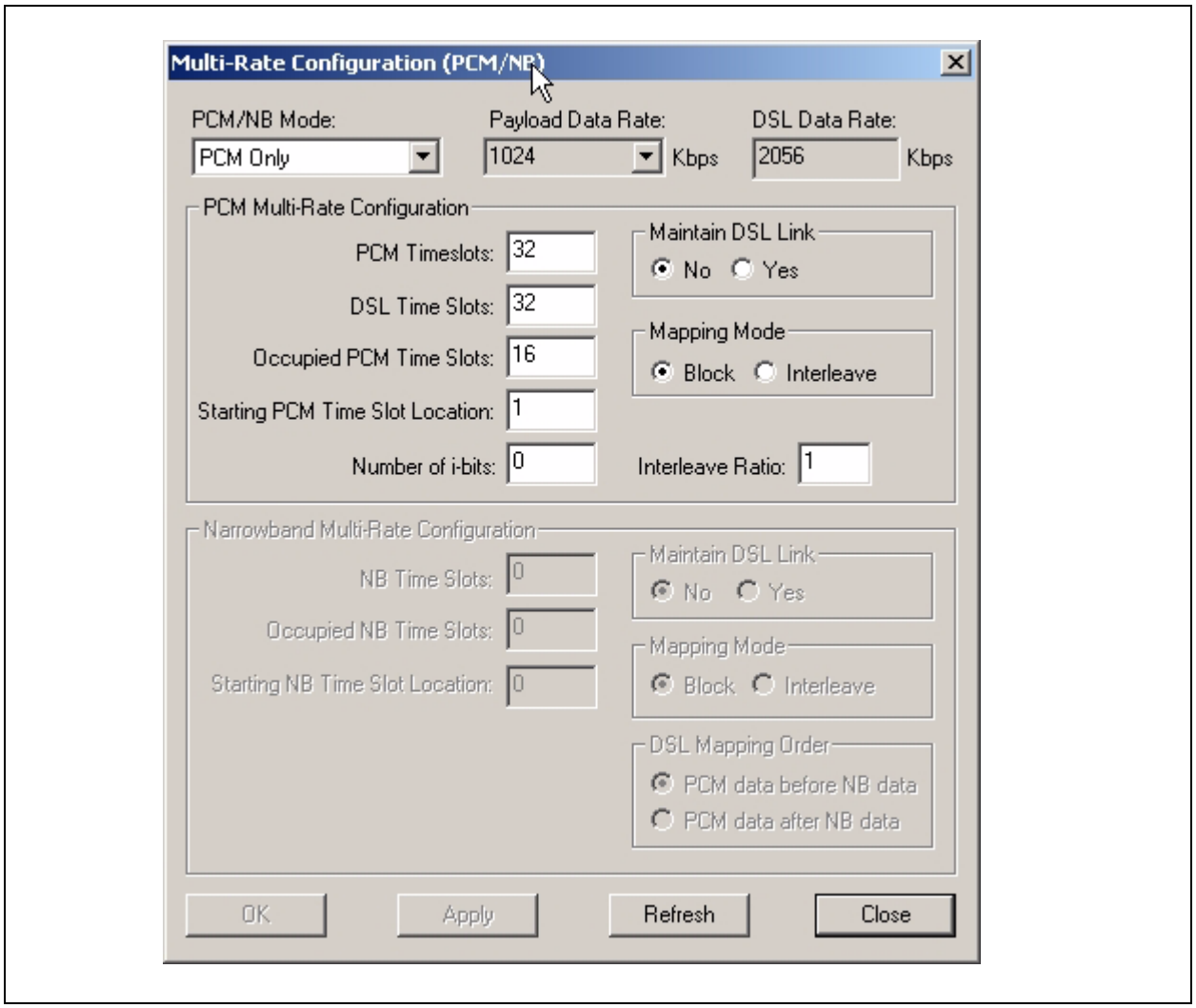


3.12.6.2.2 Slot 1 (HTU-C Side)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the Values:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

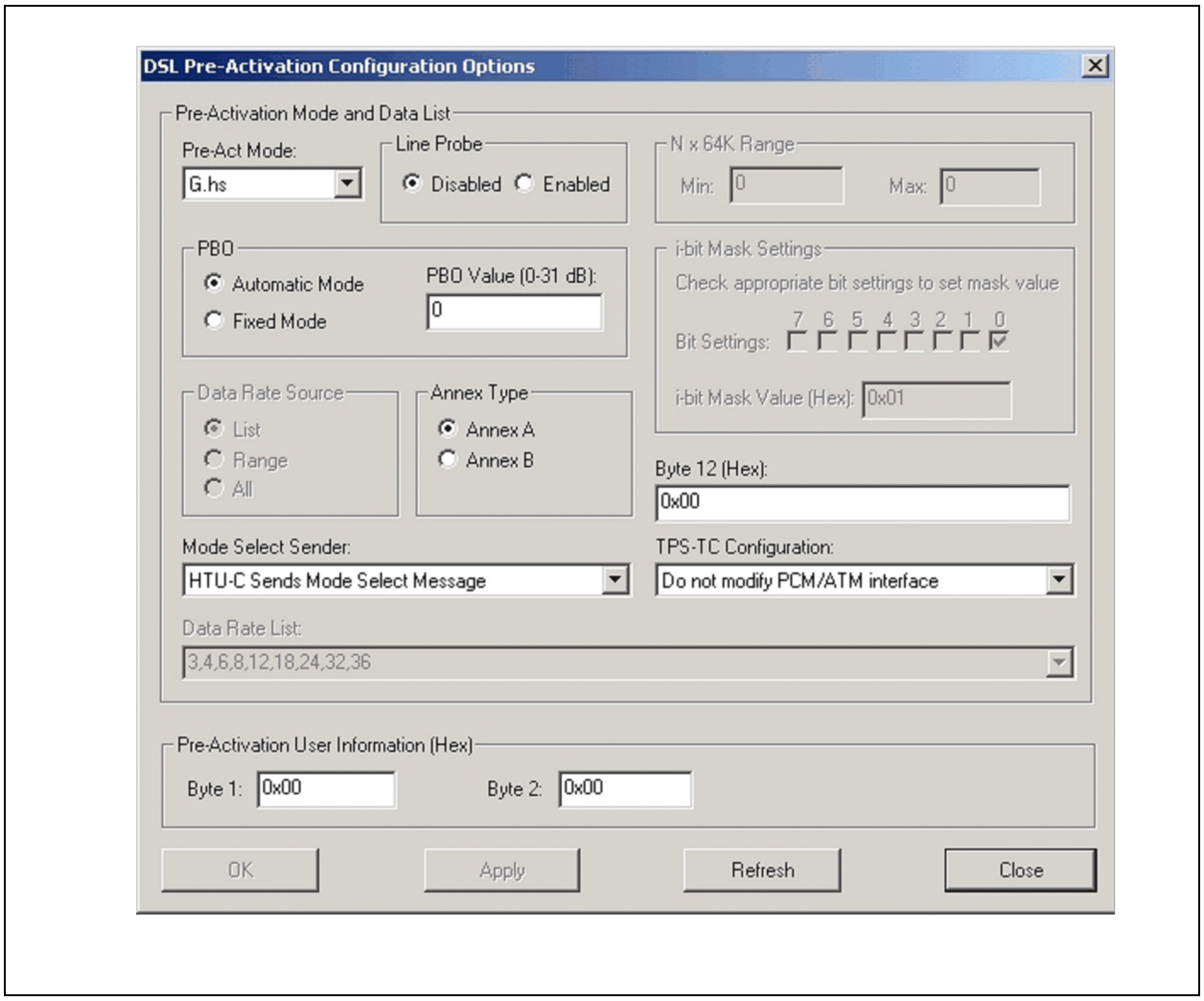
Figure 3-157. TestExec Multi-Rate Configuration for CO



Click the **Apply** button. The Payload Data Rate will change to 1024 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.

5. Click on the **Pre-Activation** button.

Figure 3-158. TestExec Preactivation Configuration for CO

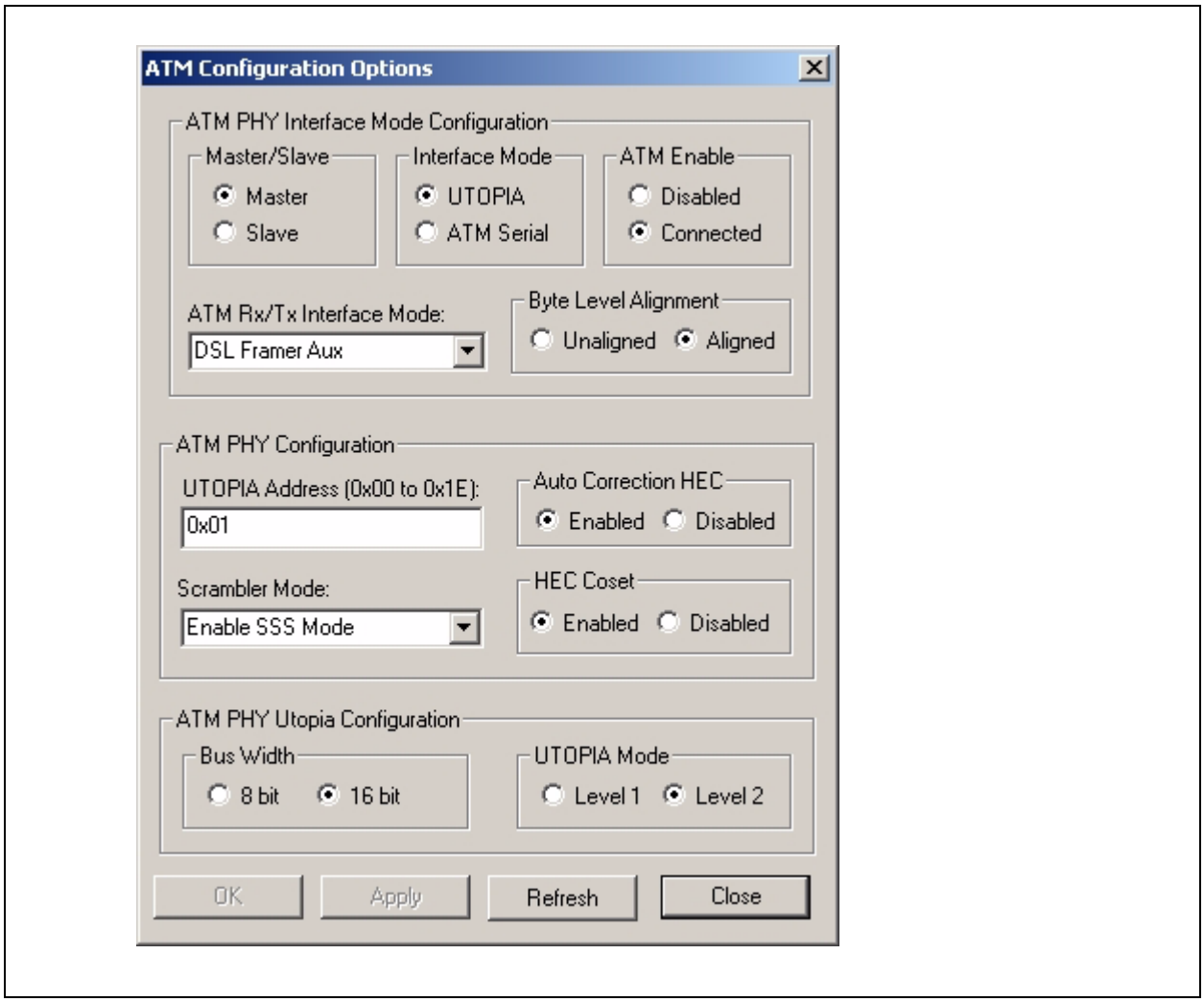


6. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
7. Click on the **Apply** button and then click on the **Close** button.
8. Click on the **ATM** button. Enter the following values.
   - ATM PHY Interface Mode Configuration
     - Master/Slave - **Master**
     - Interface Mode - **UTOPIA**
     - ATM Enable - **Connected**
     - ATM Rx/Tx Interface Mode - **DSL Framer Aux**
     - Byte Level Alignment - **Aligned**
   - ATM PHY Configuration
     - UTOPIA Address - **0x01**
     - Auto Correction HEC - **Enabled**
     - Scrambler Mode - **Enable SSS Mode**
     - HEC Closet - **Enabled**
   - ATM PHY Utopia Configuration
     - Bus Width - **16 bit**

– UTOPIA Mode - **Level 2**

9. Click on the **Apply** button and then click on the **Close** button.

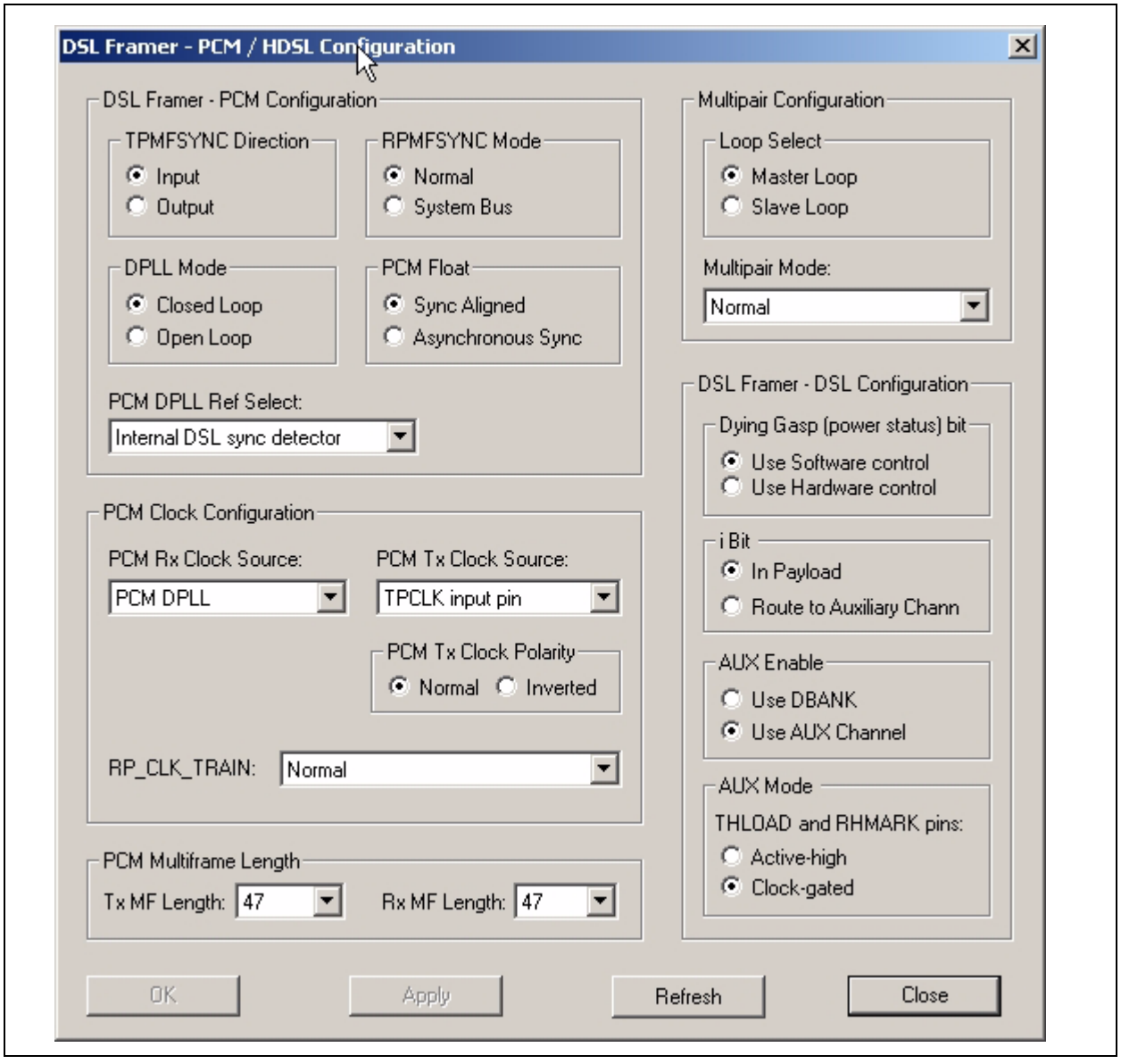
Figure 3-159. TestExec ATM Configuration for CO



10. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      – TPMFSYNC Direction - **Input**
      – RPMFSYNC Mode - **Normal**
      – DPLL Mode - **Closed Loop**
      – PCM Float - **Sync Aligned**
      – PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      – PCM Rx Clock Source - **PCM DPLL**
      – PCM Tx Clock Source - **TPCLK Input**
      – PCM Tx Clock Polarity - **Normal**
      – RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length

  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use AUX channel**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

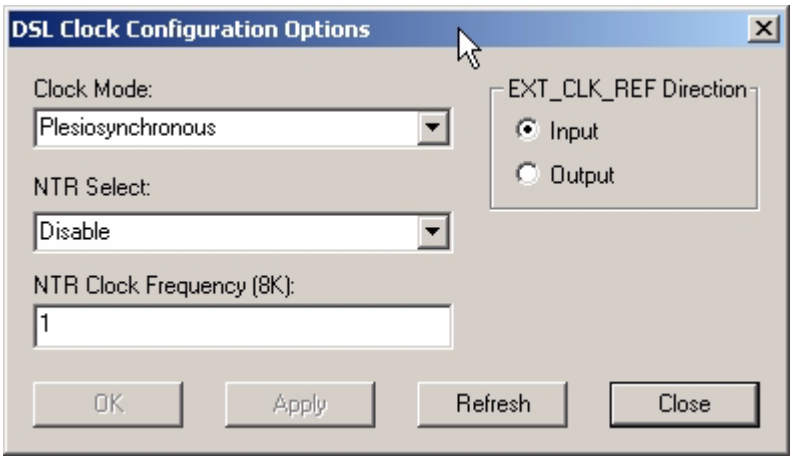
Figure 3-160. TestExec PCM/HDSL Configuration for CO



11. Click on the **Apply** button and then click on the **Close** button.

12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-161. TextExec DSL Clock Configuration for CO



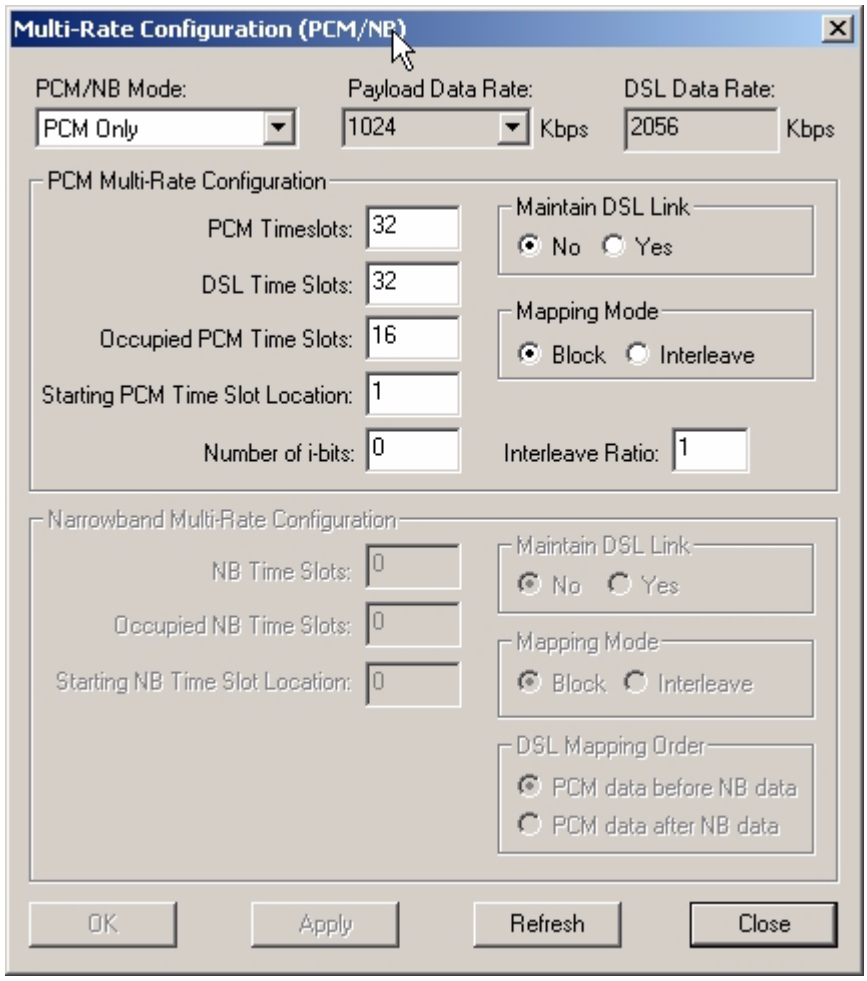
14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
15. Change to Slot 2 by right clicking the mouse button and selecting **Slot 2.**

3.12.6.2.3 Slot 2 (HTU-R Side)

1. Click on the **System Configuration** tab.
2. Set the **Terminal Type** to **HTU-R**.
3. Set the **System State** to **In-Service**.
4. Click on **Multi-Rate Button**.
5. Enter the values:

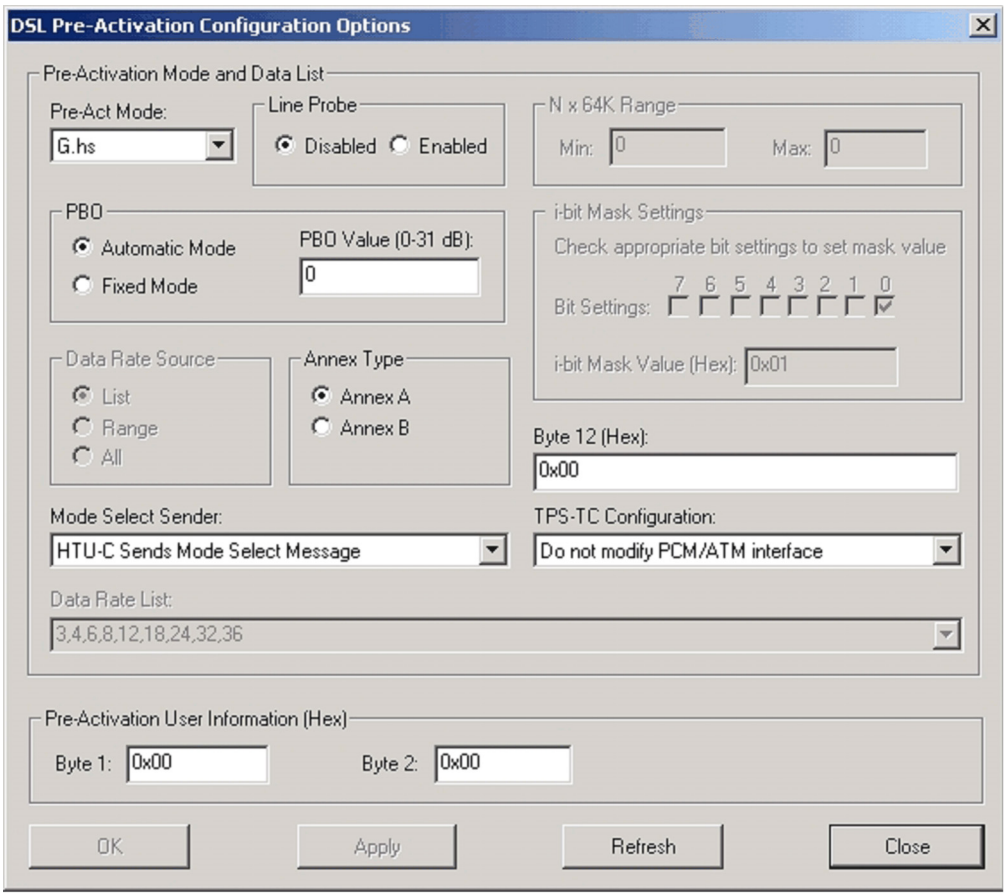
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied PCM Time Slots - **16**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-162. TestExec Multi Rate Configuration for RT



6. Click the **Apply** button. The **Payload Data Rate** will change to 1024 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

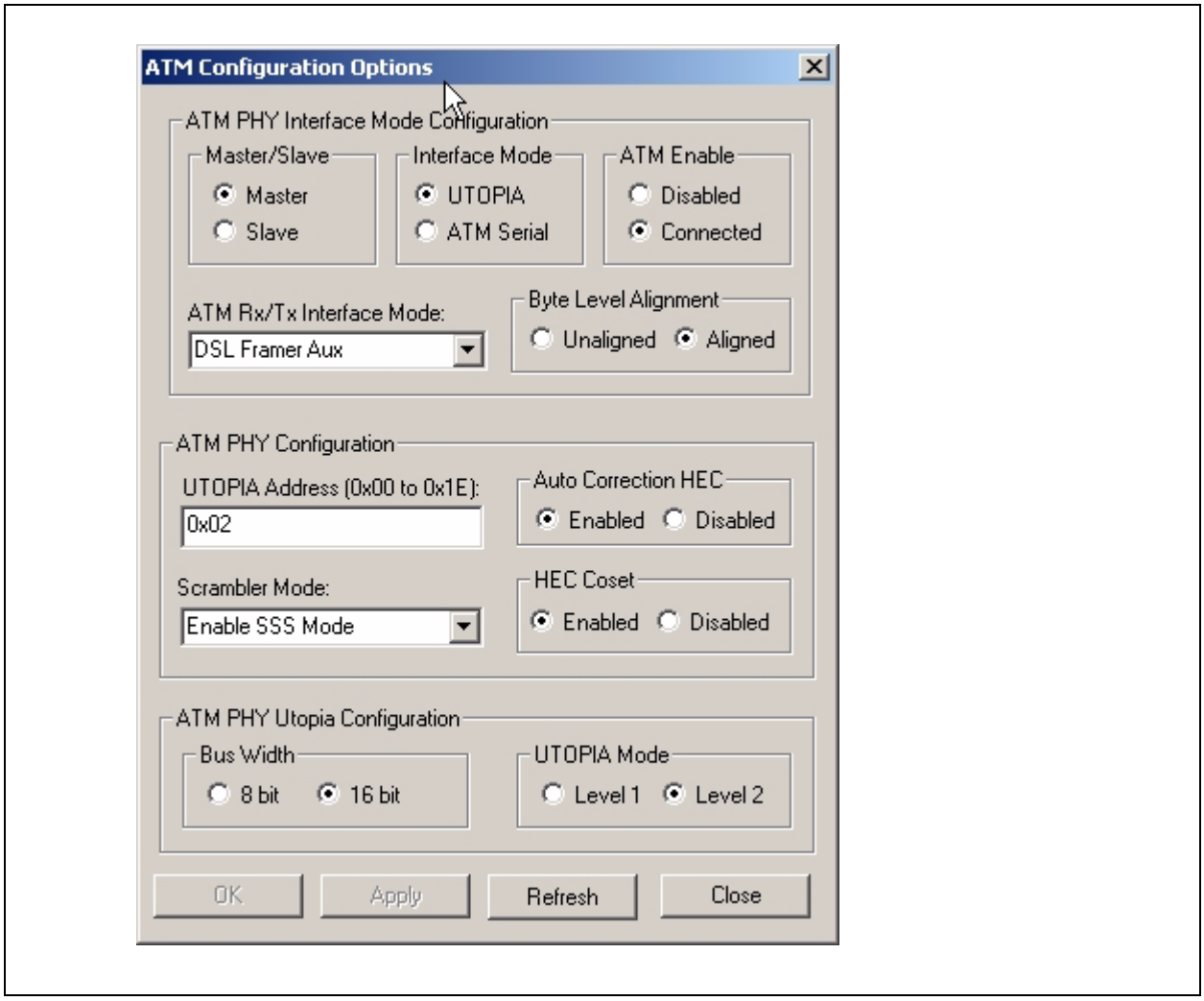
Figure 3-163. TestExec Preactivation Configuration for RT



8. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **ATM** button. Enter the following values.
    - ATM PHY Interface Mode Configuration
      - Master/Slave - **Master**
      - Interface Mode - **UTOPIA**
      - ATM Enable - **Connected**
      - ATM Rx/Tx Interface Mode - **DSL Framer Aux**
      - Byte Level Alignment - **Aligned**
    - ATM PHY Configuration
      - UTOPIA Address - **0x02**
      - Auto Correction HEC - **Enabled**
      - Scrambler Mode - **Enable SSS Mode**
      - HEC Closet - **Enabled**
    - ATM PHY Utopia Configuration
      - Bus Width - **16 bit**
      - UTOPIA Mode - **Level 2**

11. Click on the **Apply** button and then click on the **Close** button.

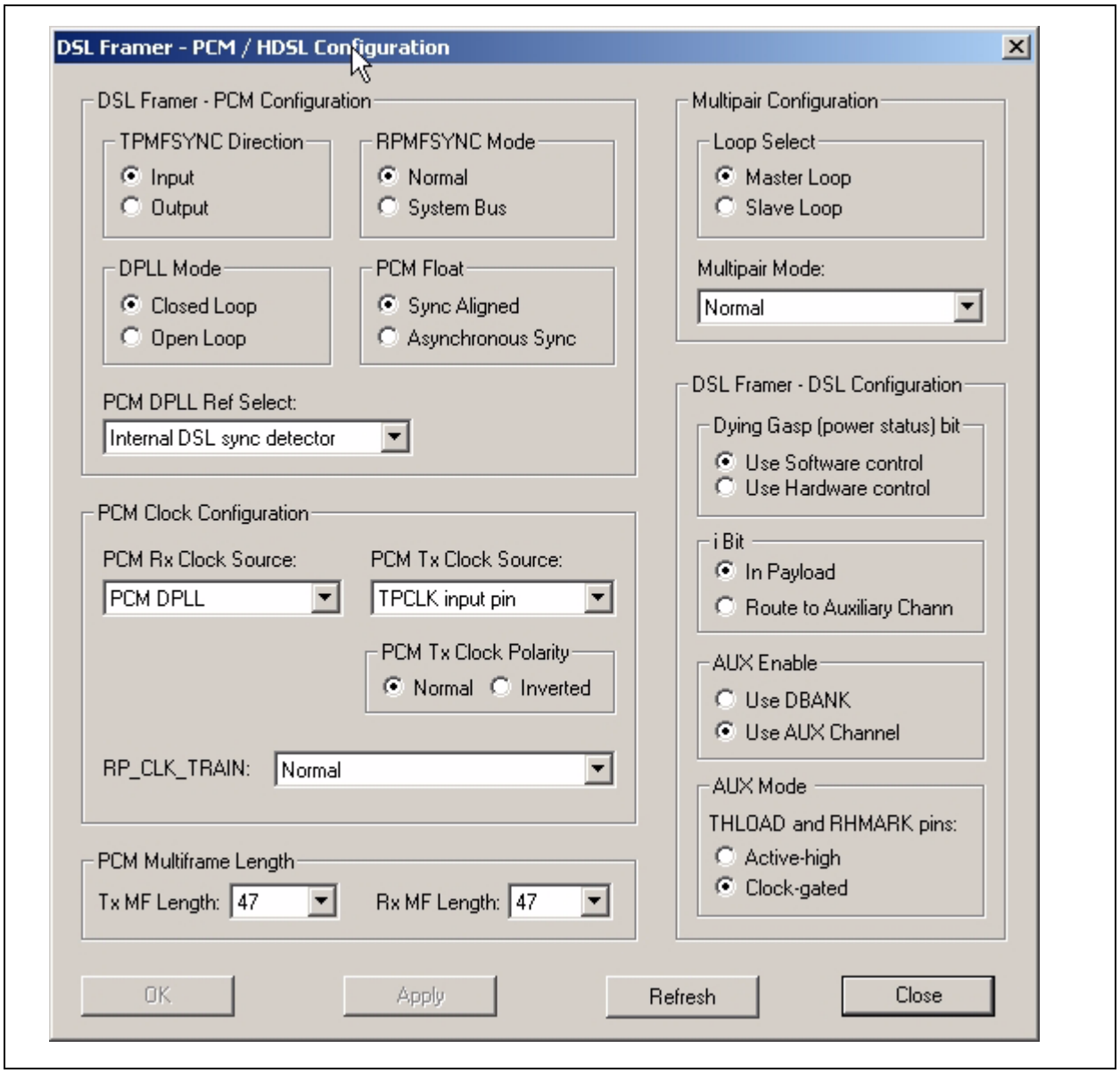
Figure 3-164. TestExec ATM Configuration for RT



12. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      - TPMFSYNC Direction - **Input**
      - RPMFSYNC Mode - **Normal**
      - DPLL Mode - **Closed Loop**
      - PCM Float - **Sync Aligned**
      - PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      - PCM Rx Clock Source - **PCM DPLL**
      - PCM Tx Clock Source - **TPCLK Input**
      - PCM Tx Clock Polarity - **Normal**
      - RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length
      - Tx MF Length - **47**

  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use AUX Channel**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

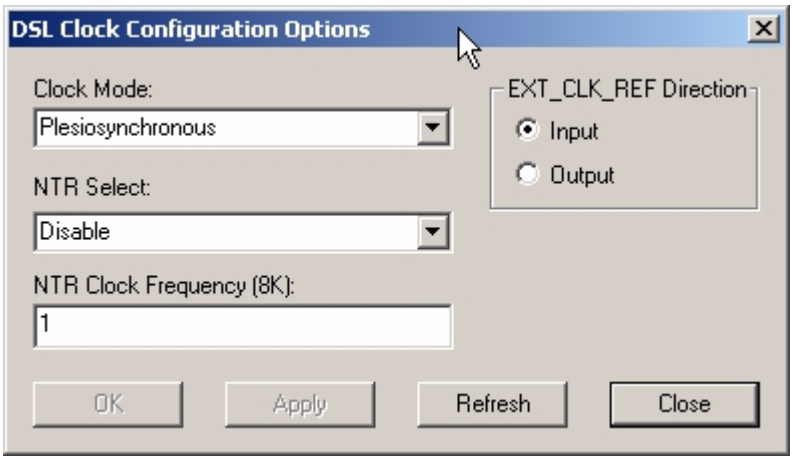
Figure 3-165. TestExec PCM/HDSL Configuration for RT



13. Click the **Apply** button and then click on the **Close** button.

14. Click on the **DSL Clock** Button.
15. Enter the following values:

Figure 3-166. TextExec DSL Clock Configuration for RT



16. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.12.6.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.
6. Go to the Cobalt ATM GUI. Click on the **Active Loop** button.
7. Verify that the Tester is running errorfree.

3.12.6.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-154. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

3.13 Enhanced EVM Setup for Single-pair Unframed PCM Transport.

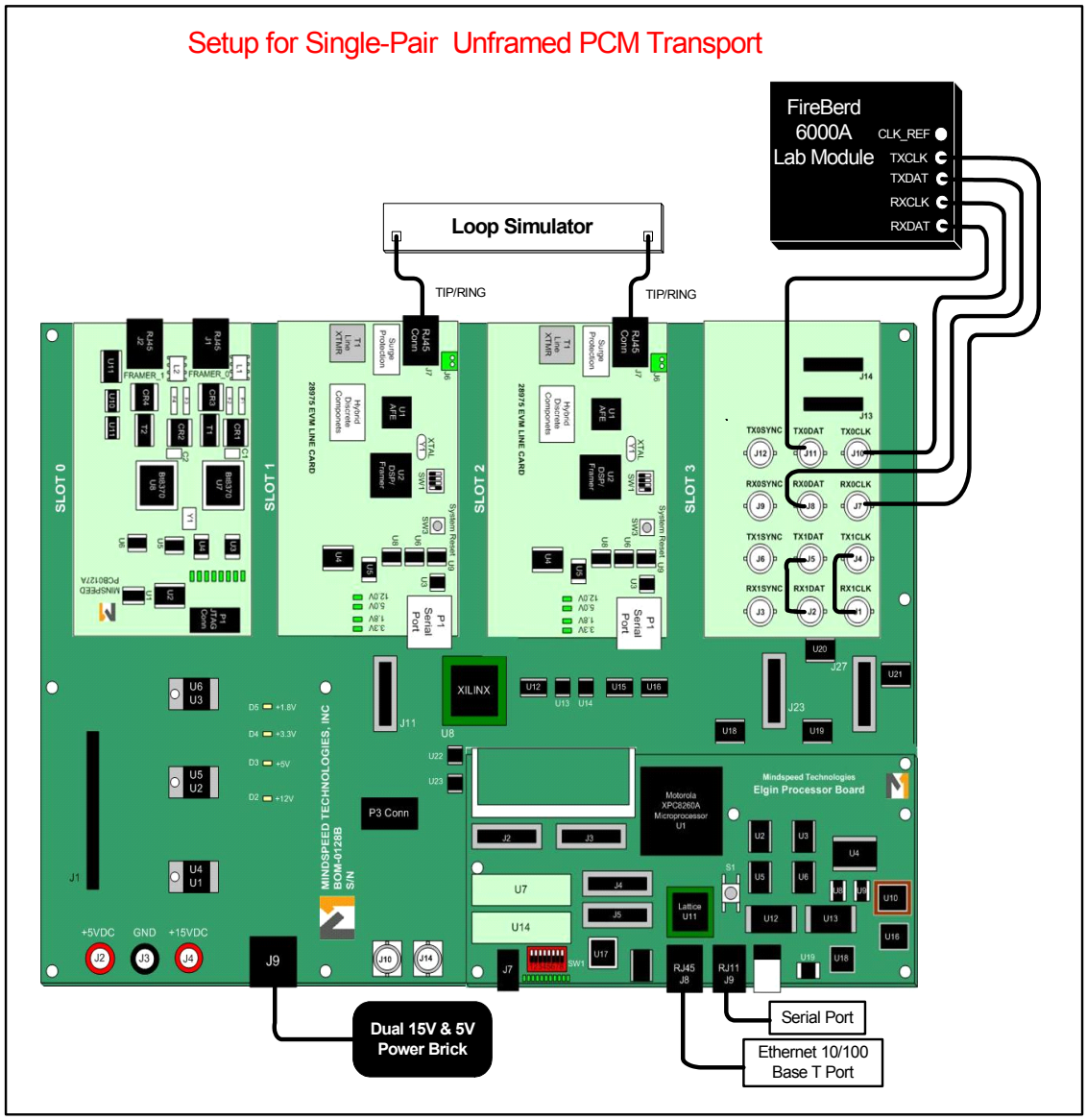
The following steps are required for running the ZipWirePlus Enhanced EVM for Single-Pair Unframed PCM Transport Application. This setup needs one enhanced EVM.

This configuration is valid for M28945, M28946, M28947 and M28950 devices.

The Hardware setup for this application is shown in Figure 3-167.

NOTE: The Fireberd must be equipped with a Lab Interface Adapter to proceed with the setup described in this section. Figure 3-167 illustrates the required interconnections.

Figure 3-167. Enhanced EVM Setup - Single Pair Unframed PCM Transport



3.13.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port

settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.

4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the HTU-C and the ZipWirePlus LIC in Slot 2 as the HTU-R. .
6. Fireberd Connections - Make the following connections
   - TX DATA (Fireberd) to RX0DAT (BNC Tester)
   - TX CLK OUT(Fireberd) to RX0CLK (BNC Tester)
   - RCV DATA (Fireberd) to TX0DAT (BNC Tester)
   - RCV CLK (Fireberd) to TX0CLK (BNC Tester)
7. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
8. BNC Tester Card Connections - Make the following connections
   - TX1DAT to RX1DAT
   - TX1CLK to RX1CLK

3.13.2 Fireberd Setup

Configure the Fireberd#2 Lab Interface Adapter as follows

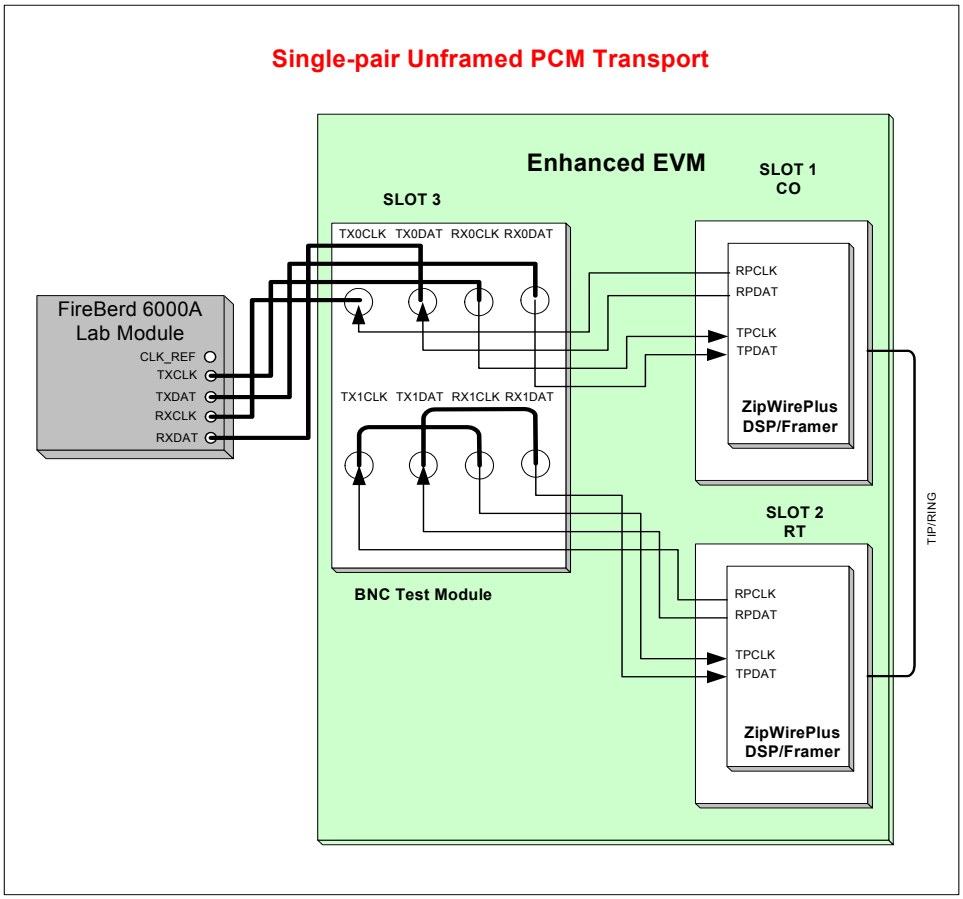
- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kH

3.13.3 FPGA Configuration

The Host Code configures FPGA(U8) into one of the many possible configurations through the TestExec (UIP) GUI.

This configuration will connect the PCM bus of the ZipWirePlus device (slot 1) to the Port #0 of the BNC Tester Card (slot 3) and the PCM bus of the ZipWirePlus device (slot 2) to the Port #1 of the BNC Tester Card(slot 3). Figure 3-168 explains the pin interconnections for this application.

Figure 3-168. Connections for Single-Pair Unframed PCM Transport



3.13.4 Enhanced EVM Configuration

3.13.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- ZipWirePlus firmware image.

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.13.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.13.5 TestExec

3.13.5.1 Installation and Configuration

Please refer to Section 3.3.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software

We will use the Enha

ncedEvm design file for the Enhanced EVM.

3.13.5.2 Enhanced EVM Configuration

1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

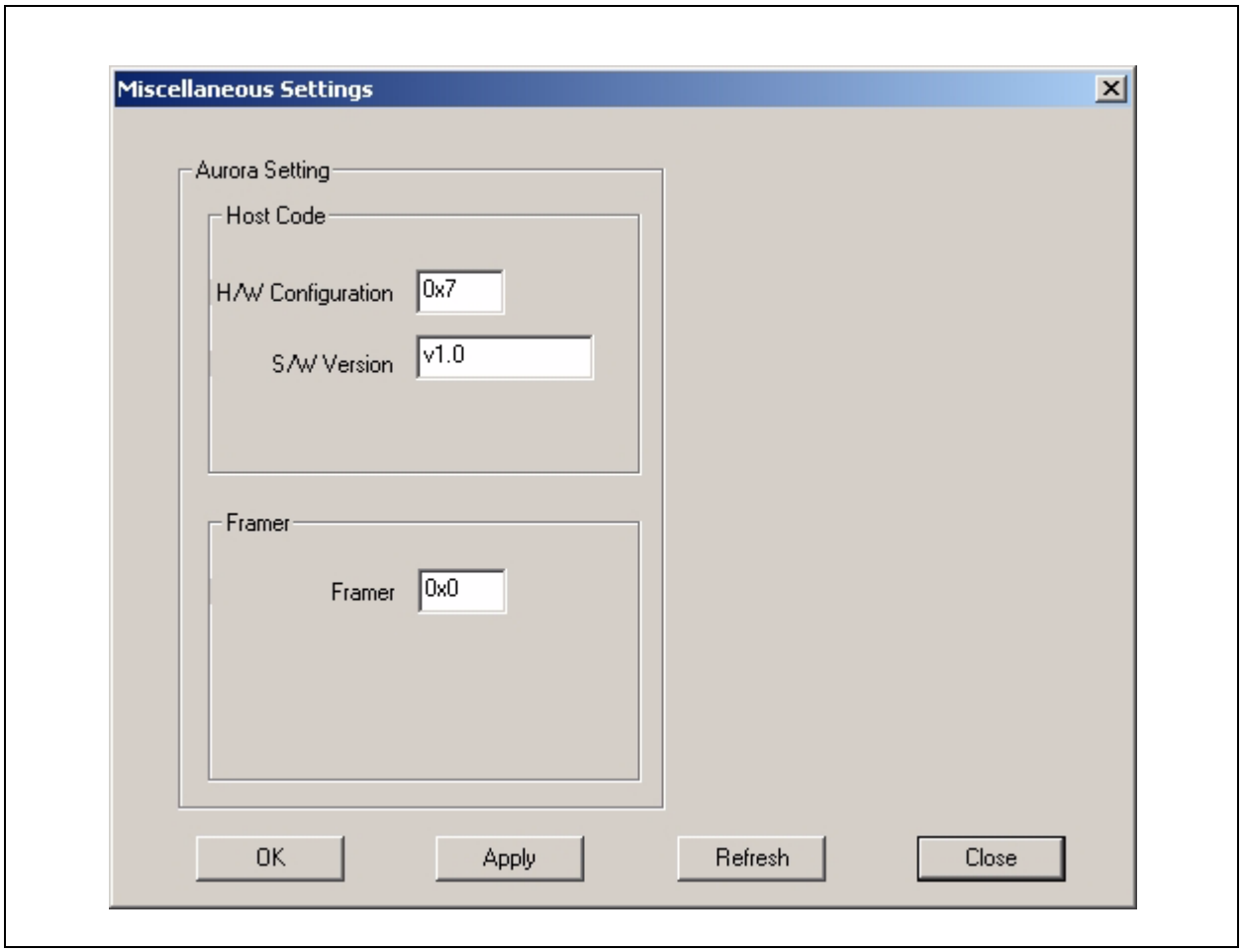
   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**

3.13.5.2.1 Hardware Configuration

1. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
2. Enter the **H/W Configuration** value to be 0x7.
3. Enter the **Framer** value to be 0x0.This value is a dont care here.

Figure 3-169. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM

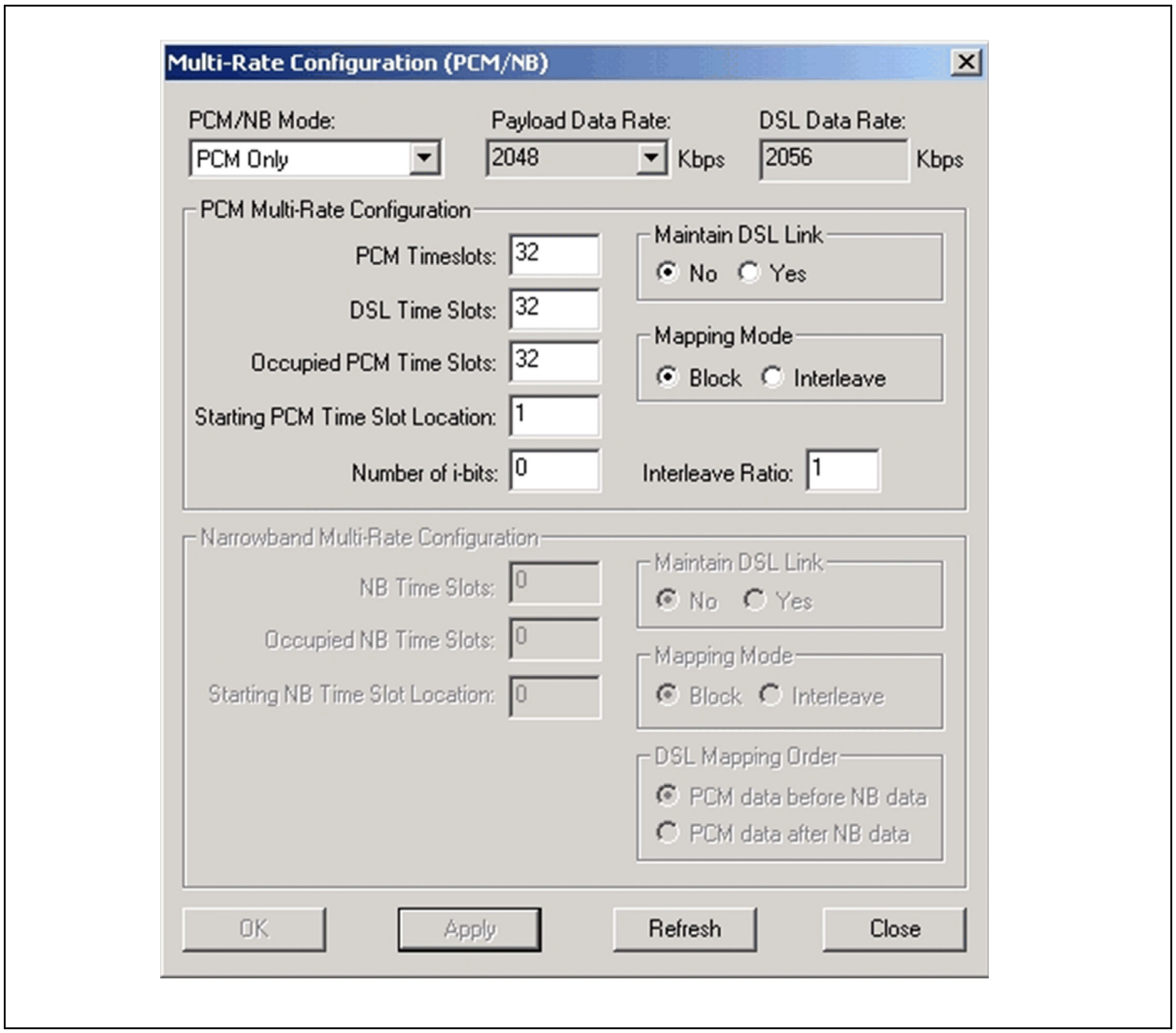


3.13.5.2.2 Slot 1 (HTU-C Side)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the Values:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

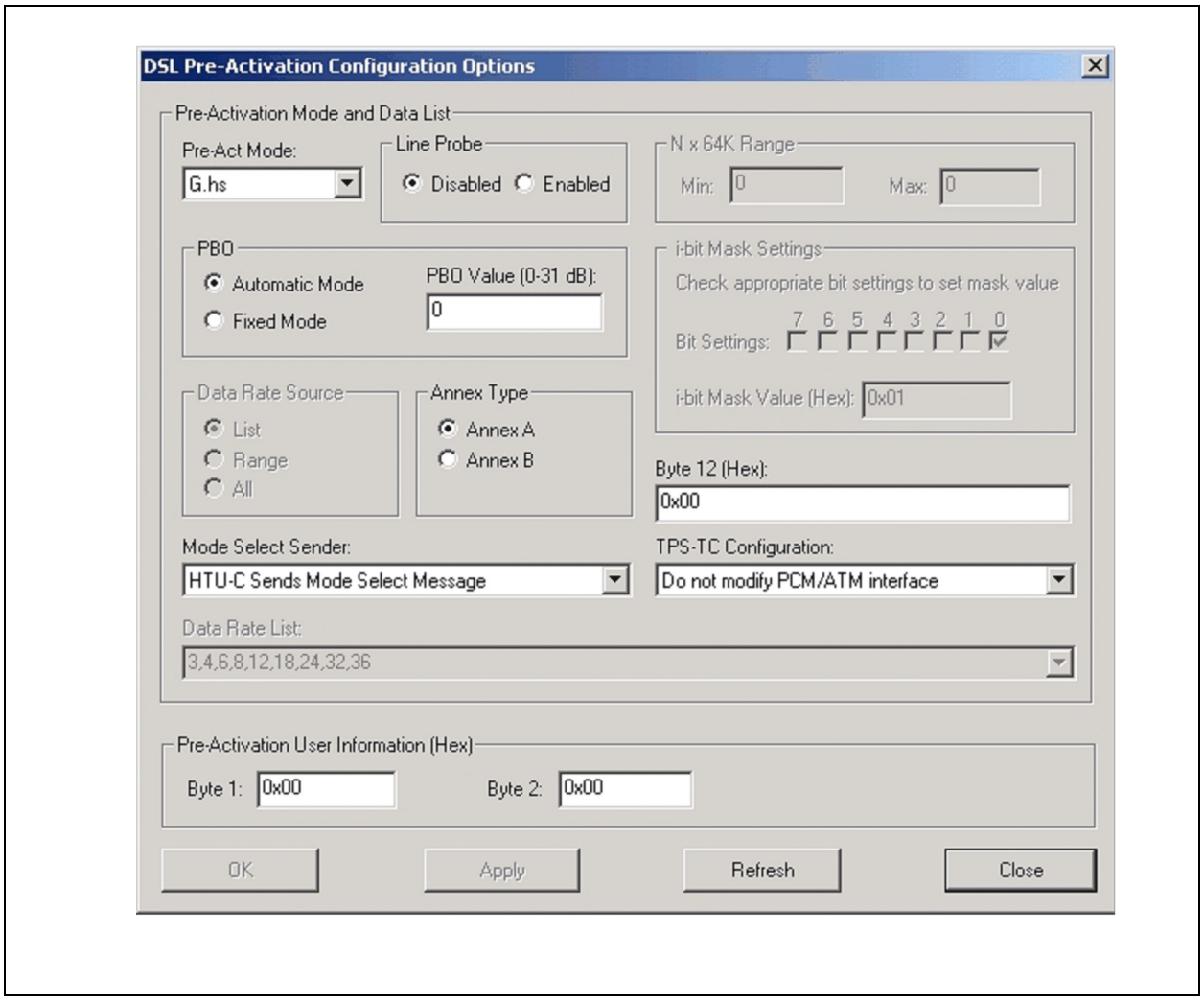
Figure 3-170. TestExec Multi-Rate Configuration for CO



Click the **Apply** button. The Payload Data Rate will change to 2048 Kbps and the DSL Data Rate will change to be 2056 Kbps. Click the **Close** button.

5. Click on the **Pre-Activation** button.

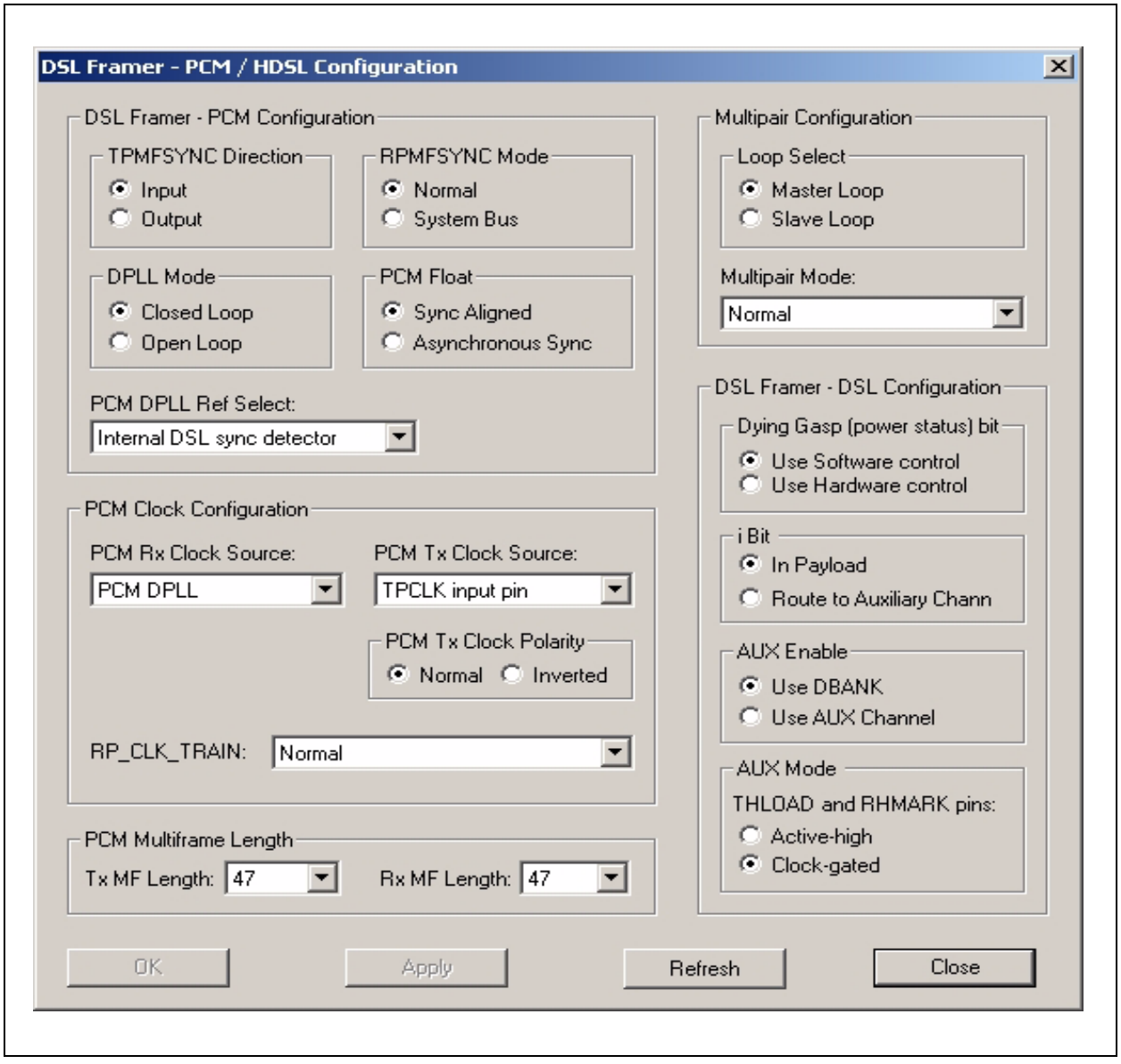
Figure 3-171. TestExec Preactivation Configuration for CO



6. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
7. Click on the **Apply** button and then click on the **Close** button.
8. Click on the **PCM/HDSL** button. Enter the following values:
   - DSL framer - PCM Configuration
     - TPMFSYNC Direction - **Input**
     - RPMFSYNC Mode - **Normal**
     - DPLL Mode - **Closed Loop**
     - PCM Float - **Sync Aligned**
     - PCM DPLL Ref Select - **Internal DSL Sync Detector**
   - PCM Clock Configuration
     - PCM Rx Clock Source - **PCM DPLL**
     - PCM Tx Clock Source - **TPCLK Input**
     - PCM Tx Clock Polarity - **Normal**
     - RP_CLK_TRAIN - **Normal**
   - PCM Multiframe Length

  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

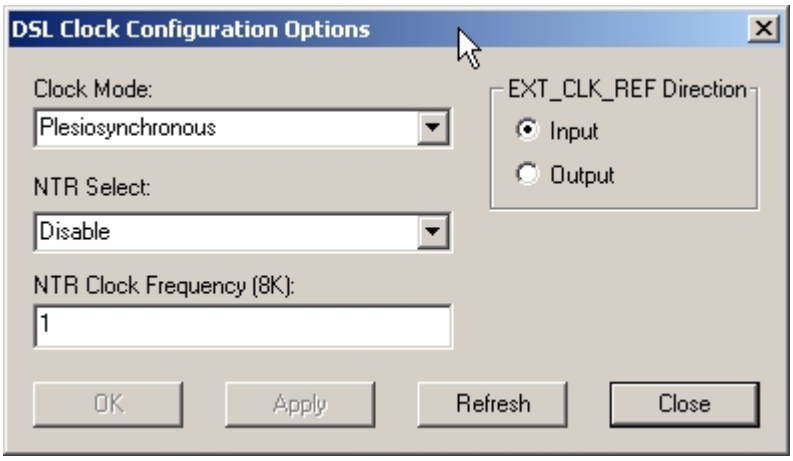
Figure 3-172. TestExec PCM/HDSL Configuration for CO



9. Click on the **Apply** button and then click on the **Close** button.

10. Click on the **DSL Clock** Button.
11. Enter the following values:

Figure 3-173. TextExec DSL Clock Configuration for CO



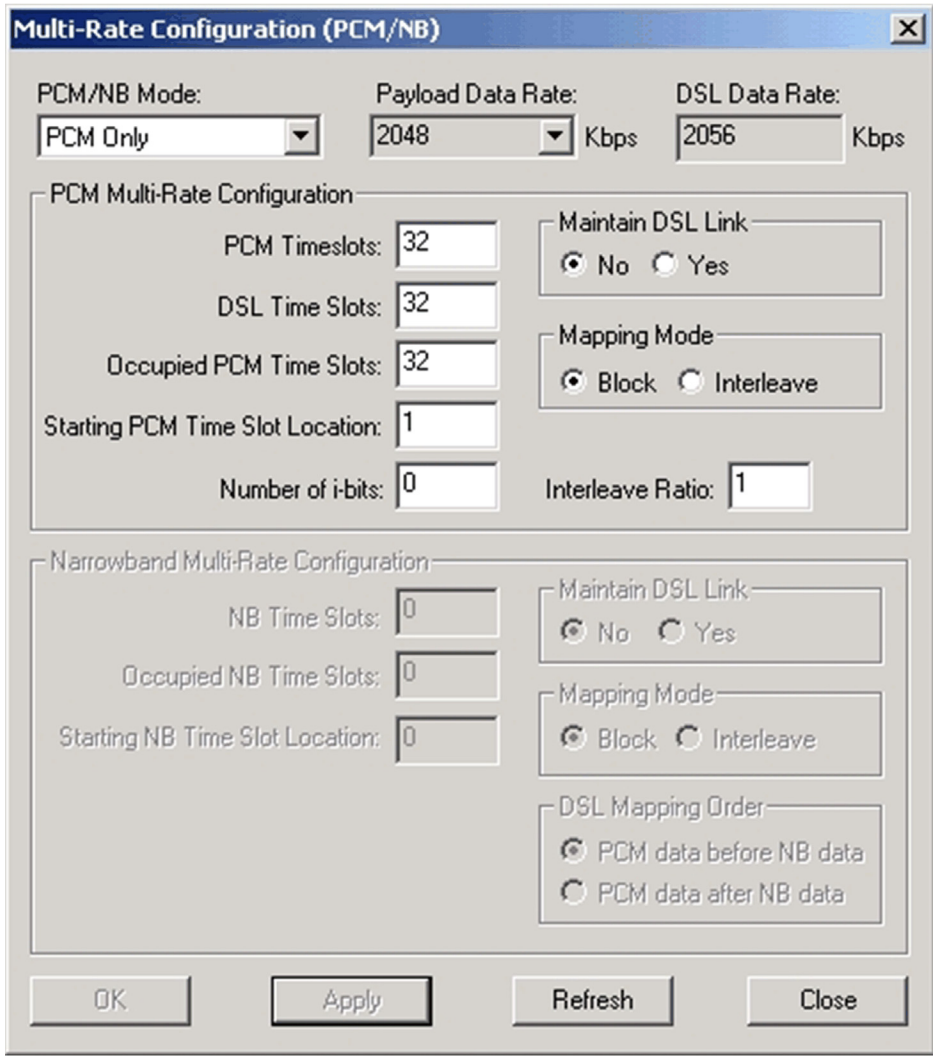
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.
13. Change to Slot 2 by right clicking the mouse button and selecting **Slot 2.**

3.13.5.2.3 Slot 2 (HTU-R Side)

1. Click on the **System Configuration** tab.
2. Set the **Terminal Type** to **HTU-R**.
3. Set the **System State** to **In-Service**.
4. Click on **Multi-Rate Button**.
5. Enter the values:

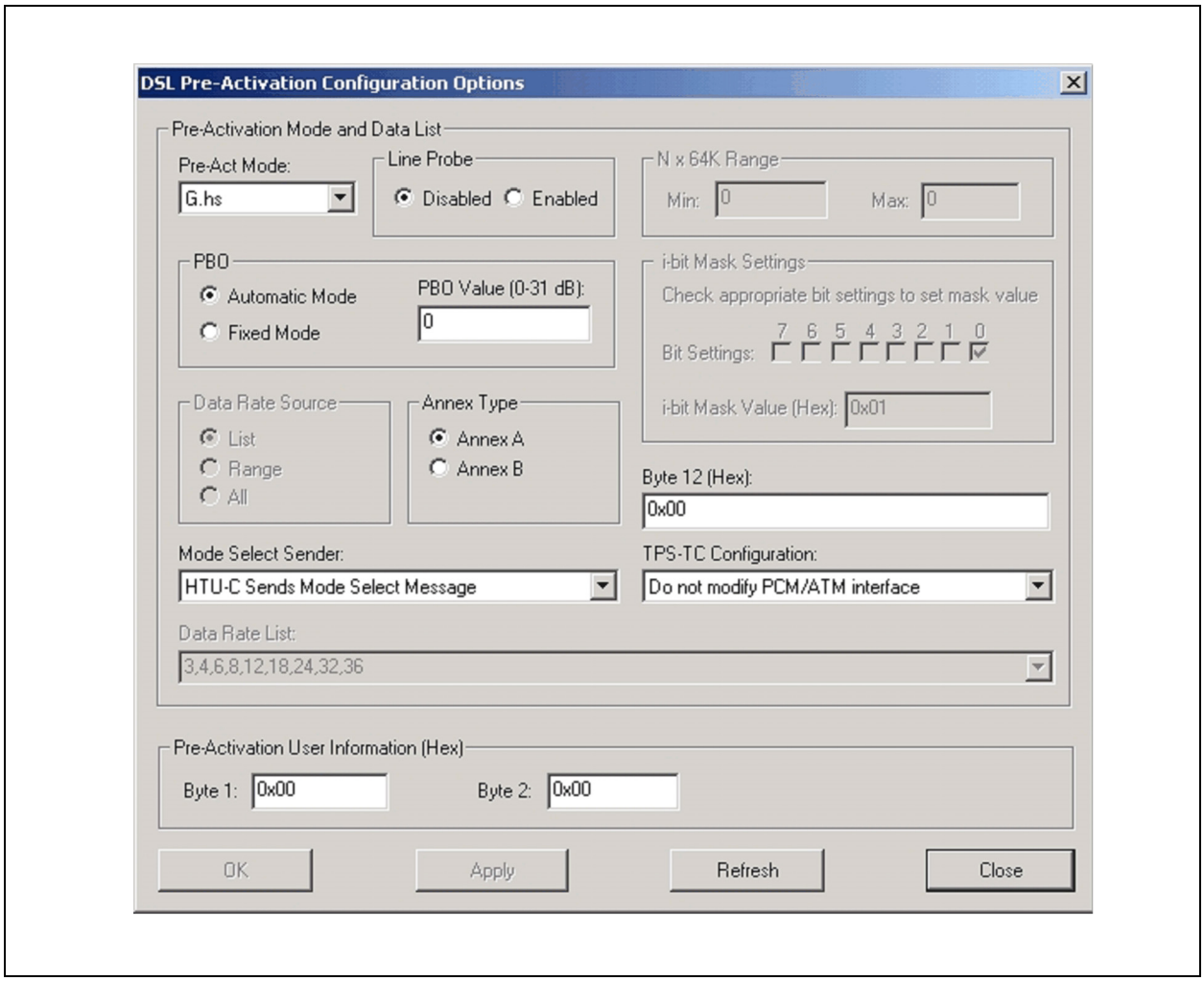
- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **32**
- Starting PCM Time Slot Location - **1**
- Number of i-bits - **0**

Figure 3-174. TestExec Multi Rate Configuration for RT



6. Click the **Apply** button. The **Payload Data Rate** will change to 2048 Kbps and the **DSL Data Rate** will change to be 2056 Kbps. Click the **Close** button.
7. Click on the **Pre-Activation** button.

Figure 3-175. TestExec Preactivation Configuration for RT



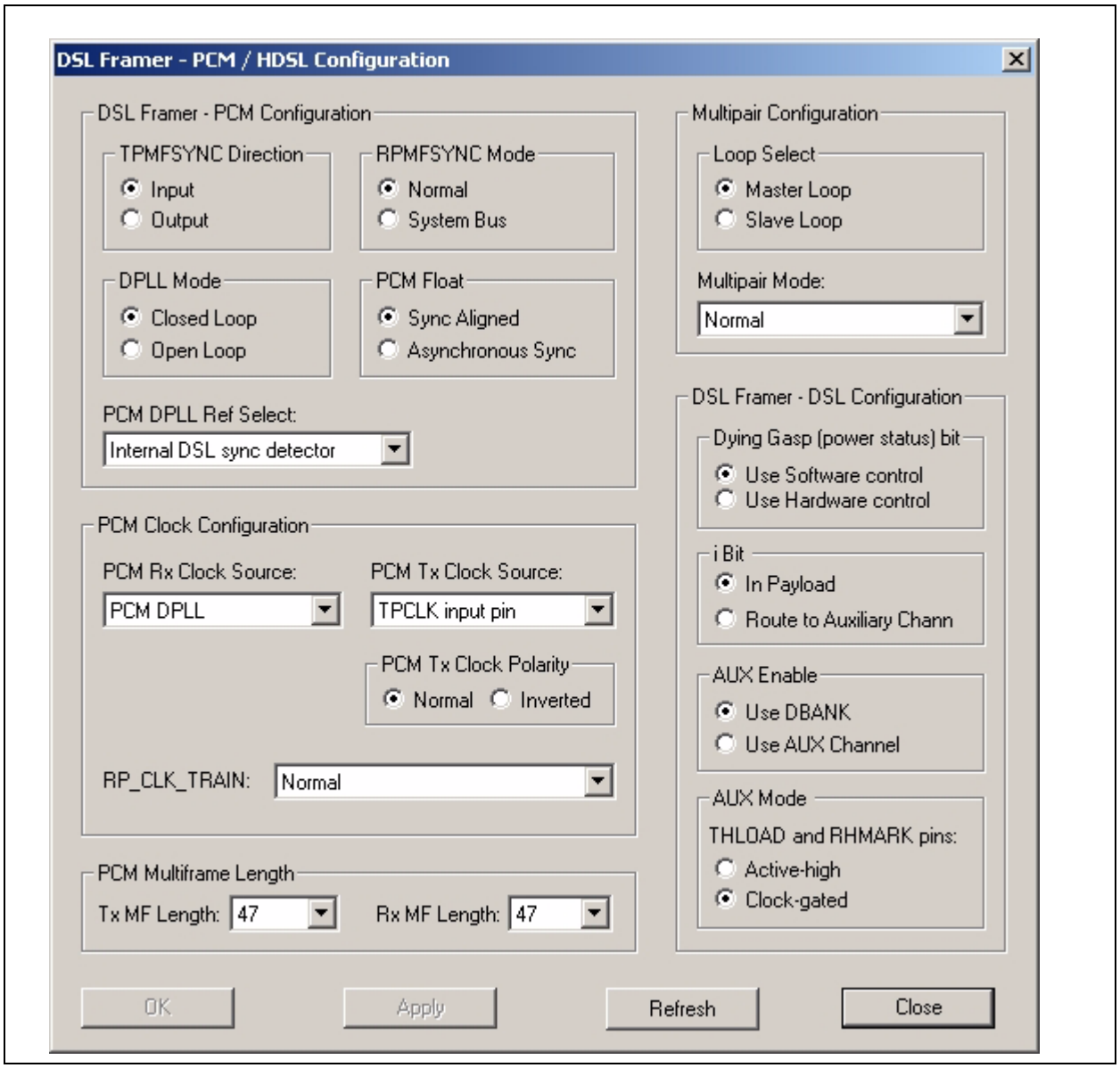
8. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
9. Click on **Apply** button and then click on the **Close** button.
10. Click on the **PCM/HDSL** button. Enter the following values:
    - DSL framer - PCM Configuration
      - TPMFSYNC Direction - **Input**
      - RPMFSYNC Mode - **Normal**
      - DPLL Mode - **Closed Loop**
      - PCM Float - **Sync Aligned**
      - PCM DPLL Ref Select - **Internal DSL Sync Detector**
    - PCM Clock Configuration
      - PCM Rx Clock Source - **PCM DPLL**
      - PCM Tx Clock Source - **TPCLK Input**
      - PCM Tx Clock Polarity - **Normal**
      - RP_CLK_TRAIN - **Normal**
    - PCM Multiframe Length
      - Tx MF Length - **47**

  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **Normal**
- DSL Framer – DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

11. Make the following changes:

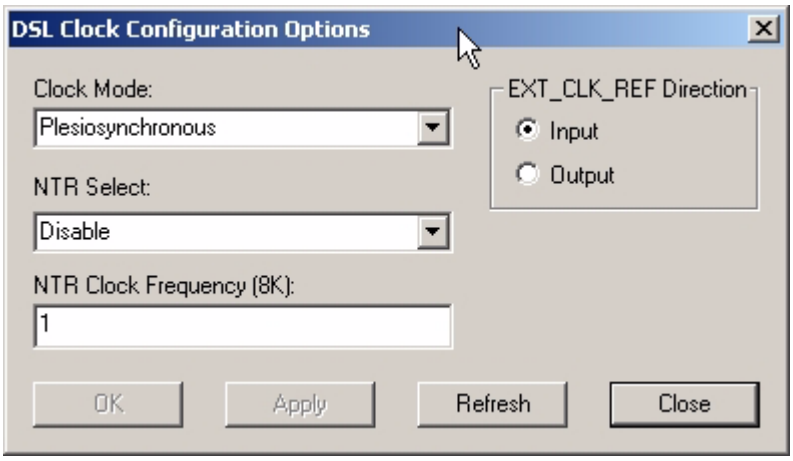
- **PCM Tx Clock Source** to be **TPCLK input pin**, as the ZipWirePlus device shall use the clock from Bt8370 for PCM Transmit direction.
- DPLL Mode - **Closed Loop**

Figure 3-176. TestExec PCM/HDSL Configuration for RT



12. Click the **Apply** button and then click on the **Close** button.
13. Click on the **DSL Clock** Button.
14. Enter the following values:

Figure 3-177. TextExec DSL Clock Configuration for RT



15. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.13.5.2.4 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the **Set** button in the **Auto Update Timer** box.
4. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State..
5. Verify the Fireberds are in SYNC with no Bit Errors.

3.13.5.3 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-167. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

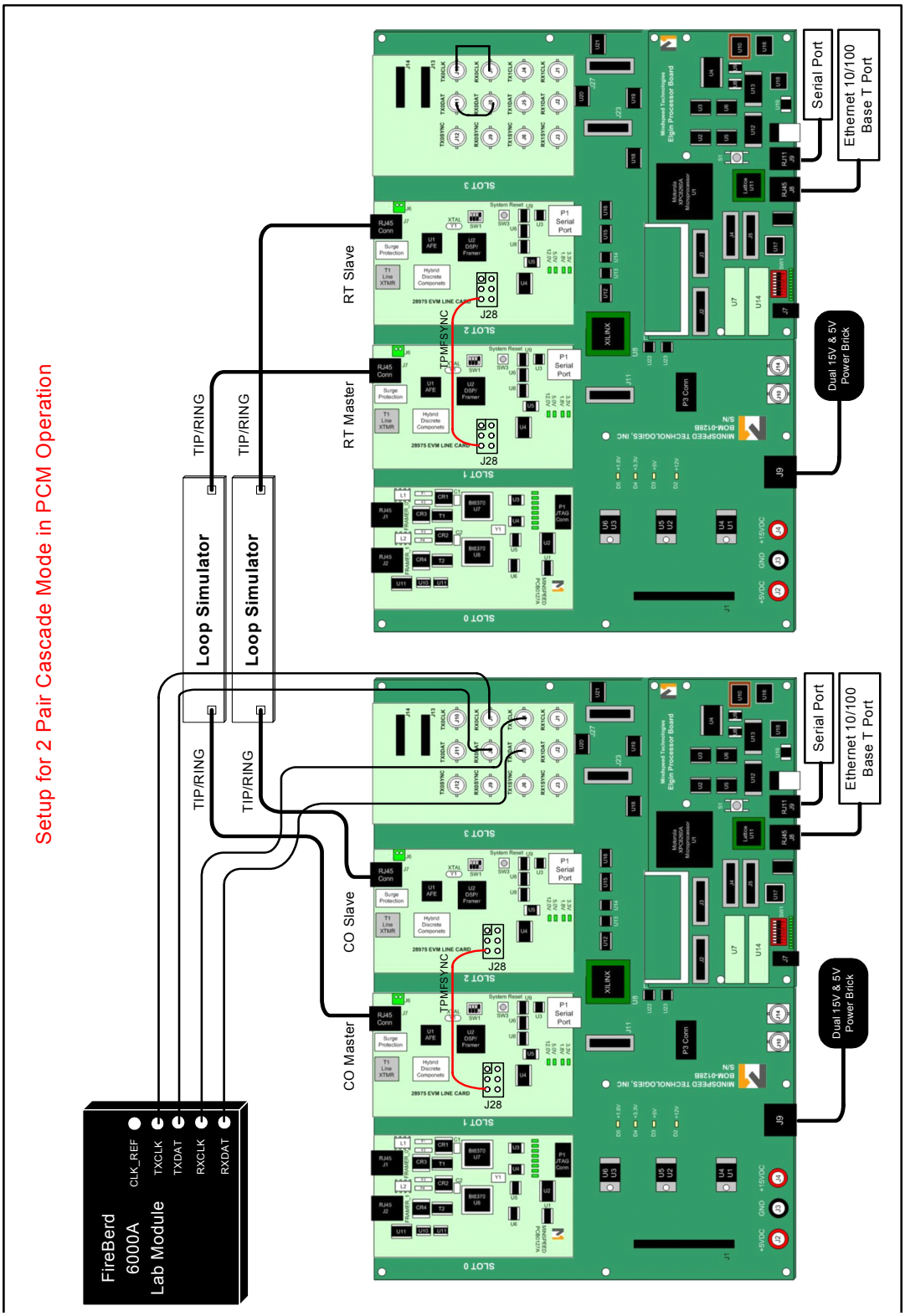
3.14 Enhanced EVM Setup for Multi-pair Unframed PCM Operation

The following steps are required for running the ZipWirePlus Enhanced EVM in Multi-Pair Unframed PCM Mode. This setup needs two enhanced EVMs.

First, we shall use only the HTU-C EVM and put the DSL side is put into loopback. Then we shall perform end to end testing with two enhanced EVMs. The Hardware setup for this application is shown in Figure 3-178.

NOTE: The Fireberd must be equipped with a Lab Interface Adapter to proceed with the setup described in this section. Figure 3-178 illustrates the required interconnections.

Figure 3-178. Enhanced EVM Setup for Two-Pair Framed PCM Operation



3.14.1 Enhanced EVM Setup

The setup procedure is as follows:

1. Place the Enhanced EVM on a bench.
2. Ensure the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Hardware Modifications - Connect the TPMFSYNC (pin 5 of J28) of the ZipWirePlus Master LIC (Slot 1) to the TPMFSYNC (pin 5 of J28) of the ZipWirePlus Slave LIC (Slot 2).
7. Fireberd Connections - Make the following connections
   - TX DATA (Fireberd) to RX0DAT (BNC Tester)
   - TX CLK OUT(Fireberd) to RX0CLK (BNC Tester)
   - RCV DATA (Fireberd) to TX0DAT (BNC Tester)
   - RCV CLK (Fireberd) to TX0CLK (BNC Tester)
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.

3.14.2 Fireberd Setup

Configure the Fireberd#2 Lab Interface Adapter as follows

- DATA: 2^{23}-1
- GEN CLK: SYNTH
- SYNTH FREQ: 2048.0 kH

3.14.3 FPGA Configuration

This configuration will connect the PCM bus of ZipWirePlus device (slot 1 - Master) and ZipWirePlus device (slot 2 - Slave) to the Port #0 of the BNC Tester Card (slot 3). The Figure 3-179 & Figure 3-180 explain the pin interconnections for this application.

Figure 3-179. Connections for Two-Pair unframed PCM Application CO Side

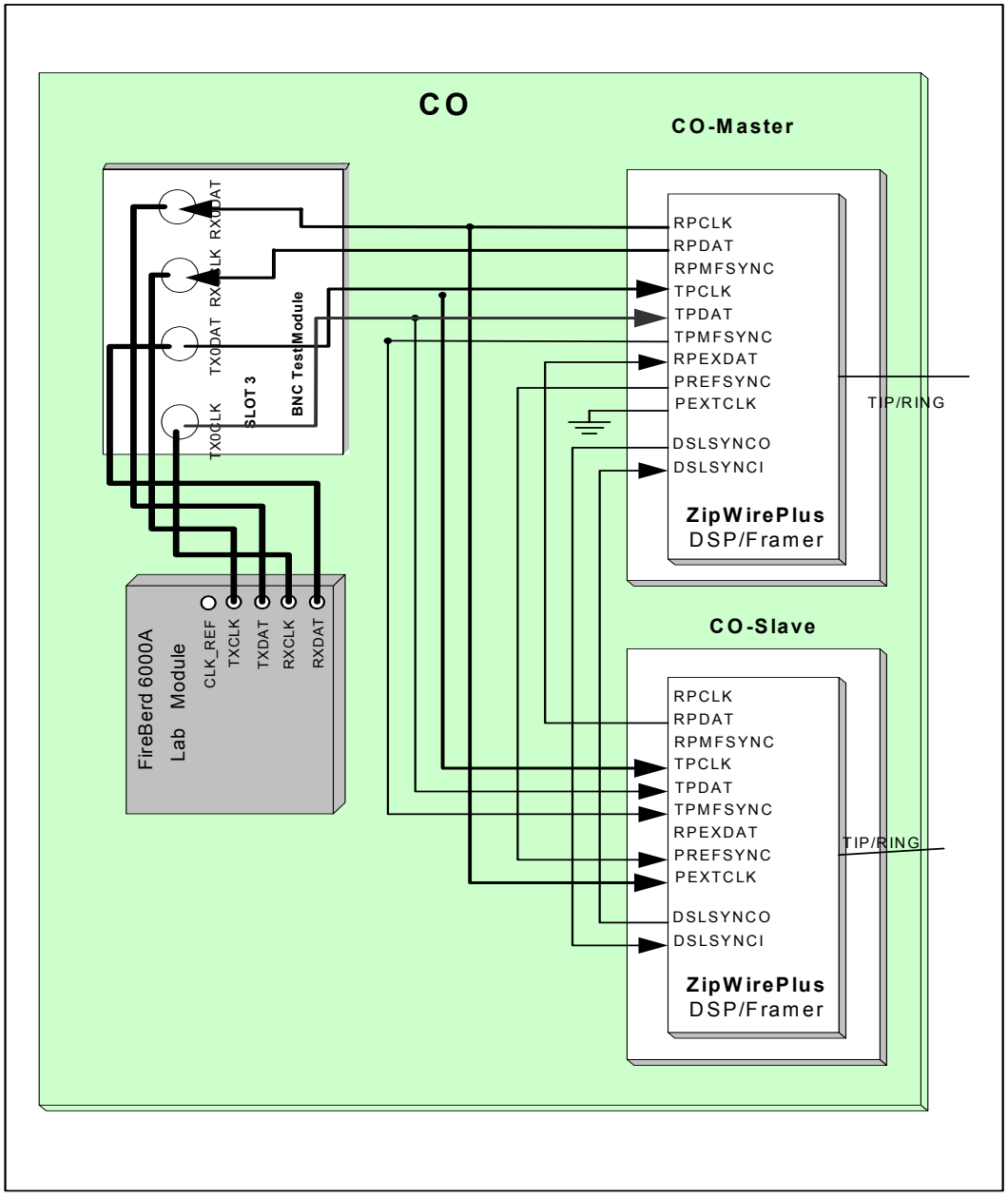
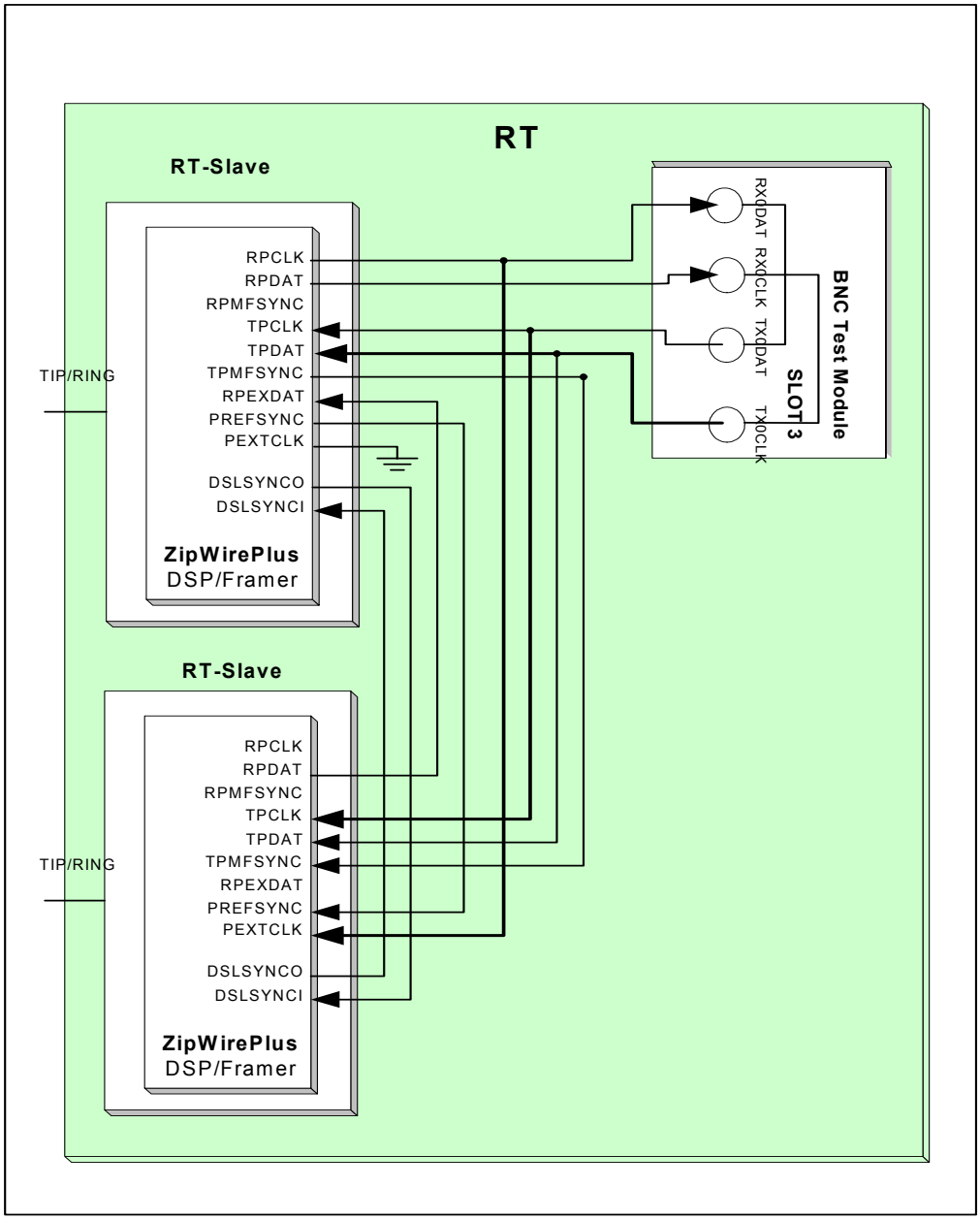


Figure 3-180. Connections for Two-Pair unframed PCM Application RT Side



3.14.4 Enhanced EVM Configuration

3.14.4.1 Enhanced EVM Software

The following files are needed for the bringing up the Enhanced EVM.

- EVM Elgin Microprocessor Software Image (vX_X_M289XX_eevm
- ZipWirePlus firmware image

Please refer to Section 3.2.4.2. This section explains the procedure for configuring the Enhanced EVM when powering up the Enhanced EVM for the first time.

3.14.4.2 Subsequent Power Ups

Please refer to Section 3.2.4.3. This section outlines the procedure for Enhanced EVM power up if the user has already configured the boot parameters.

3.14.5 TestExec

3.14.5.1 Installation and Configuration

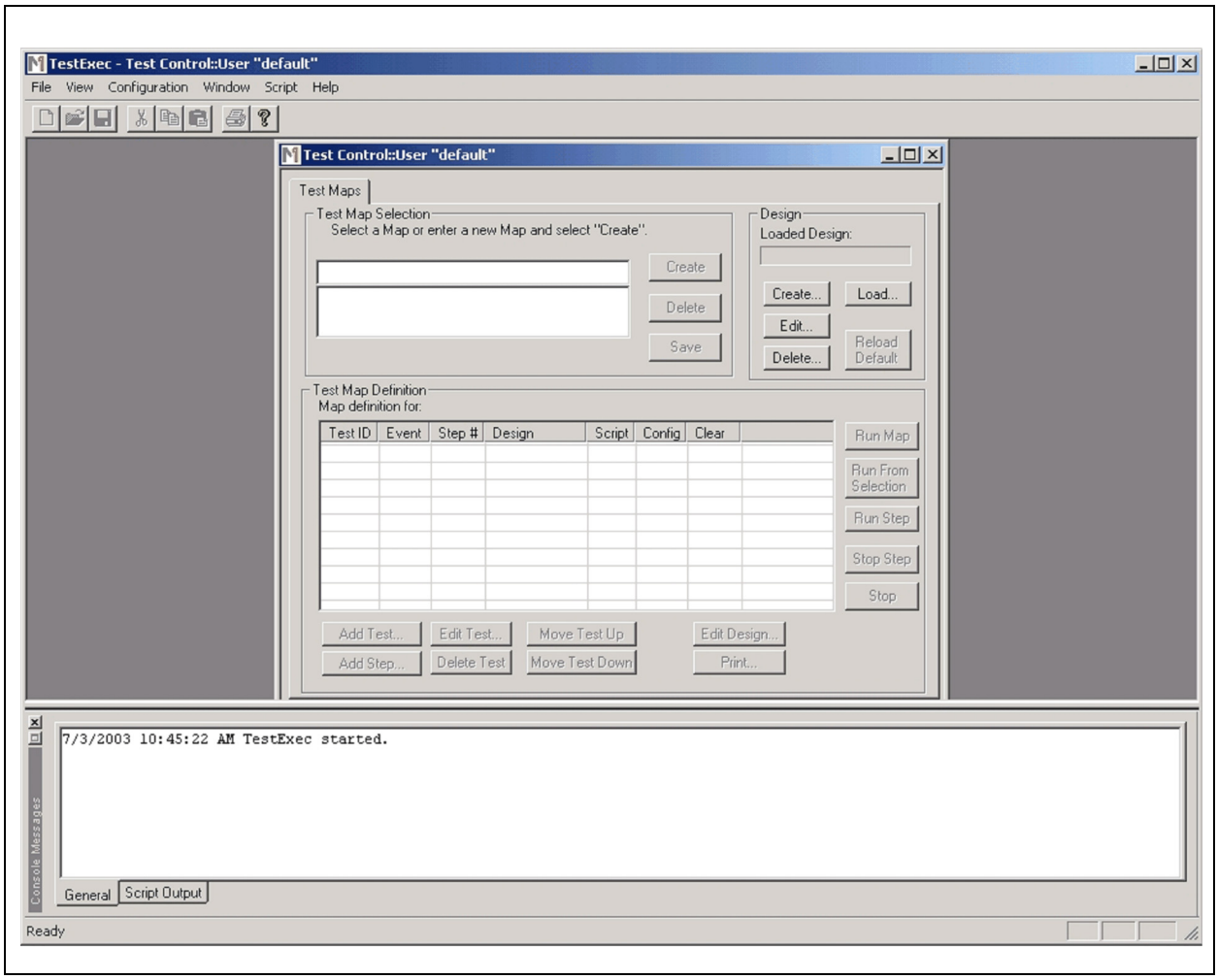
Please refer to Section 3.2.5.1 for a detailed procedure on installation and configuration of the TestExec(UIP) software.

We will use the **EnhancedEvm** design file for the HTU-C Enhanced EVM.

3.14.5.2 Enhanced EVM Configuration

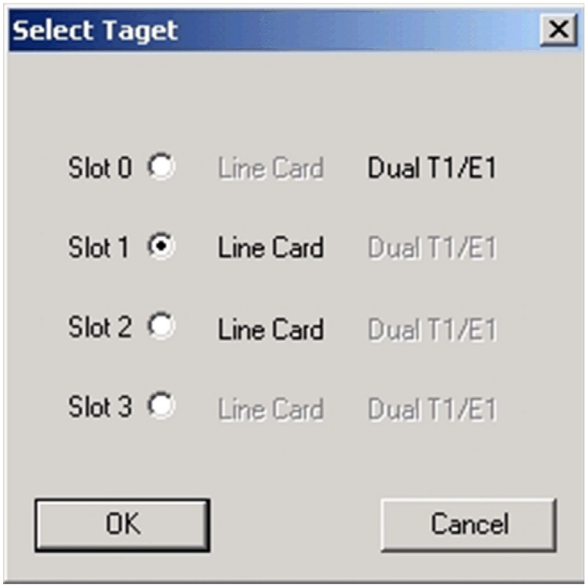
1. Run the Testexec.exe from the desktop.
2. The TestExec application will startup and displays the following screen.

Figure 3-181. TestExec Main GUI



3. Click on the **Load** button to load the design file.
4. The Test Exec will prompt you with a menu containing 3 design files
   a. **EnhancedEvm**
   b. **EnhancedEvm2**
   c. **LegacyEvm**
5. Select the **EnhancedEvm** design file. The TestExec will load the selected design file. Please note that for the HTU-C (CO) side EVM please select **EnhancedEvm** design file. For HTU-R (RT) side EVM please select the **EnhancedEvm2** design file.
6. Click on the **System Configuration** Tab.
7. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
8. The Enhanced EVM has four slots - starting from zero. Select the slot to be configured by right clicking the mouse. The following menu appears.

Figure 3-182. Selecting the Slot

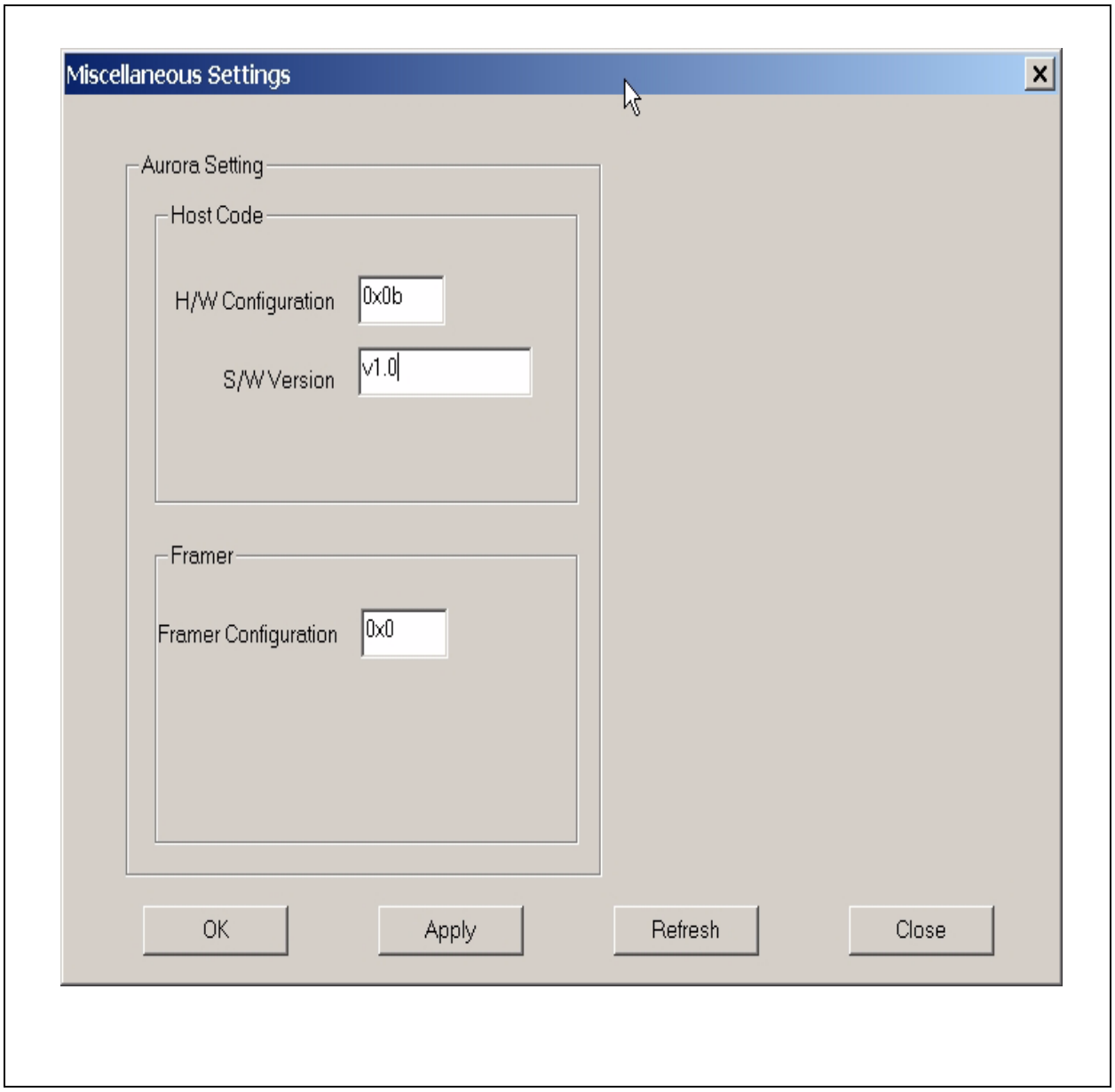


9. Select **Slot 1**.

3.14.5.2.1 Hardware Configuration

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1.**
2. Click on the **Miscellaneous Settings** button to configure the FPGA and Bt8370(T1/E1 Framer).
3. Enter the **H/W Configuration** value to be 0x0B.
4. Enter the **Framer** value to be 0x0.This value is a dont care here.

Figure 3-183. Miscellaneous Settings Window- for Hardware configuration of Enhanced EVM



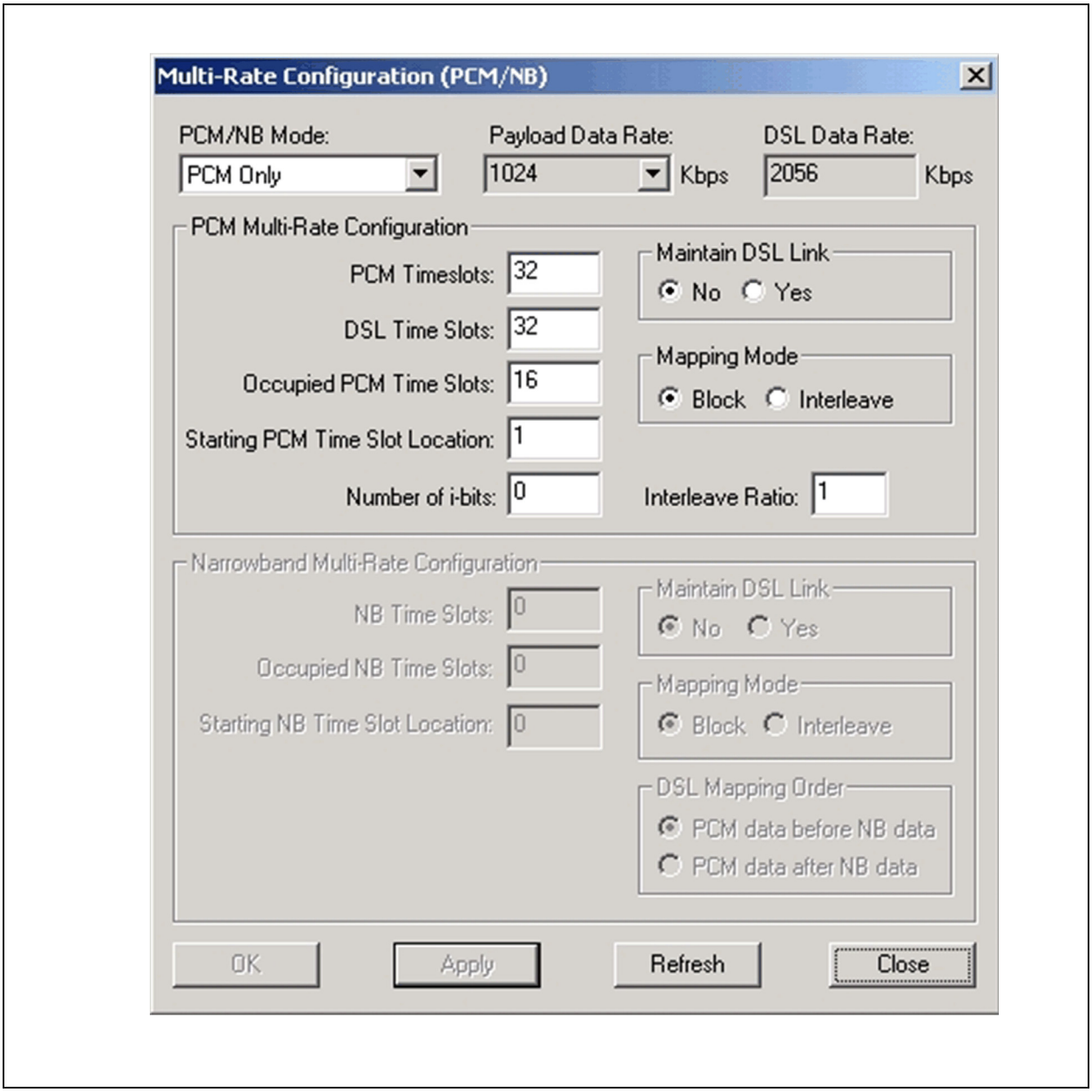
3.14.5.2.2 Slot 1 (HTU-C Master)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:

- PCM/NB Mode - **PCM Only**
- PCM Timeslots - **32**
- DSL Time Slots - **32**
- Occupied Time Slots - **16**
- Starting PCM Time Slot Location - **1**

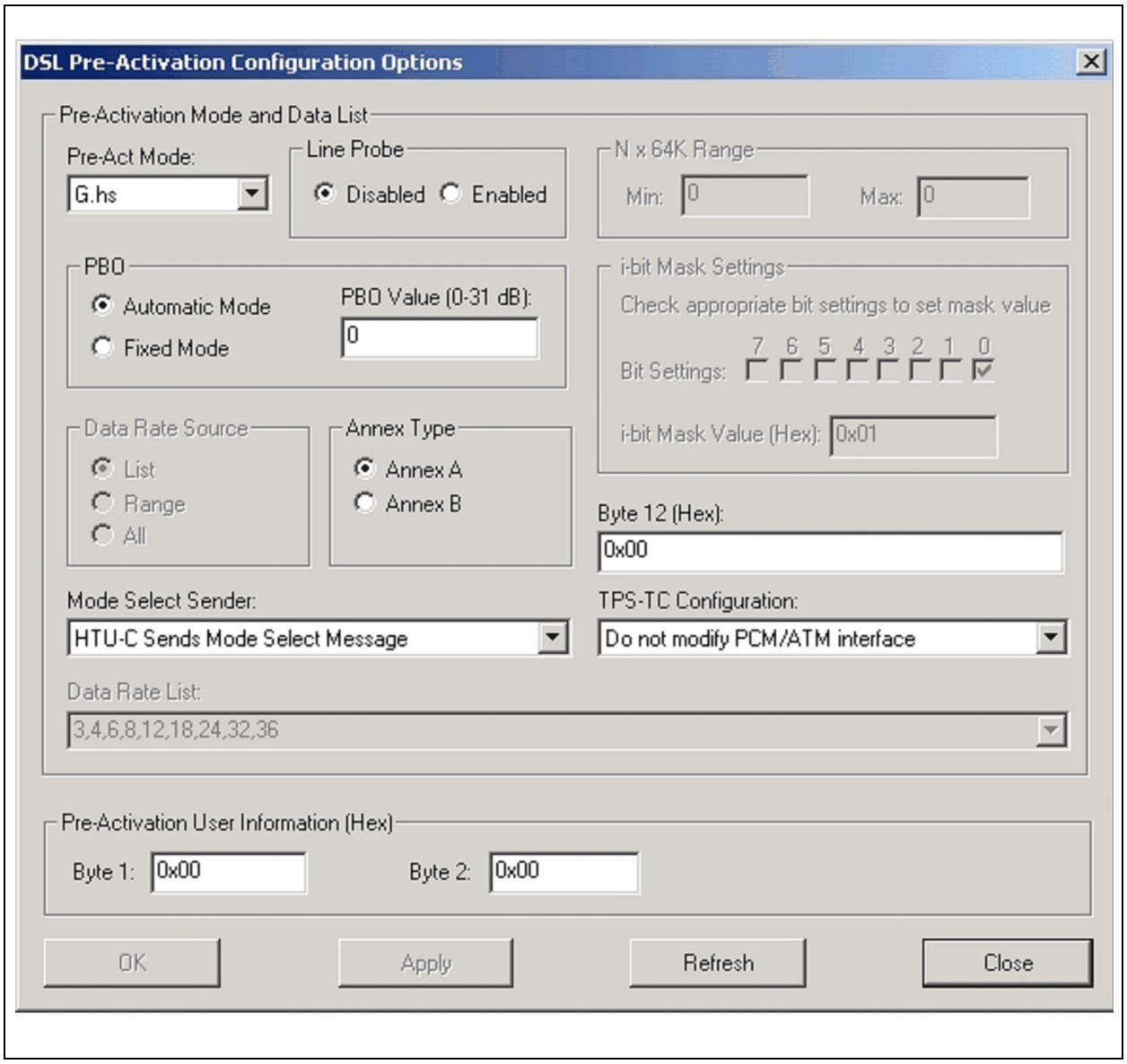
- Number of i-bits - **0**

Figure 3-184. TestExec Multi-Rate Configuration for Master



5. Click the **Apply** button. The **Payload Data Rate** will change to 1024 Kbps and the **DSL Data Rate** will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-185. TestExec Preactivation Configuration for Master

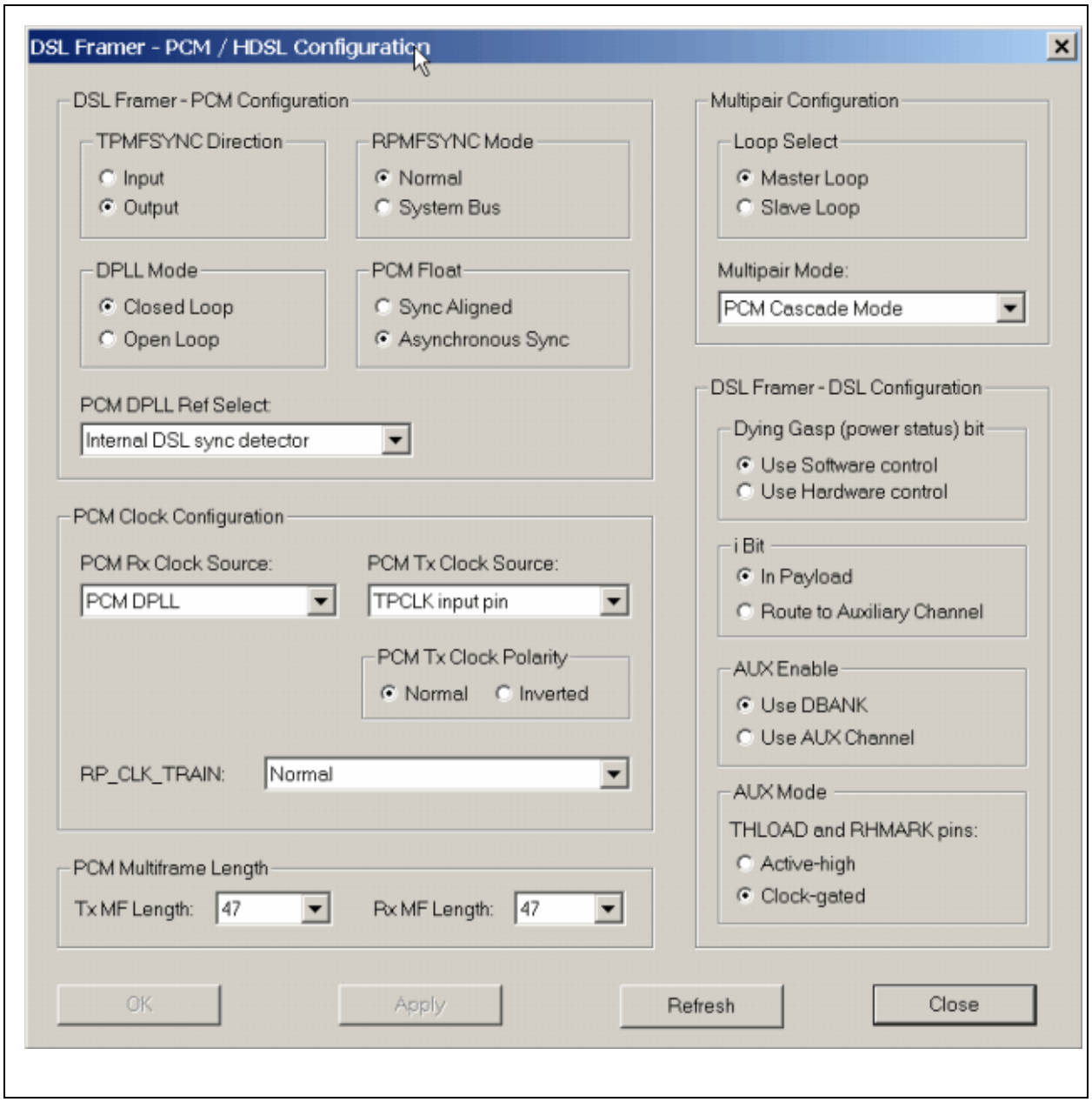


7. Change the **TPS-TC Configuration** to be **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - PCM Configuration
  - TPMFSYNC Direction - **Output**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Closed Loop**
  - PCM Float - **Asynchronous Sync**
  - PCM DPLL Ref Select - **Internal DSL Sync Detector**
- PCM Clock Configuration

  - PCM Rx Clock Source - **PCM DPLL**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**
- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Master Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - DSL Configuration
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - **Use DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-186. TextExec PCM/HDSL Configuration for Master



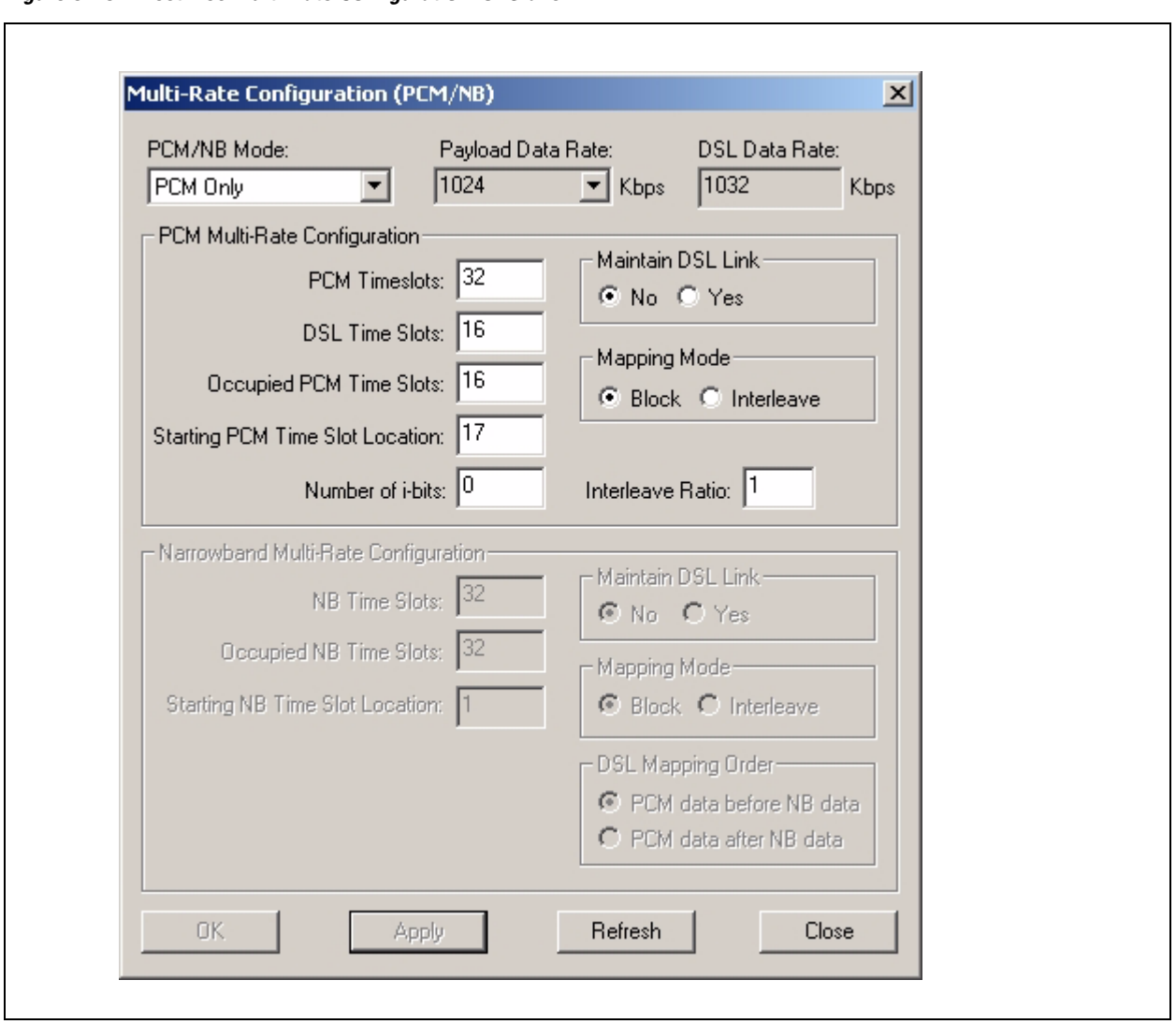
11. Click on **Apply** button and then click on the **Close** button.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration Menu**. This will enable the ZipWirePlus device and it will start training.
13. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.

3.14.5.2.3 Slot 2 (HTU-C Slave)

1. Click on the **System Configuration** tab.
2. Set the **System State** to **In-Service**.

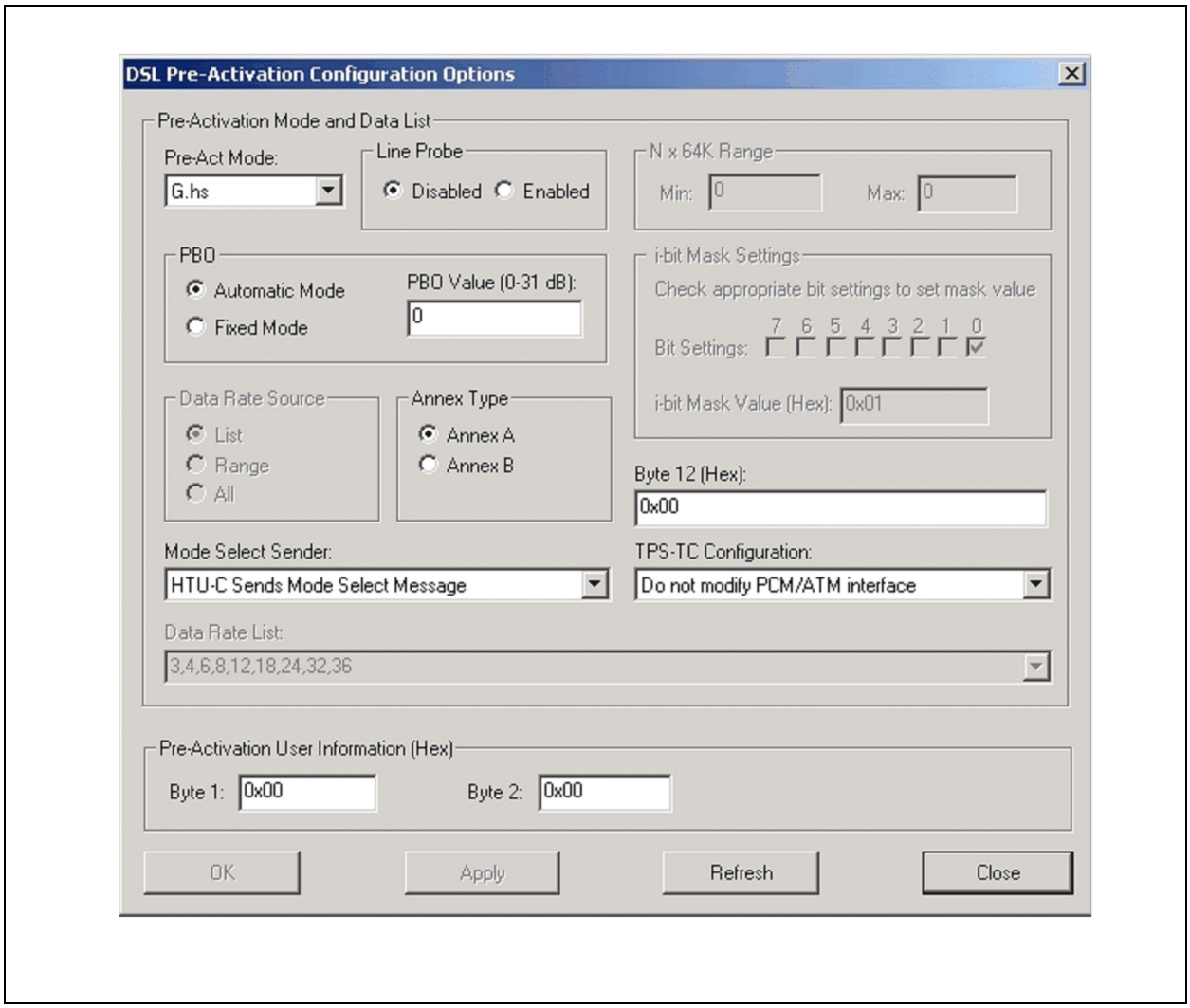
3. Click on the **Multi-Rate** Button.
4. Enter the values as follows:
   - PCM/NB Mode - **PCM Only**
   - PCM Timeslots - **32**
   - DSL Time Slots - **32**
   - Occupied Time Slots - **16**
   - Starting PCM Time Slot Location - **17**
   - Number of i-bits - **0**

Figure 3-187. TestExec Multi Rate Configuration for Slave



5. Click the **Apply** button. The Payload Data Rate will change to 1024 Kbps and the DSL Data Rate will change to be 1032 Kbps. Click the **Close** button.
6. Click on the **Pre-Activation** button.

Figure 3-188. TestExec Preactivation Configuration for Slave

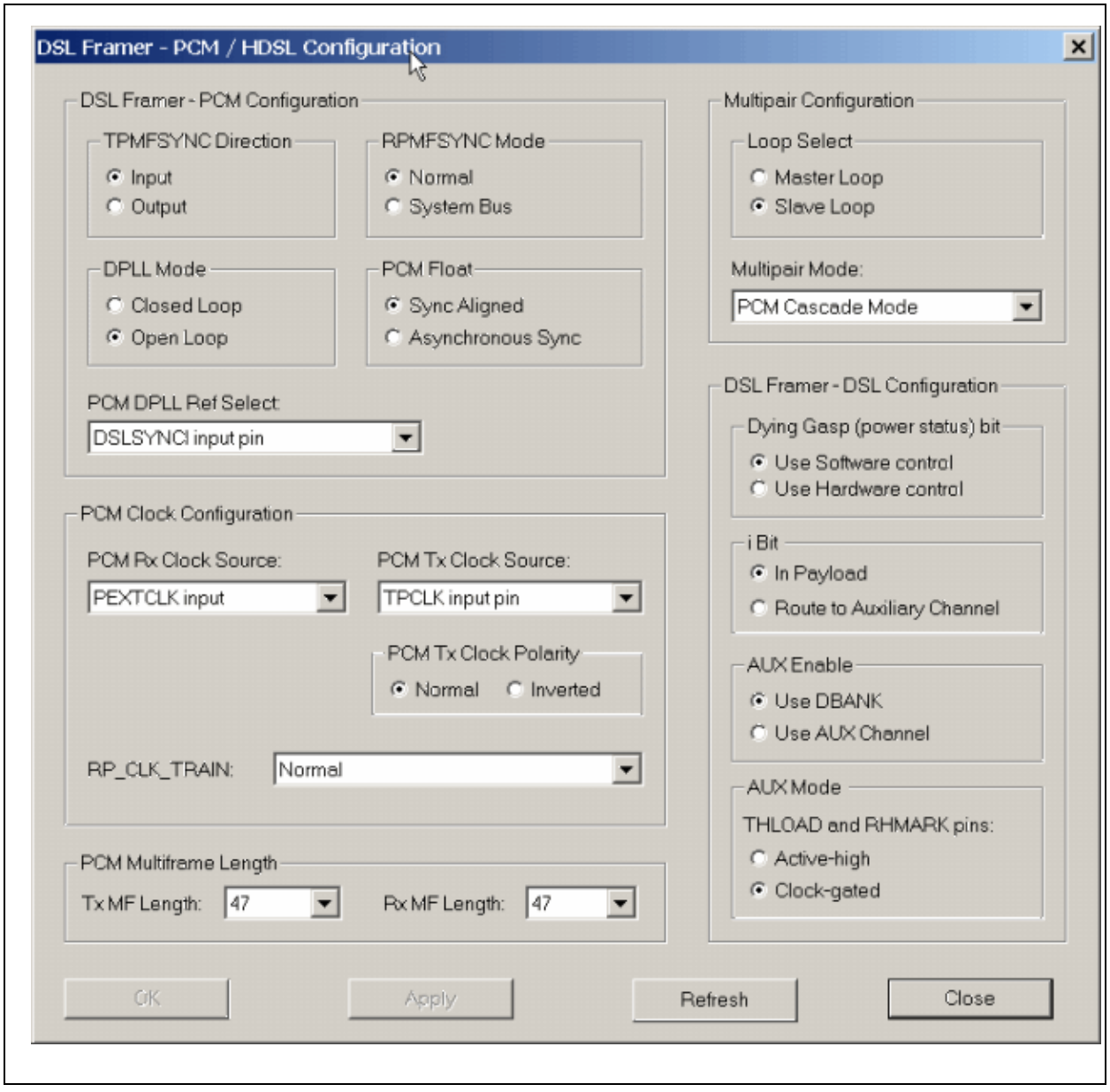


7. Change the **TPS-TC Configuration** to **Do not modify PCM/ATM Interface**.
8. Click on **Apply** button and then click on the **Close** button.
9. Click on the **PCM/HDSL** button.
10. Enter the following values:

- DSL framer - **PCM Configuration**
  - TPMFSYNC Direction - **Input**
  - RPMFSYNC Mode - **Normal**
  - DPLL Mode - **Open Loop**
  - PCM Float - **Sync Aligned**
  - PCM DPLL Ref Select - **DSLSYNCI input pin**
- PCM Clock Configuration
  - PCM Rx Clock Source - **PEXTCLK input**
  - PCM Tx Clock Source - **TPCLK Input**
  - PCM Tx Clock Polarity - **Normal**
  - RP_CLK_TRAIN - **Normal**

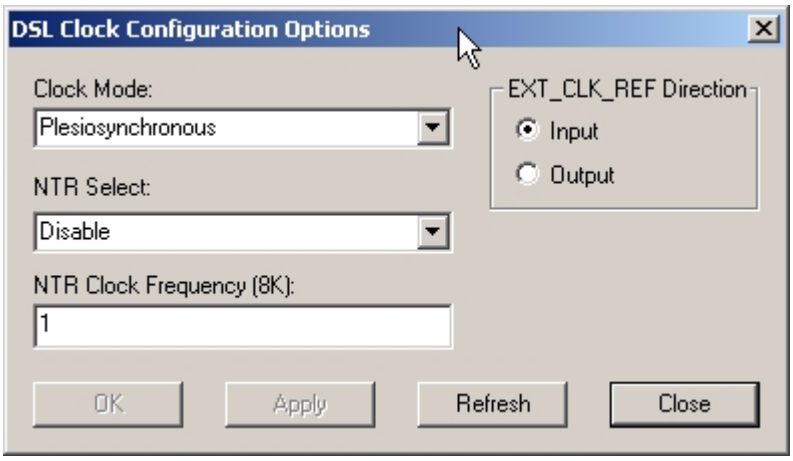
- PCM Multiframe Length
  - Tx MF Length - **47**
  - Rx MF Length - **47**
- Multipair Configuration
  - Loop Select - **Slave Loop**
  - Multipair Mode - **PCM Cascade Mode**
- DSL Framer - **DSL Configuration**
  - Dying Gasp - **Use Software Control**
  - i-bit - **In Payload**
  - AUX Enable - Use **DBANK**
  - AUX Mode THLOAD and RHMARK pins - **Clock Gated**

Figure 3-189. TextExec PCM/HDSL Configuration for Slave



11. Click on **Apply** button and then click on the **Close** button.
12. Click on the **DSL Clock** Button.
13. Enter the following values:

Figure 3-190. TextExec DSL Clock Configuration

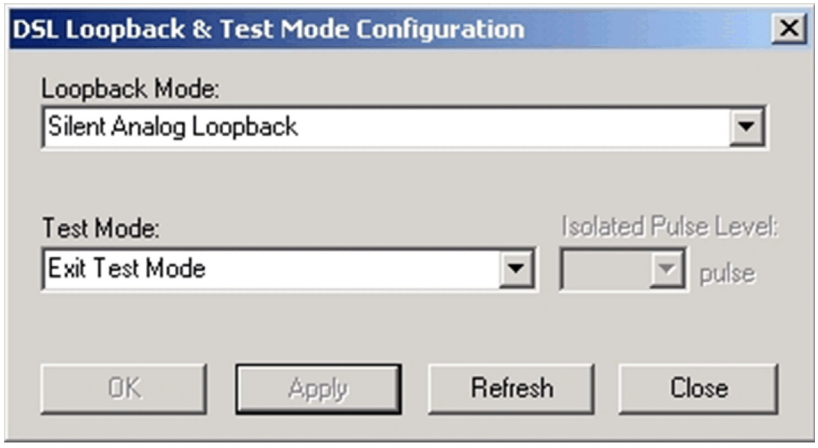


14. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the ZipWirePlus device and it will start training.

3.14.5.2.4 Loopback

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Loopback/Test** button.
3. Set the **Loopback Mode** to **Silent Analog Loopback**.

Figure 3-191. Setting the ZipwirePlus Device into Loopback

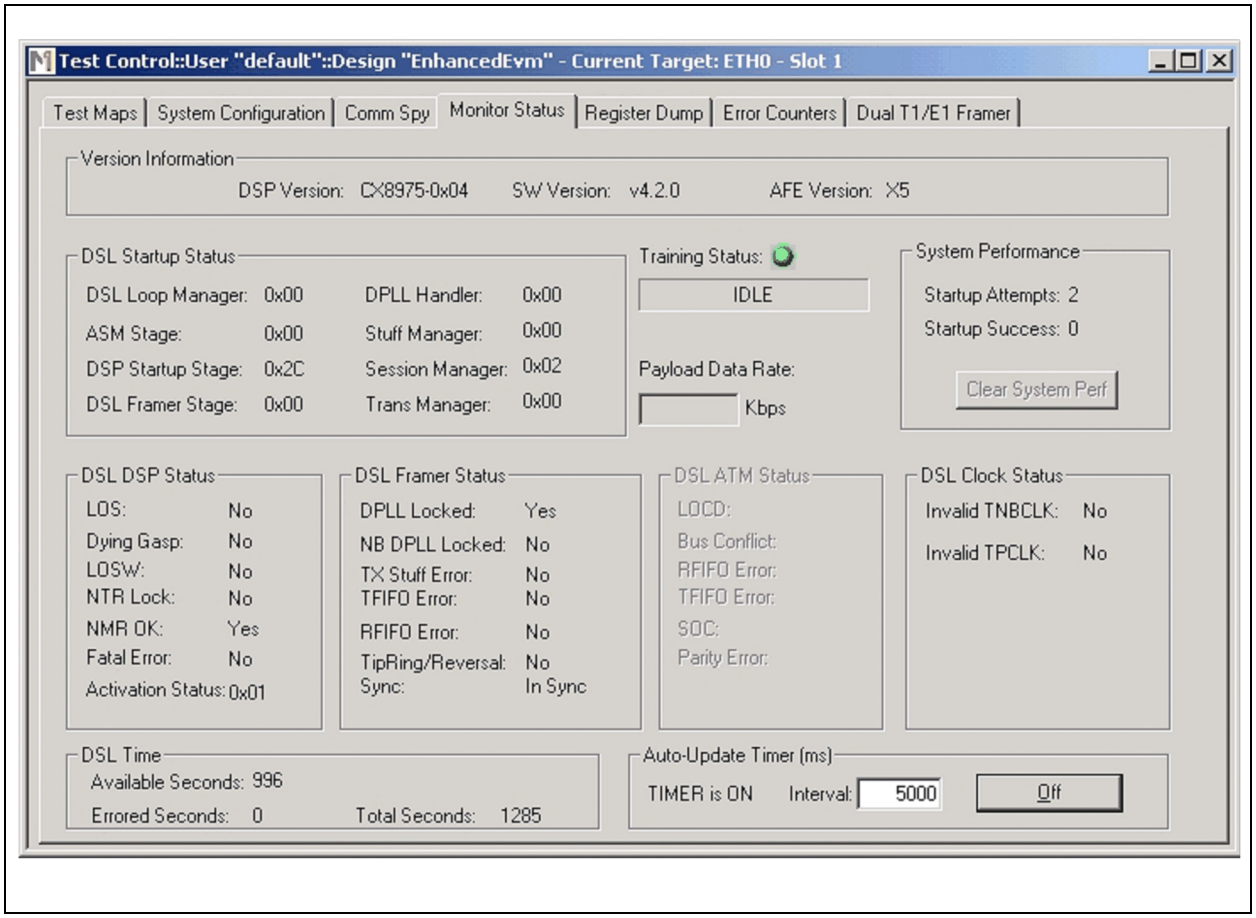


4. Click on the **Apply** button and then click on the Close button.
5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Click on the **Loopback/Test** button.
7. Set the **Loopback Mode** to **Silent Analog Loopback**. Click on the **Apply** button and then click on the **Close** button.

3.14.5.2.5 Monitor the Link

1. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
2. Click on the **Monitor Status** tab.
3. Click the Set button in the **Auto Update Timer** box.
4. Verify that the Training Status is **GREEN** and showing **IDLE** State.

Figure 3-192. Monitoring the ZipWirePlus Device in Loopback



5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2.**
6. Repeat Steps 2 - 4.
7. Verify the Fireberd is in SYNC with no Bit Errors.

3.14.5.3 Varying the PCM Rates

The above configuration transports 32 timeslots of unframed PCM data, 16 timeslots being transported on the Master Loop and 16 timeslots on the Slave Loop. The user

can vary the rates for PCM . Please note that the user would need to set the water level for the PCM traffic. This can be done through the Comm Spy window in the TestExec using the API _DSL_PCM_WATER_LEVEL (0x2C) on both the Master and Slave ZipWirePlus devices.

Table 3-1. Water Level Settings for Multi-pair Unframed PCM Application

PCM Rate	DSL Rate	Water Level
384Khz	192K+8k	00 30 00 30 00
512Khz	256K + 8k	00 40 00 40 00
640Khz	320K+8k	00 40 00 40 00
768Khz	384K+8k	00 40 00 40 00
896Khz	448K+8k	00 40 00 40 00
1024Khz	512K+8k	00 80 00 80 00
1152Khz	576K+8k	00 80 00 80 00
1280Khz	640K+8k	00 80 00 80 00
1408Khz	704K+8k	00 80 00 80 00
1536Khz	768K+8k	00 80 00 80 00
1664Khz	832K+8k	00 80 00 80 00
1792Khz	896K+8k	00 C0 00 C0 00
1920Khz	960K+8k	00 80 00 80 00
2048Khz	1024K+8k	00 F0 00 F0 00
2176Khz	1088K+8k	00 80 00 80 00
2304Khz	1152K+8k	00 F0 00 F0 00
2432Khz	1216K+8k	00 80 00 80 00
2560Khz	1280K+8k	00 80 00 80 00
2688Khz	1344K+8k	00 80 00 80 00
2816Khz	1408K+8k	00 80 00 80 00
2944Khz	1472K+8k	00 80 00 80 00
3072Khz	1536K+8k	00 80 00 80 00
3200Khz	1600K+8k	00 80 00 80 00
3328Khz	1664K+8k	00 80 00 80 00
3456Khz	1728K+8k	00 80 00 80 00
3584Khz	1792K+8k	00 80 00 80 00

3712Khz	1856K+8k	00 B0 00 B0 00
3840Khz	1920K+8k	00 B0 00 B0 00
3968Khz	1984K+8k	00 B0 00 B0 00
4096Khz	2048K+8k	00 F0 00 F0 00
4224Khz	2112K+8k	00 B0 00 B0 00
4352Khz	2176K+8k	00 D0 00 D0 00
4480Khz	2240K+8k	00 D0 00 D0 00
4608Khz	2304K+8k	00 F0 00 F0 00

3.14.6 End to End Testing Using Two Enhanced EVMs

For end to end testing, one additional Enhanced EVM is needed.

3.14.6.1 Enhanced EVM Setup for HTU-R Side

1. Place the Enhanced EVM on a bench.
2. Ensure the ZipWirePlus LICs are plugged into Slot 1(HTU-C) and Slot 2(HTU-R) respectively. The BNC Tester card should be plugged into Slot 3.
3. Connect the RJ-11 to Serial port cable from the COM port on the PC to the RJ-11port J9 located on the Microprocessor Board on the Enhanced EVM. Start a serial port session using hyperterm/teraterm. The Serial Communication Port settings should be Baud Rate 9600, Data 8 bit, Parity None, Stop 1 bit, Flow Control None.
4. Connect an Ethernet cable to the RJ45 port J8 located on the Microprocessor Board of the Enhanced EVM. This port shall be used for the TestExec(UIP) as well as the code download.
5. Designate the ZipWirePlus LIC in Slot 1 as the Master HTU-C and the ZipWirePlus LIC in Slot 2 as the Slave HTU-C. Later in the setup procedure, these units need to be configured the same way using the User Interface Program (UIP).
6. Hardware Modifications - Connect the TPMFSYNC (pin 5 of J28) of the ZipWirePlus Master LIC (Slot 1) to the TPMFSYNC (pin 5 of J28) of the ZipWirePlus Slave LIC (Slot 2).
7. Fireberd Connections - Make the following connections
   - TX0DAT (BNC Tester) to RX0DAT (BNC Tester)
   - TX0CLK (BNC Tester) to RX0CLK (BNC Tester)
8. Power Supply Connection - Connect the power supply brick (provided) to AC Power. Plug the DC power outlet into plugs into J9 of the Enhanced EVM.
9. Set up for Zero Loop Length

   a) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Master Slot 1) to J7 of the ZipWirePlus LIC(HTU-R Master Slot 1) of this Enhanced EVM.

b) Connect the RJ-45 cable(provided) from J7 of ZipWirePlus LIC (HTU-C Slave Slot 2) to J7 of the ZipWirePlus LIC(HTU-R Slave Slot 2) of this Enhanced EVM.

3.14.6.2 Fireberd #2 Setup

Configure the Fireberd as defined in Section 3.3.2

3.14.6.3 TestExec

3.14.6.3.1 Installation and Configuration

Please refer to Section 3.2.5.1 for detailed procedure for installing the configuring the TestExec(UIP) software.

Assuming the same PC is being used to control both HTU-C & HTU-R, we will use the **EnhancedEvm2** design file for the HTU-R Enhanced EVM.

3.14.6.3.2 Enhanced EVM Configuration

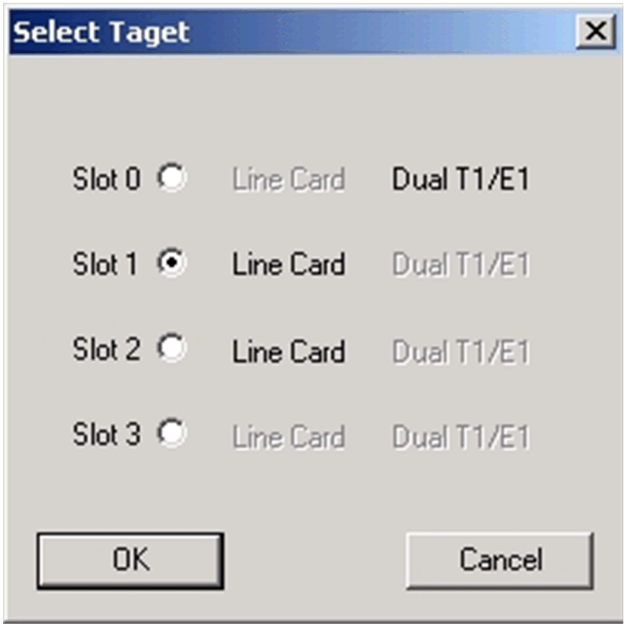
1. Run the Testexec.exe from the desktop.
2. Click on the **Load** button to load the design file.
3. The Test Exec will prompt you with a menu containing 3 design files

   a.**EnhancedEvm**

   b.**EnhancedEvm2**

   c.**LegacyEvm**
4. Select the **EnhancedEvm2** design file. The TestExec will load the selected design file.
5. Click on the **System Configuration** Tab.
6. Download the firmware to the ZipWirePlus devices. Please refer to Section 3.2.5.2.1for more details.
7. The Enhanced EVM has four slots - starting from zero. Select the slot to be configured by right clicking the mouse. The following menu appears.

Figure 3-193. Selecting the Slot



8. Select **Slot 1**.

3.14.6.3.3 Slot 1 (HTU-R Master)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Master card. Please refer to Section 3.3.5.2.2.

3.14.6.3.4 Slot 2 (HTU-R Slave)

1. Click on the **System Configuration** Tab.
2. Set the **Terminal Type** to be **HTU-R**.
3. The rest of the configuration is exactly the same as HTU-C Slave card. Please refer to Section 3.3.5.2.3.

3.14.6.3.5 Loop Activation

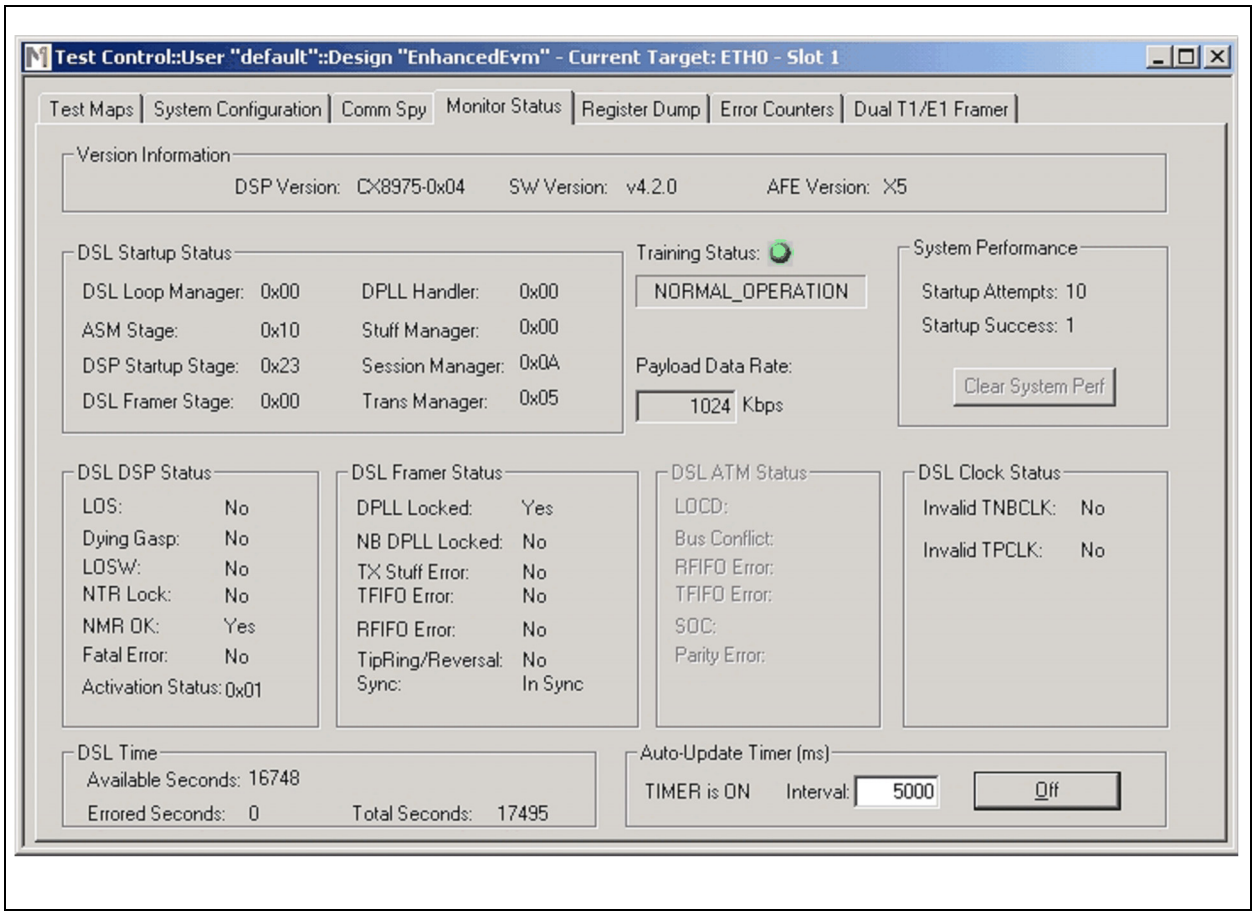
1. Go to the TestExec GUI for HTU-C EVM.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Now take the HTU-C Master out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
4. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Master ZipWirePlus device and it will start training.

5. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
6. Now take the HTU-C Slave out of loopback by setting the **Activation Status Request** to **Disabled** on the Main **System Configuration** Menu. This will disable the ZipWirePlus device and take it out of loopback.
7. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-C Slave ZipWirePlus device and it will start training.
8. Go to the TestExec GUI for HTU-R EVM.
9. Change to slot 1 by right clicking the mouse button and selecting Slot 1.
10. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Master ZipWirePlus device and it will start training.
11. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
12. Set the **Activation Status Request** to **Enabled** on the Main **System Configuration** Menu. This will enable the HTU-R Slave ZipWirePlus device and it will start training.

3.14.6.3.6 Monitor the Link

1. Go the HTU-C TestExec GUI.
2. Change to slot 1 by right clicking the mouse button and selecting **Slot 1**.
3. Click on the **Monitor Status** tab.
4. Click the **Set** button in the **Auto Update Timer** box.
5. Verify that the **Training Status** is **GREEN** and showing **NORMAL OPERATION** State.

Figure 3-194. Monitoring the DSL Link



6. Change to slot 2 by right clicking the mouse button and selecting **Slot 2**.
7. Repeat Steps 2 - 4.
8. Verify the Fireberds are in SYNC with no Bit Errors.

3.14.6.4 Evaluate Loop Performance

You are now ready to evaluate the loop performance on your Enhanced EVM systems. To do this, disconnect the zero loop length between HTU-C and HTU-R ZipWirePlus LICs. Connect the HTU-C and HTU-R through a line simulators using RJ-45 cables (provided) as shown in the Figure 3-178. The modems are configured to automatically train if the DSL link is opened or DSL length is changed. Therefore there is no requirement for the user to issue a retrain from the TestExec (UIP).

4.0 Hardware Identification

4.1 Aurora Motherboard Identification

The Enhanced EVM kit contains one Aurora motherboard. The Aurora mother board supplies the necessary regulated voltages to the LICs, Dual T1/E1 Framer card, and Elgin Microprocessor board.

In addition, the FPGA on the Aurora motherboard provides the bus conversation between the microprocessor bus and the host interface bus of the interface cards, and the flexibility to configure the board through the FPGA to provide multiple modes of operation such as single, multi-pair, and repeater. Figures 4-1 and 4-2 show the Aurora Motherboard Block Diagram and the board assembly, respectively.

Figure 4-1. Aurora Motherboard Block Diagram

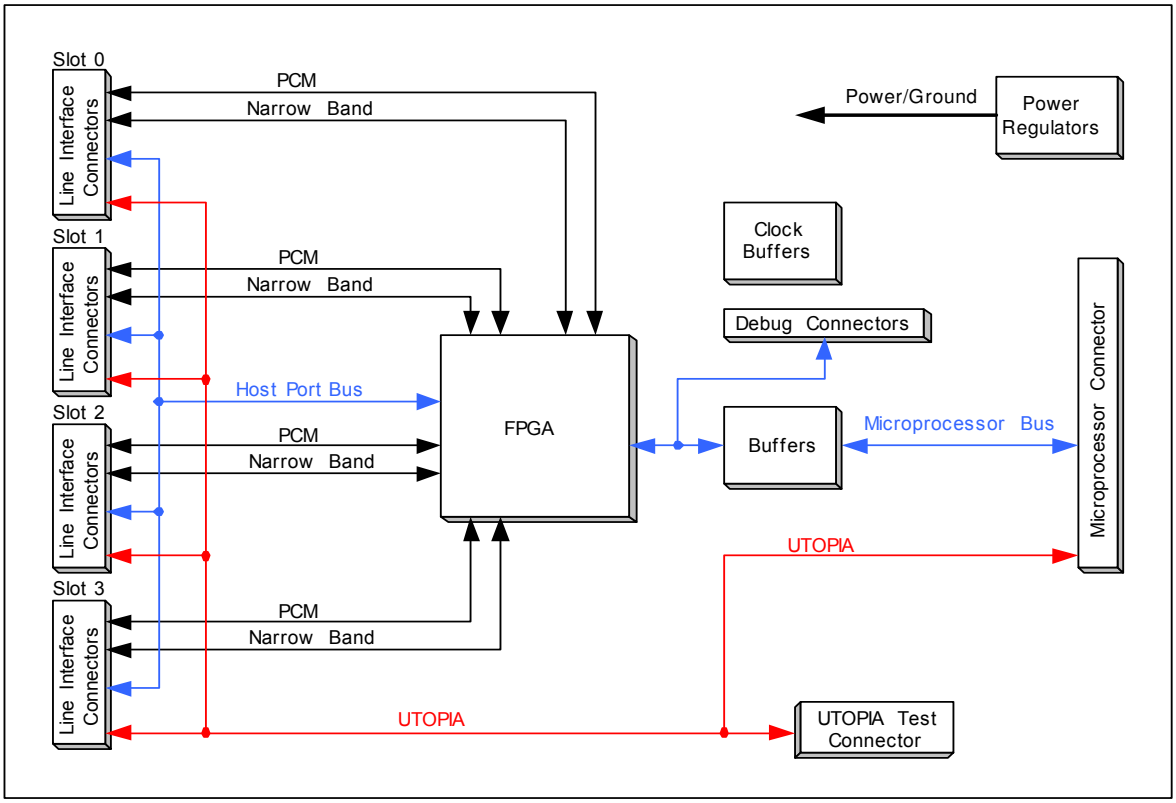
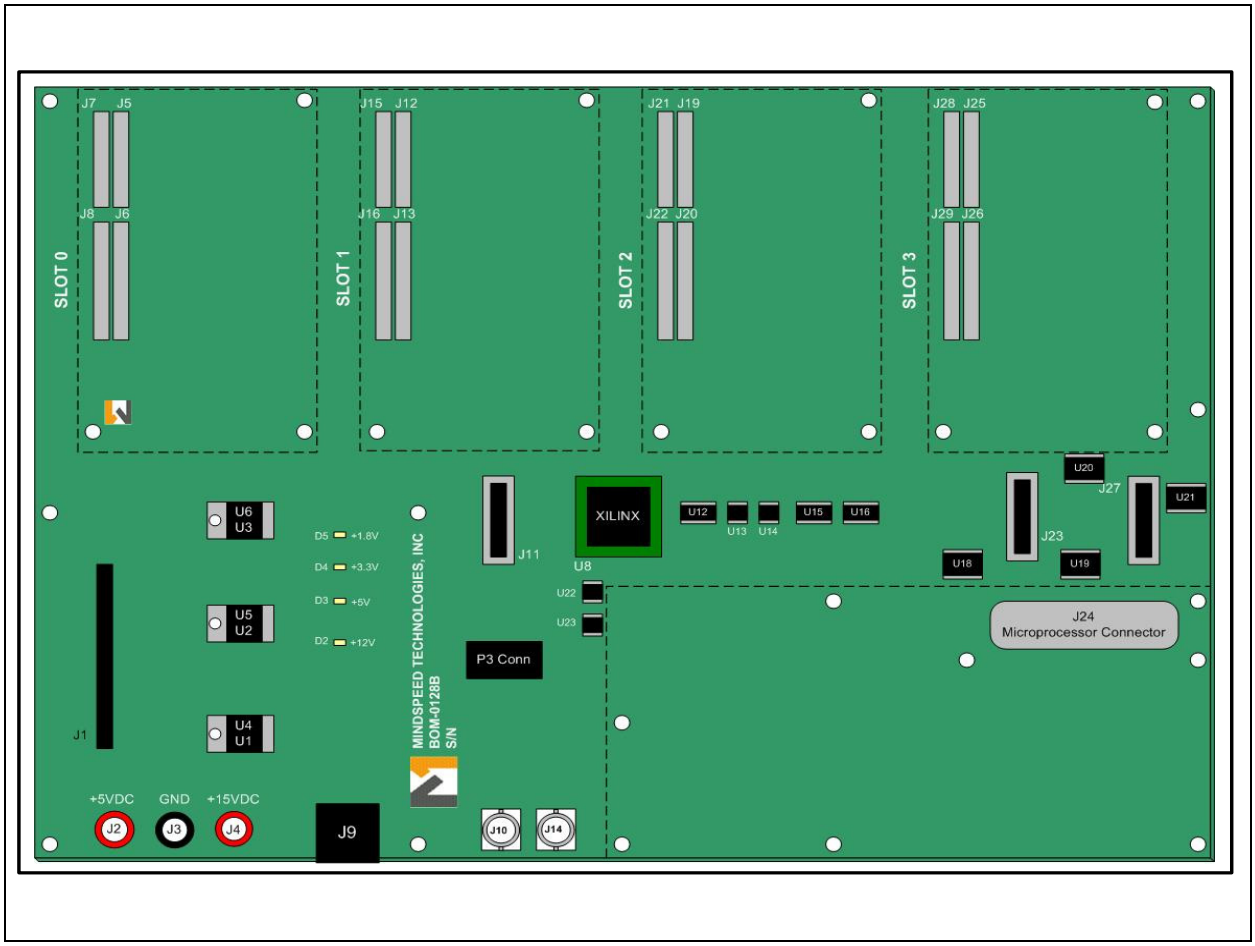


Figure 4-2. Aurora Mother Board Assembly



4.1.1 Power and Ground

The Aurora power is supplied by a 15 V and 5 V Dual Power Supply brick by connecting through the J9 connector. The power supply brick requires a universal voltage input of 90–240 VAC, 50–60 Hz.

A bench power supply can also be used to provide power to the Aurora board by connecting 5V to the J2 connector and 15 V to the J4 connector.

The 15 V and 5 V inputs are regulated down to +12 V and +3.3 V respectively by adjustable Linear LDO regulators. The +1.8 V output is generated from +3.3 V to have the correct power-up sequencing. Four on-board LEDs, D2–D5, indicate nominal power levels for each of the required voltages, respectively.

4.2 Aurora Interface Signals

The ZipWirePlus LIC interface is achieved through various user-accessible connectors on the Aurora motherboard. These connectors contain the following signal groups:

- Power/Ground — 15 VDC x 5 VDC
- Clocks — Device Input clock, Network Reference Clock, and so on.
- UTOPIA Level II bus

4.2.1 UTOPIA II Interface

Connector J1 can be used to access the UTOPIA II bus. J1 acommodates a cobalt UE-FZ ATM tester with a UTEC-16A interface connector. Connector J1 is Berg part number 84699-640.

4.2.2 BNC Connectors (Clock Interface)

The Aurora board contains two BNC connectors that enable connections the the DEV_REF_CLK (J14) and NET_REF_CLK (J10) signals. The DEV_REF_CLK connector is provided to insert an external device clock or utilize the buffered device clock output. Access to the XTLI or XTL_B pins is selectable through JP7 on the ZipWirePlus LIC. The NET_REF_CLK connector is provided to supply an external 8 kHz reference clock or to utilize the 8 kHz network reference clock provided by the ZipWirePlus DSP/Framer.

4.3 Elgin Microprocessor Board Identification

The following list provides an overview of the Elgin Microprocessor board capabilities and responsibilities.

- Controls ZipWirePlus via host port interface
- Controls external devices, such as Bt8370, LEDs, DIP switches, etc.
- Controls FPGA(U11) on the Aurora board to configure multiple modes of operation such as single, multipair, and repeater.
- ATM data processing:
  - Compliant with ATM forum UNI 4.0
  - UTOPIA Level II bus to ZipWirePlus device
  - Cell processing up to 50–70 Mbps at 50 MHz system clock
  - Support AAL5 and AAL0 protocols
  - Support constant bit rate (CBR), unavailable bit rate (UBR), and available bit rate (ABR)
- Fast Ethernet support
- Four serial communication controllers (SCC)

Figures 4-3 and 4-3 show the Elgin Board Block Diagram and Assembly, respectively.

Figure 4-3. Elgin Microprocessor Board Block Diagram

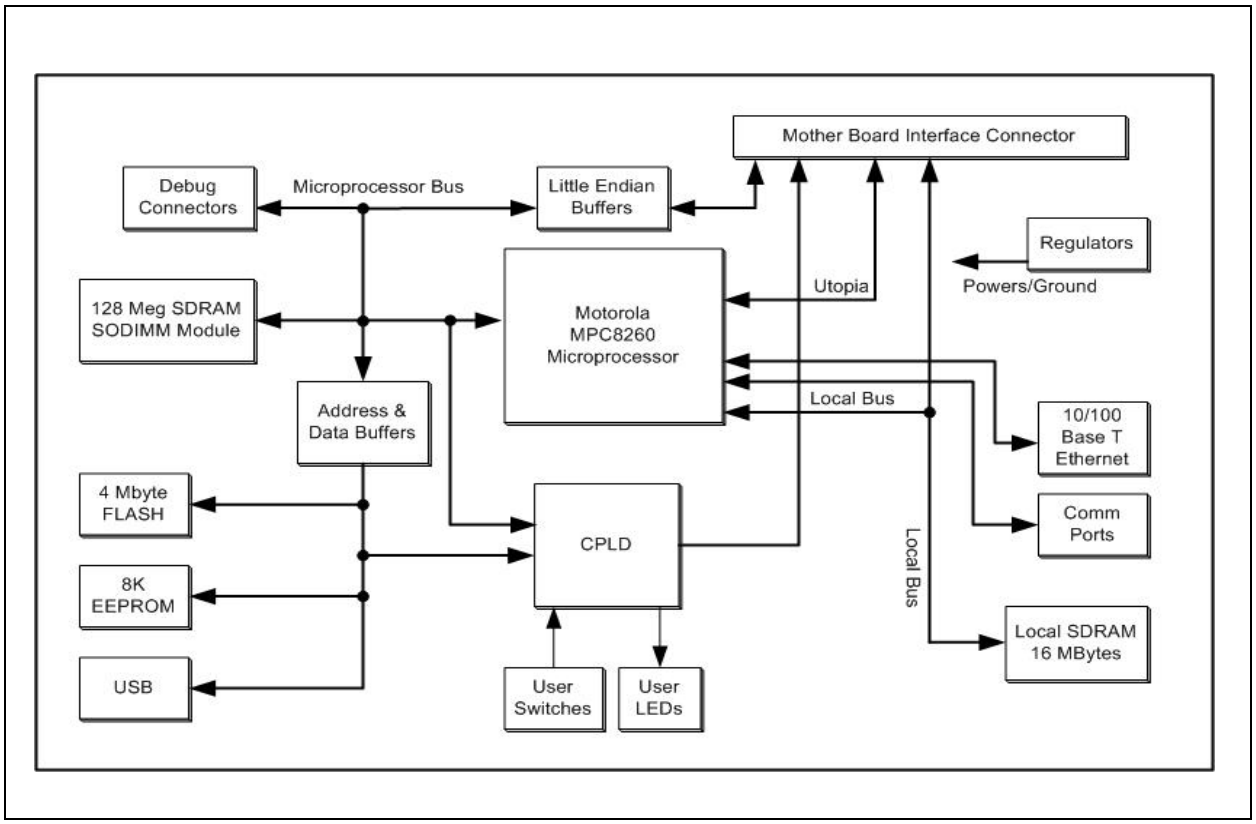
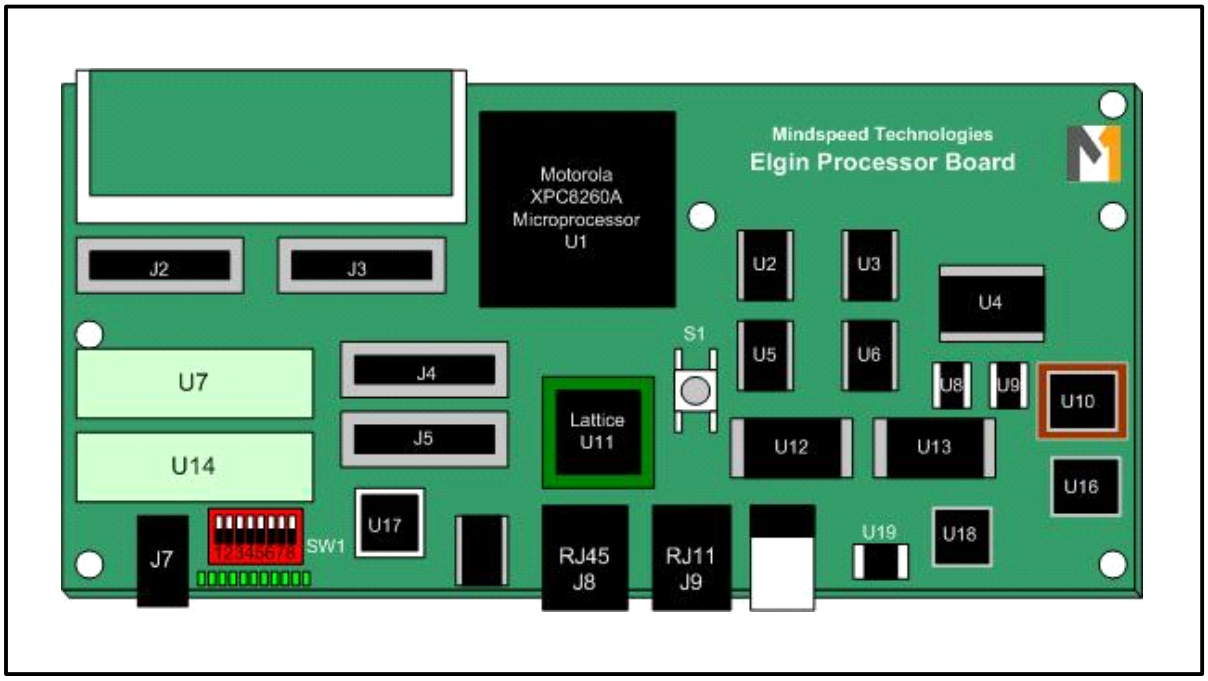


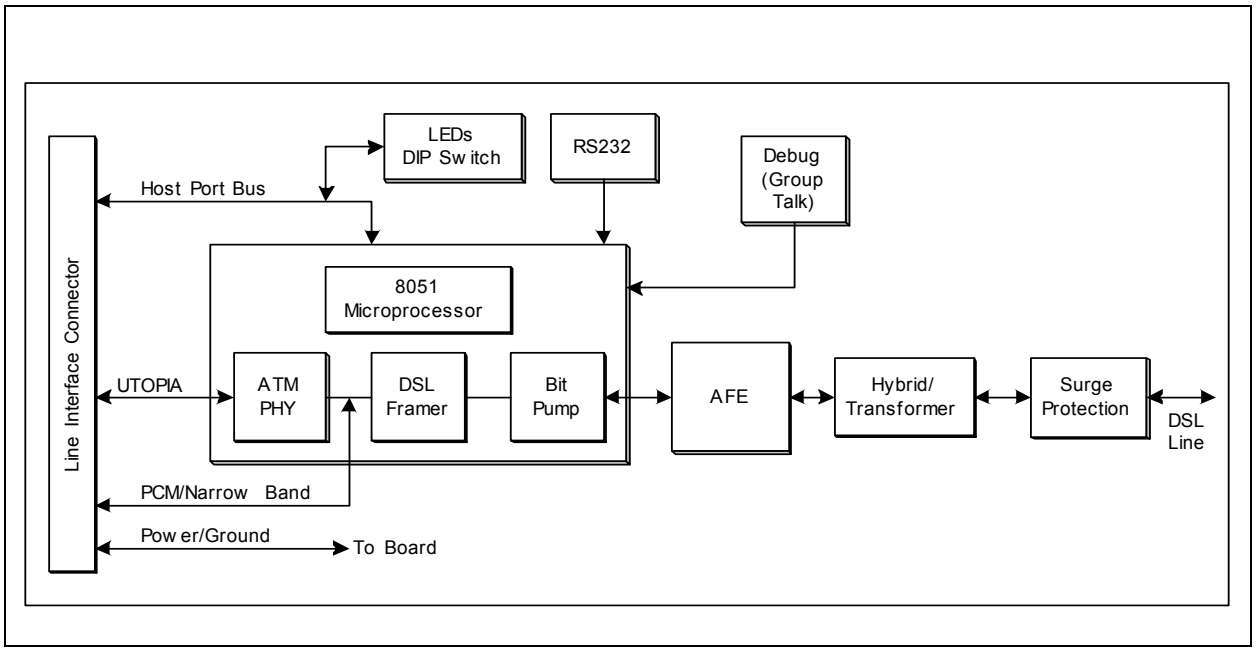
Figure 4-4. Elgin Microprocessor Board Assembly



4.4 ZipWirePlus Line Interface Card (LIC)

Figure 4-5 is a block diagram of the line interface card.

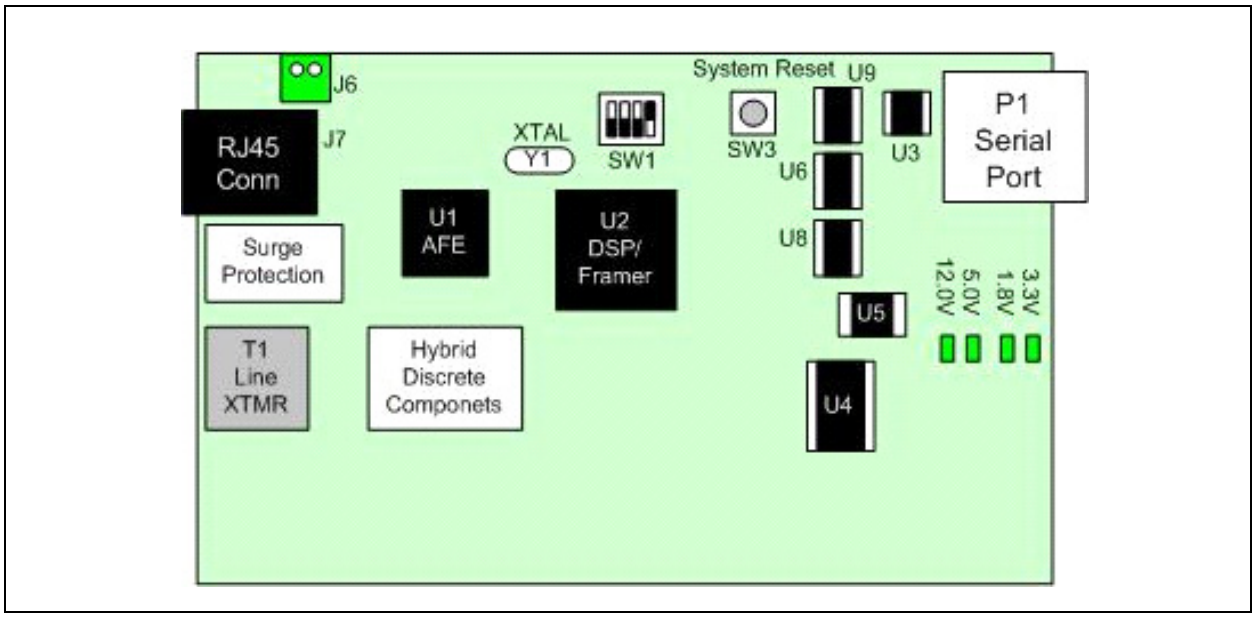
Figure 4-5. Line Interface Card Block Diagram



4.4.1 LIC Identification

Figure 4-6 illustrates the LIC board assembly.

Figure 4-6. Line Interface Card Assembly



4.4.2 ZipWirePlus LIC JTAG

The ZipWirePlus JTAG is accessible through the 10-pin header (J3).

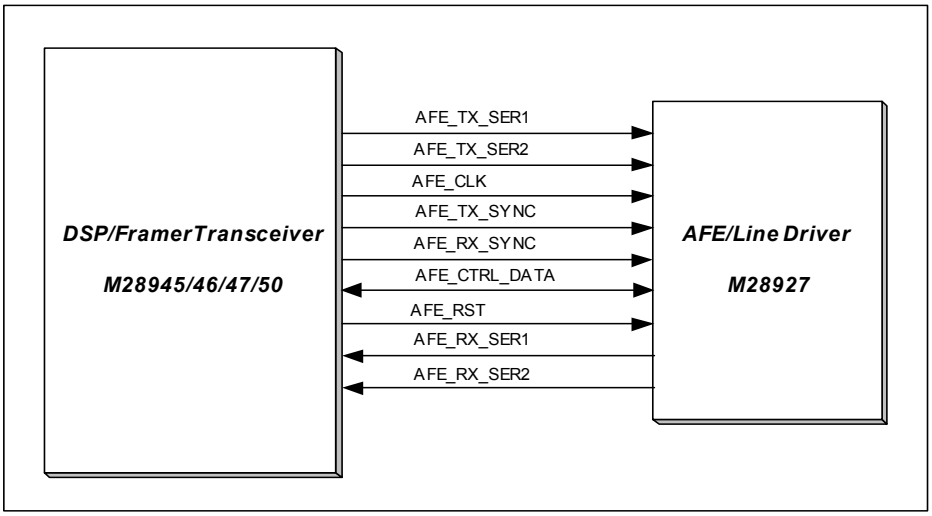
4.4.3 The Serial Port Connection

The UIP/PC and Debug ports are accessible through Connector P1 using a female 9-pin μd connector.

4.5 ZipWirePlus DSP-to-AFE Interface

Figure 4-7 illustrates the ZipWirePlus DSP-to-AFE interface connections.

Figure 4-7. ZipWirePlus DSP-to-AFE Interface Connection



4.6 ZipWirePlus Analog Front End (AFE)

4.6.1 DSL Compromise Hybrid

The DSL Compromise hybrid features an impedance matching network that attempts to match the line impedance. The capacitors found in the AFE section should be NPO- or Polyester-type. Using other capacitor types may result in poor linearity and poor echo canceling performance. The capacitors must be chosen for low dielectric absorption.

4.6.2 DSL Transformer

The transformer used is a Midcom 50772.

4.6.3 DSL Line Interface

The ZipWirePlus EVM provides the DSL line connections through either the RJ-45 (J7) or the 2-pin terminal connector (J6). The RJ-45 and terminal connector pinouts are defined in Table 4-1.

Table 4-1. DSL RJ-45 and Terminal Connector Pinout

Signal	RJ-45 Pin(1)	Terminal Connector Pin
Tx Tip	4	1
Tx Ring	5	2

FOOTNOTE:
(1) Pins 1, 2, 3, 6, 7, and 8 on the RJ-45 are no-connects.

4.6.4 DSL Surge Protection

The ZipWirePlus EVM provides footprints for line- and circuit-side surge protection schemes. The customer may utilize these footprints to add their own surge protection.

4.6.5 DSL Remote Power Feeding

Remote power feeding is not provided on the ZipWirePlus EVM. However, customers can utilize the ZipWirePlus EVM as a prototype board to experiment with their own remote power feeding circuitry.

4.7 Dual T1/E1 Card Identification

Figure 4-8 illustrates a block diagram of the Dual T1/E1 Framer card. This line interface card provides the ability to pass the T1/E1 data to the ZipWirePlus line interface cards. These allow a simple mechanism to connect a Fireberd or other pieces of equipment to test the throughput data. Figure 4-9 shows the card assembly.

Figure 4-8. Dual T1/E1 Card Block Diagram

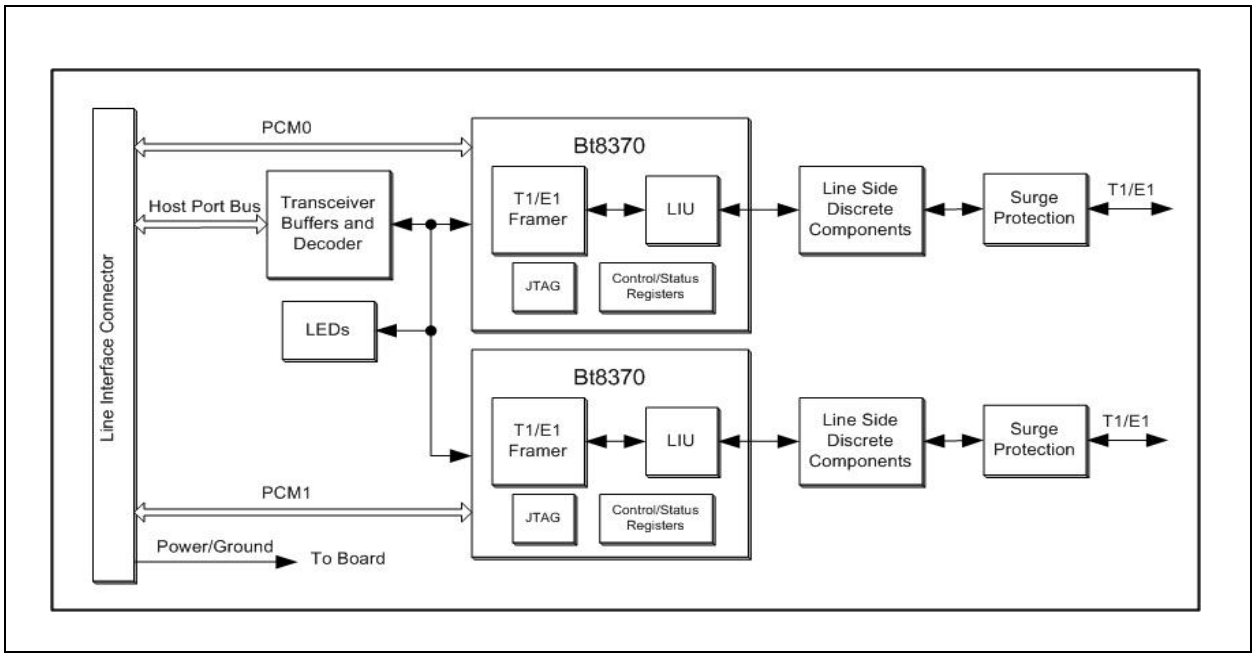
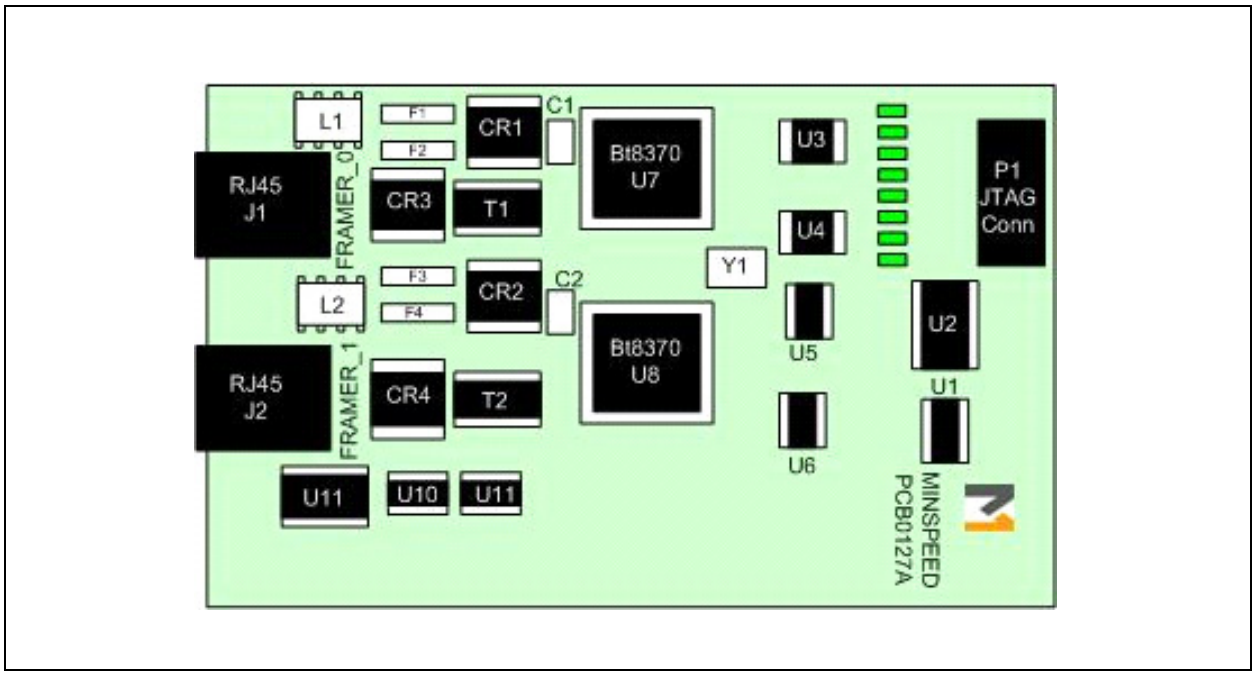


Figure 4-9. Dual T1/E1 Card Assembly



4.8 BNC Tester Card Identification

Each Enhanced EVM kit contains one BNC tester card. The purpose of the BNC tester card is to provide the ability to pass raw clock/data (BNC) to the ZipWirePlus Line Interface Cards without going through the Dual T1/E1 Framer card. Figures 4-10 and 4-11 show the block diagram and assembly of the BNC tester card.

Figure 4-10. BNC Tester Card Block Diagram

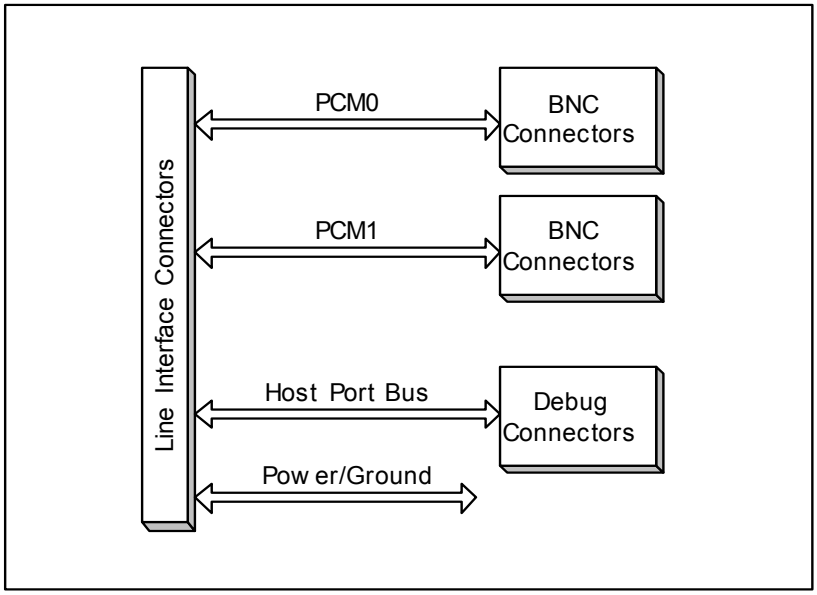
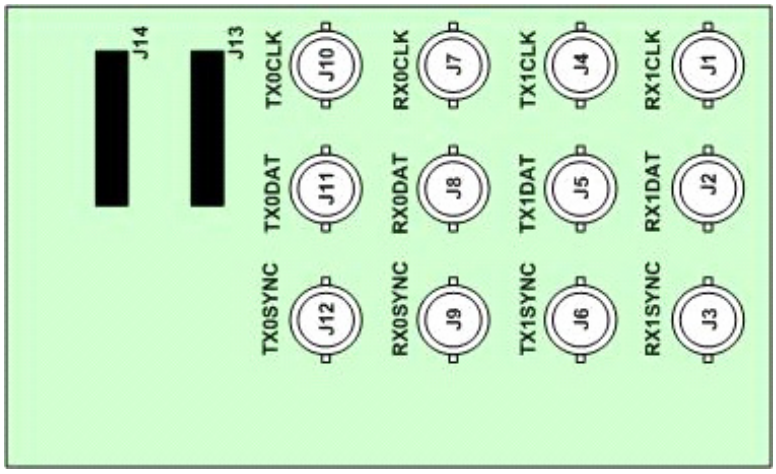


Figure 4-11. BNC Tester Card Assembly



Appendix A: Acronyms and Definitions

2B1Q	2 Binary, 1 Quaternary
AAF	Anti-Alias Filters
ABR	Available Bit Rate
ADC (A/D)	Analog-to-Digital Converter
AFE	Analog Front End
AIS	Alarm Indication Signal
API	Application Programming Interface
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BGA	Ball Grid Array
BP	Bit Pump
BT	Bit Pump Transceiver
CBR	Constant Bit Rate
CMOS	Complimentary Metal-Oxide Semiconductor
CO	Central Office
CPE	Customer Premise Equipment
CRC-N	Cyclic Redundancy Check-N
DAC (D/A)	Digital-to-Analog Converter
DFE	Decision Feedback Equalizer
DIP	Dual In-Line Package
Downstream	From the HTU-C towards the HTU-R (includes regenerators)
DPLL	Digital Phase Lock Loop
DSL	Digital Subscriber Line
DSL Framer	ZipWirePlus DSL Framer Block
DSP	Digital Signal Processing (Processor)
EC	Echo Canceller
EOC	Embedded Operations Channel
ESD	Electrostatic Discharge

EVM	Evaluation Module
FEBE	Far-End Block Error (the far end reported a CRC error)
FEXT	Far-End Cross Talk
FFE	Feed Forward Equalizer
FIFO	First-In, First-Out
FR	Framer
H2TU	HDSL2 Terminal Unit
HDLC	High-Level Data Link Controller
HDSL	High-Bit-Rate Digital Subscriber Line
HEC	Header Error Check
HTU	HDSL Terminal Unit
HTU-C or COT or LTU	Central Office Terminal or Local Terminal Unit
HTU-R or RT or NTU	Remote Terminal or Network Terminal Unit
IDS	International Data Services
LAN	Local Area Network
LED	Light Emitting Diode
LIC	Line Interface Card
LOCD	Loss Of Cell Delineation
LOS	Loss Of Signal
µs	microsecond
ms	millisecond
NEXT	Near-End Cross Talk
OOF	Out Of Frame
P2MP	Point to Multipoint
PAM	Pulse Amplitude Modulation
PCM	Pulse Code Modulation
PLL	Phase Lock Loop
PRA	Primary Rate Access
PRBS	Pseudo-Random Bit Sequence
PSD	Power Spectral Density
RAM	Random Access Memory
ROM	Read-Only Memory
SAR	Segmentation and Reassembly
SCC	Serial Communication Controller
SRC	Segmentation and Reassembly Controller
S/W	Software

TAS	Telecom Analysis Systems
TC	Transmission Convergence
TCM	Time Code Modulation
TQFP	Thin Quad Flat Pack
Transceiver	ZipWirePlus DSP/Transceiver Block
TTC	Telecommunications Technique Corporation
UART	Universal Asynchronous Receive Transmit
UBR	Unavailable Bit Rate
UIP	User Interface Program
Upstream	From the HTU-R towards the HTU-C (includes regenerators)

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