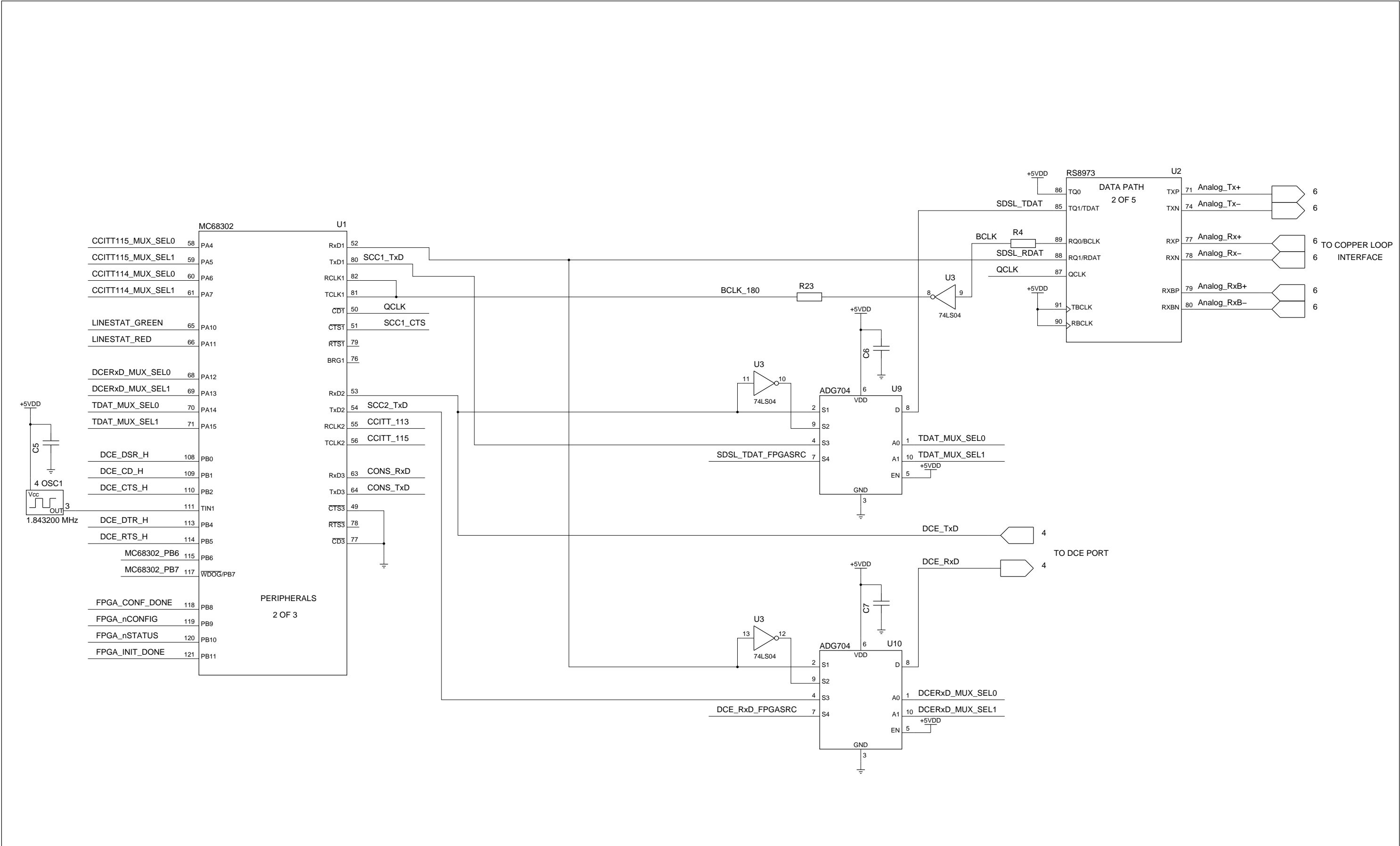


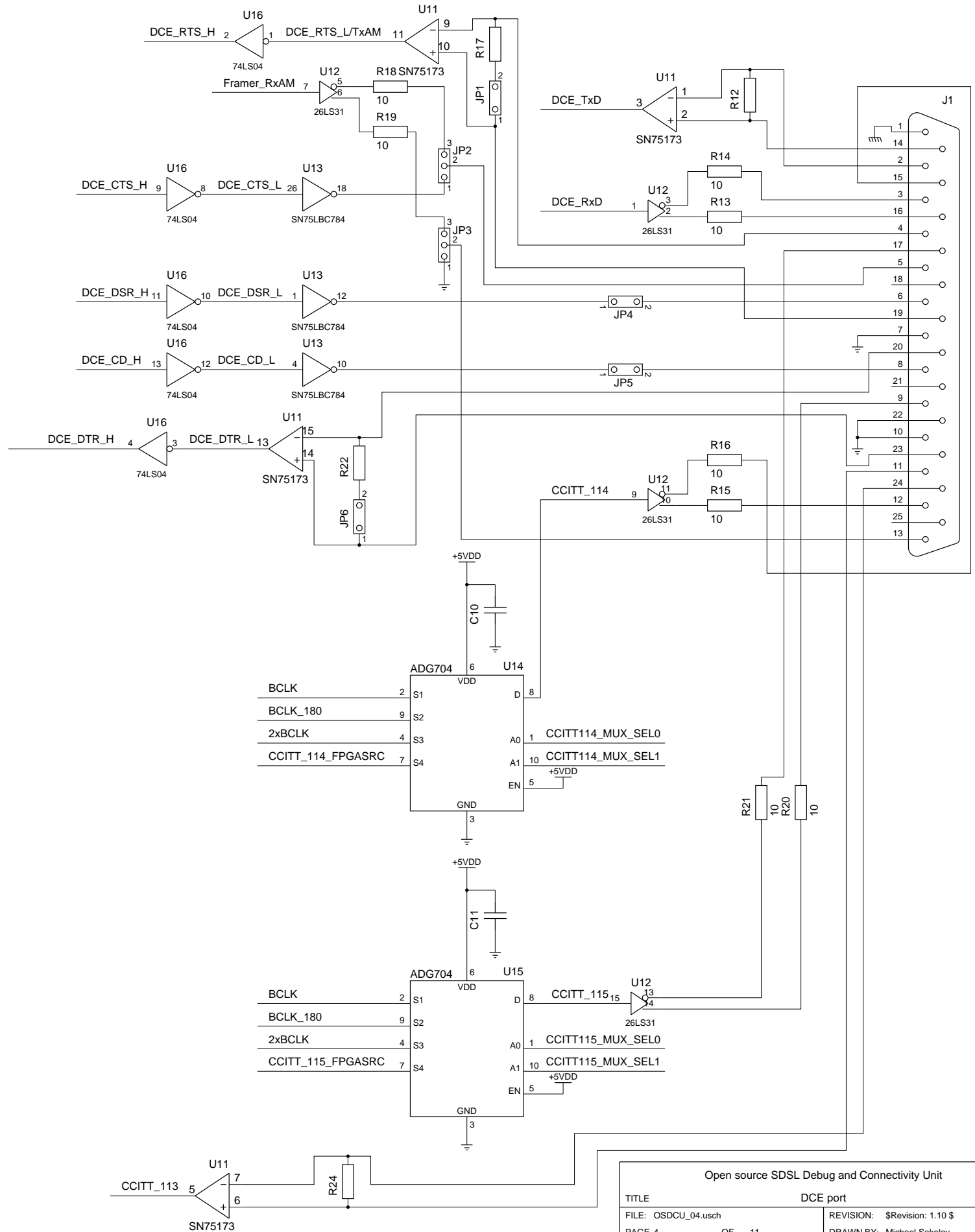
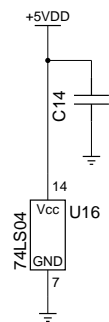
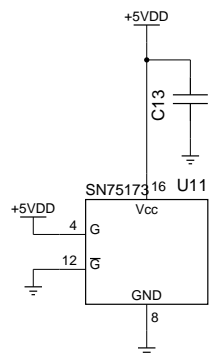
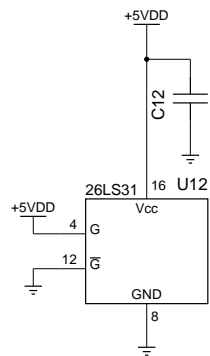
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit			
TITLE		Flash & RAM	
FILE: OSDCU_02.usch		REVISION: \$Revision: 1.3 \$	
PAGE 2	OF 11	DRAWN BY: Michael Sokolov	



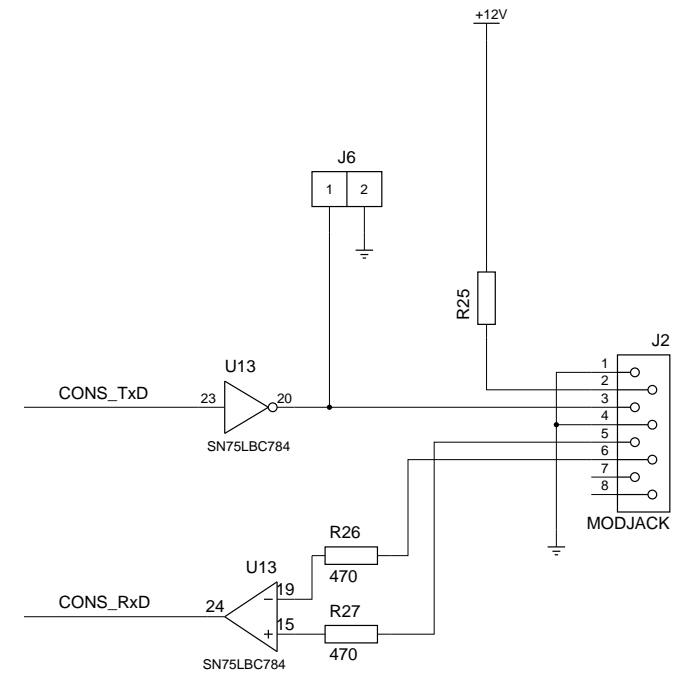
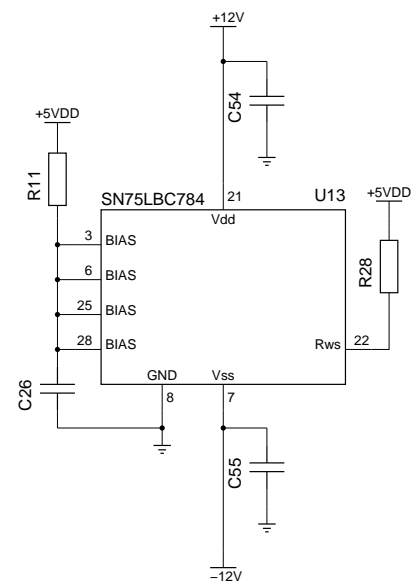
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit			
TITLE		Data path	
FILE: OSDCU_03.usch	REVISION: \$Revision: 1.7 \$		
PAGE 3	OF 11	DRAWN BY: Michael Sokolov	



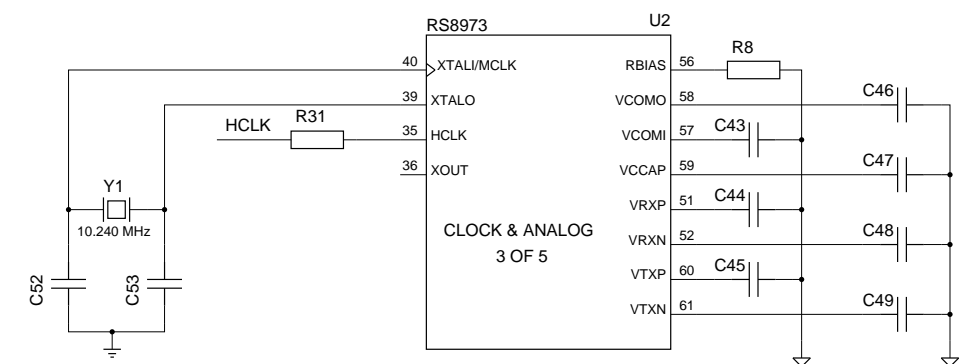
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit		
TITLE		DCE port
FILE: OSDCU_04.usch	REVISION: \$Revision: 1.10 \$	
PAGE 4	OF 11	DRAWN BY: Michael Sokolov

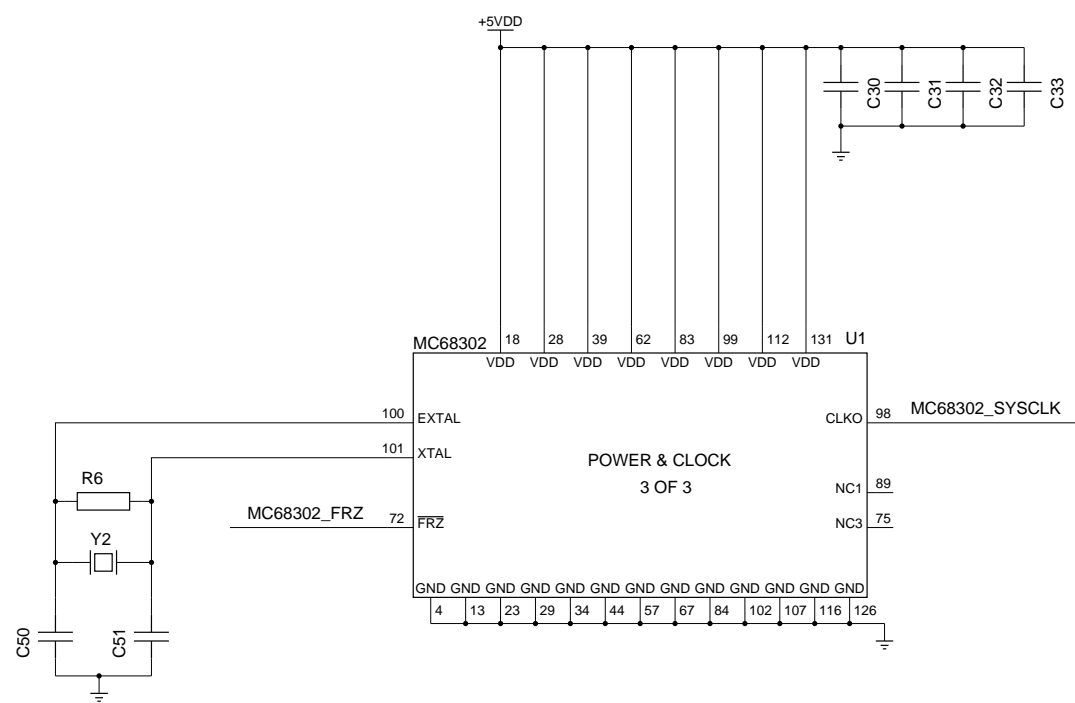
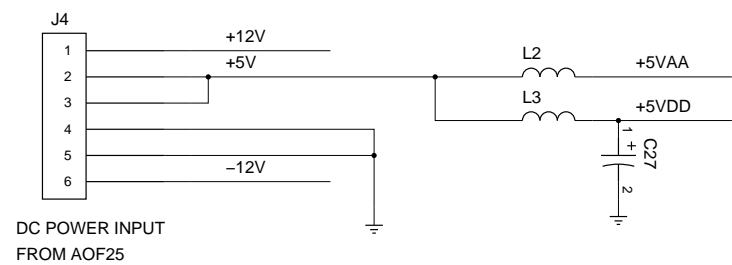
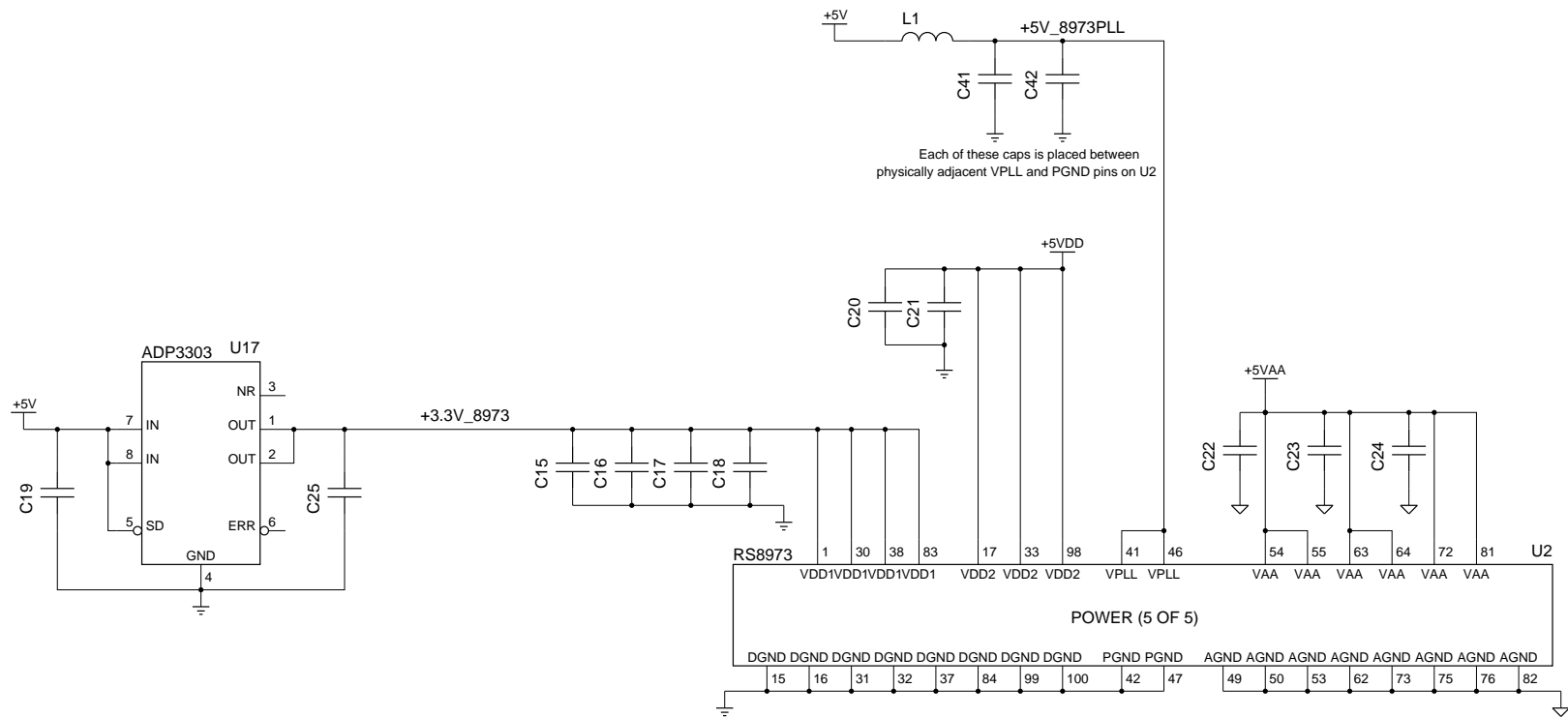


The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit		
TITLE		Console port
FILE: OSDCU_05.usch	REVISION: \$Revision: 1.4 \$	
PAGE 5	OF 11	DRAWN BY: Michael Sokolov

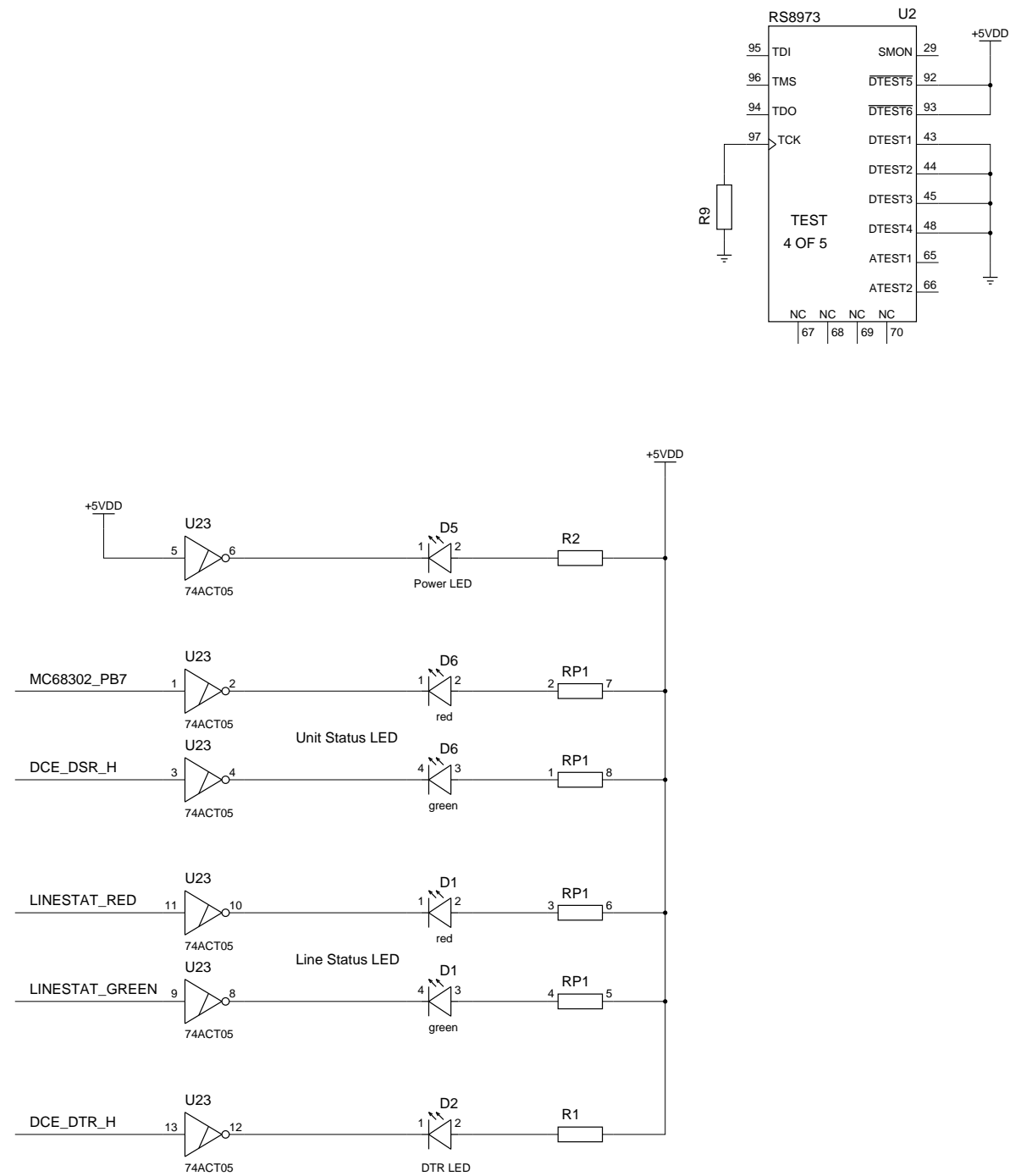
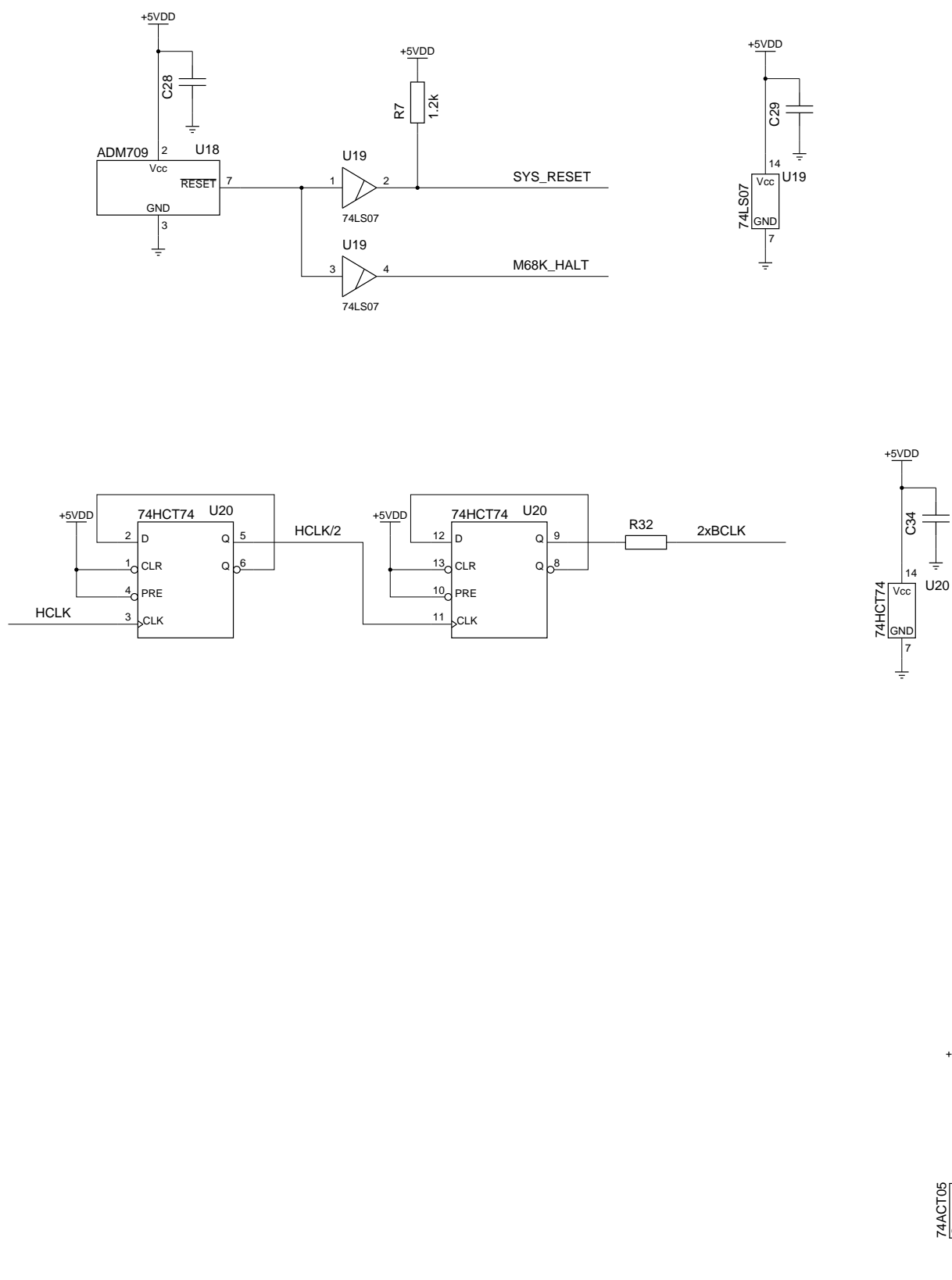


Open source SDSL Debug and Connectivity Unit		
TITLE Copper loop interface		
FILE: OSDCU_06.usch	REVISION: \$Revision: 1.7 \$	
PAGE 6 OF 11	DRAWN BY: Michael Sokolov	



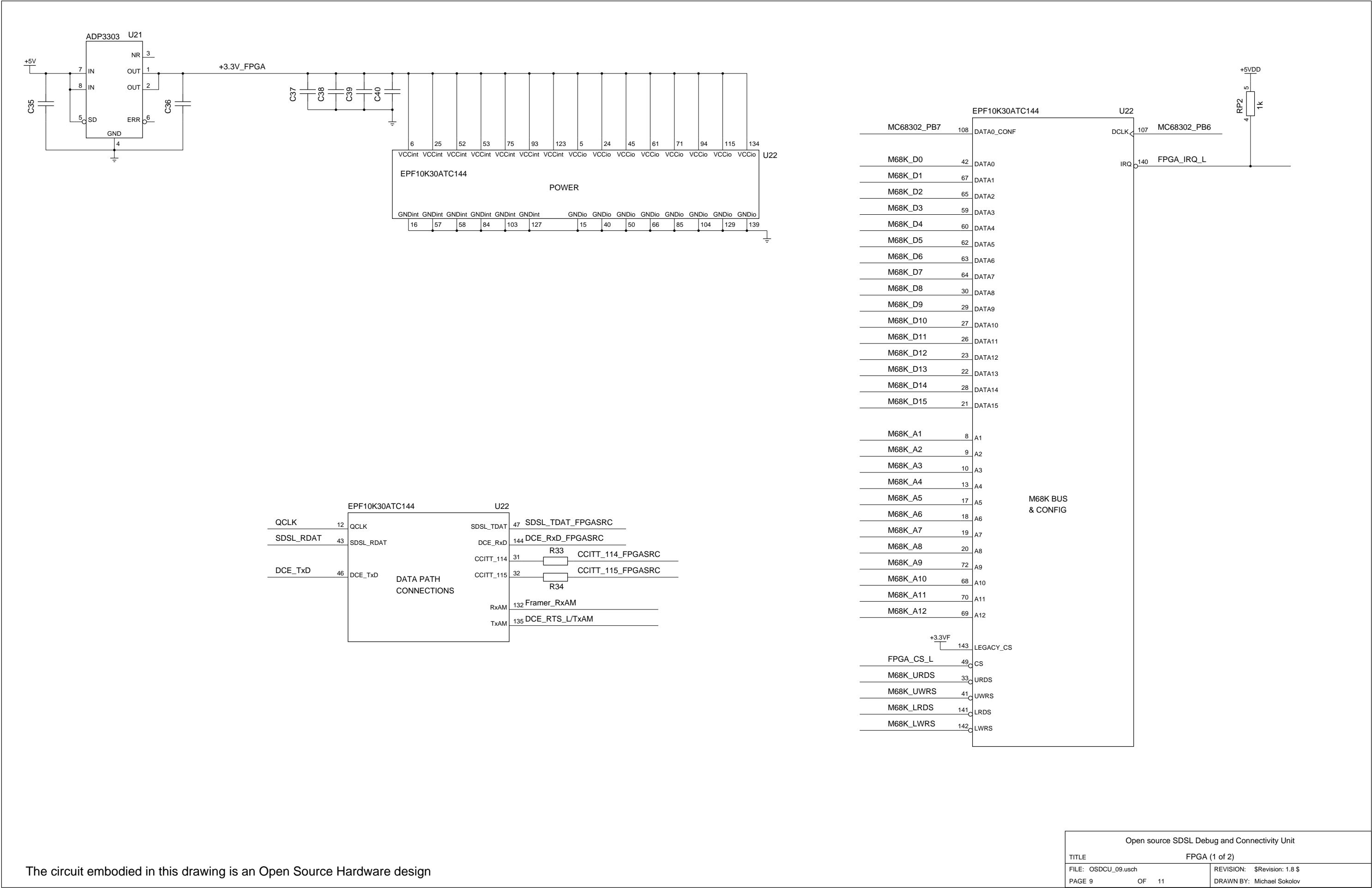
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit			
TITLE		Power	
FILE: OSDCU_07.usch	REVISION: \$Revision: 1.6 \$		
PAGE 7	OF 11	DRAWN BY: Michael Sokolov	

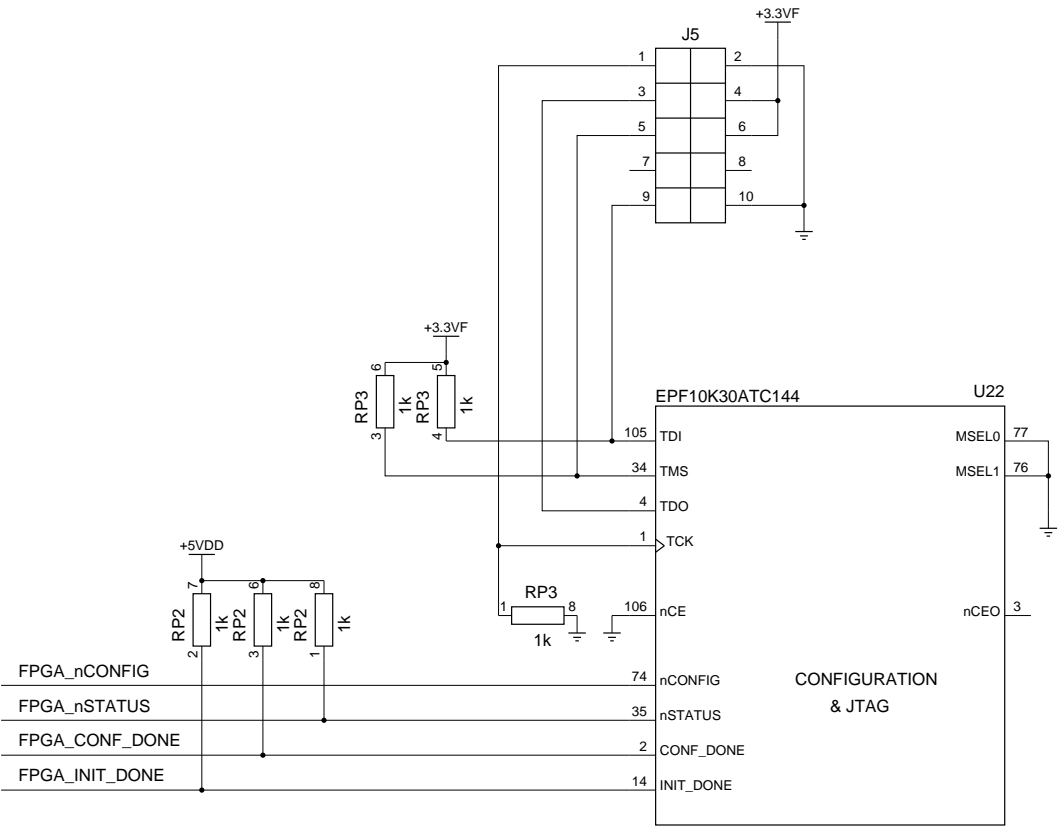
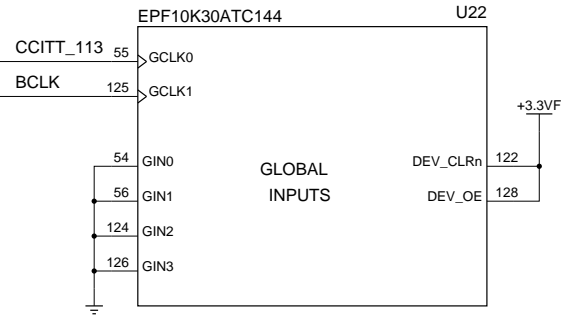


The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit		
TITLE Miscellaneous		
FILE: OSDCU_08.usch	REVISION: \$Revision: 1.6 \$	
PAGE 8	OF 11	DRAWN BY: Michael Sokolov

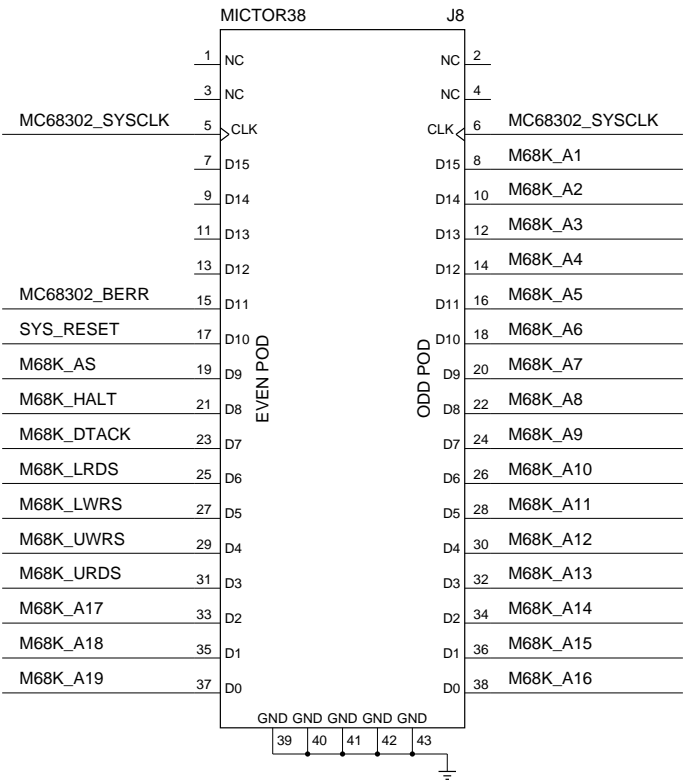
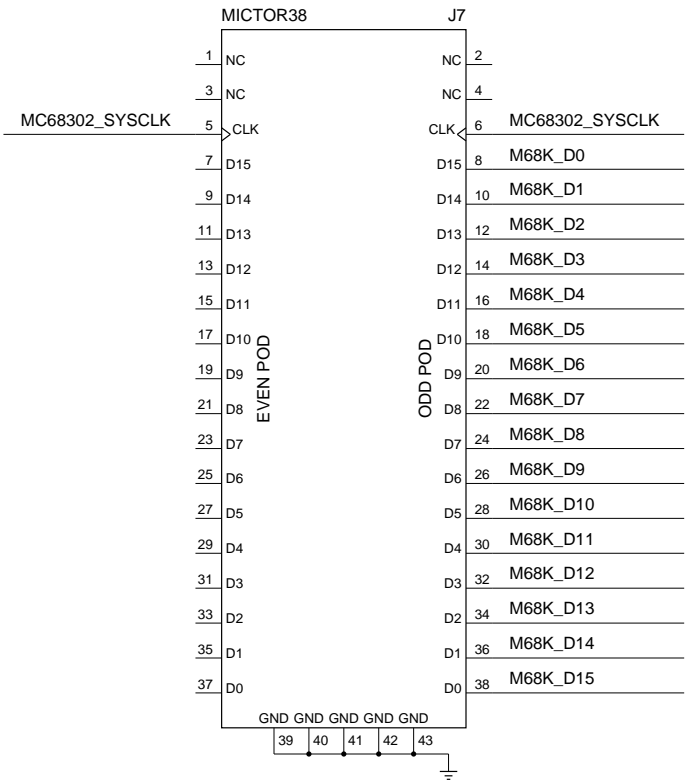


The circuit embodied in this drawing is an Open Source Hardware design



The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit		
TITLE FPGA (2 of 2)		
FILE: OSDCU_10.usch	REVISION: \$Revision: 1.9 \$	
PAGE 10	OF 11	DRAWN BY: Michael Sokolov



The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit		
TITLE		Debug
FILE: OSDCU_11.usch		REVISION: \$Revision: 1.1 \$
PAGE 11	OF 11	DRAWN BY: Michael Sokolov