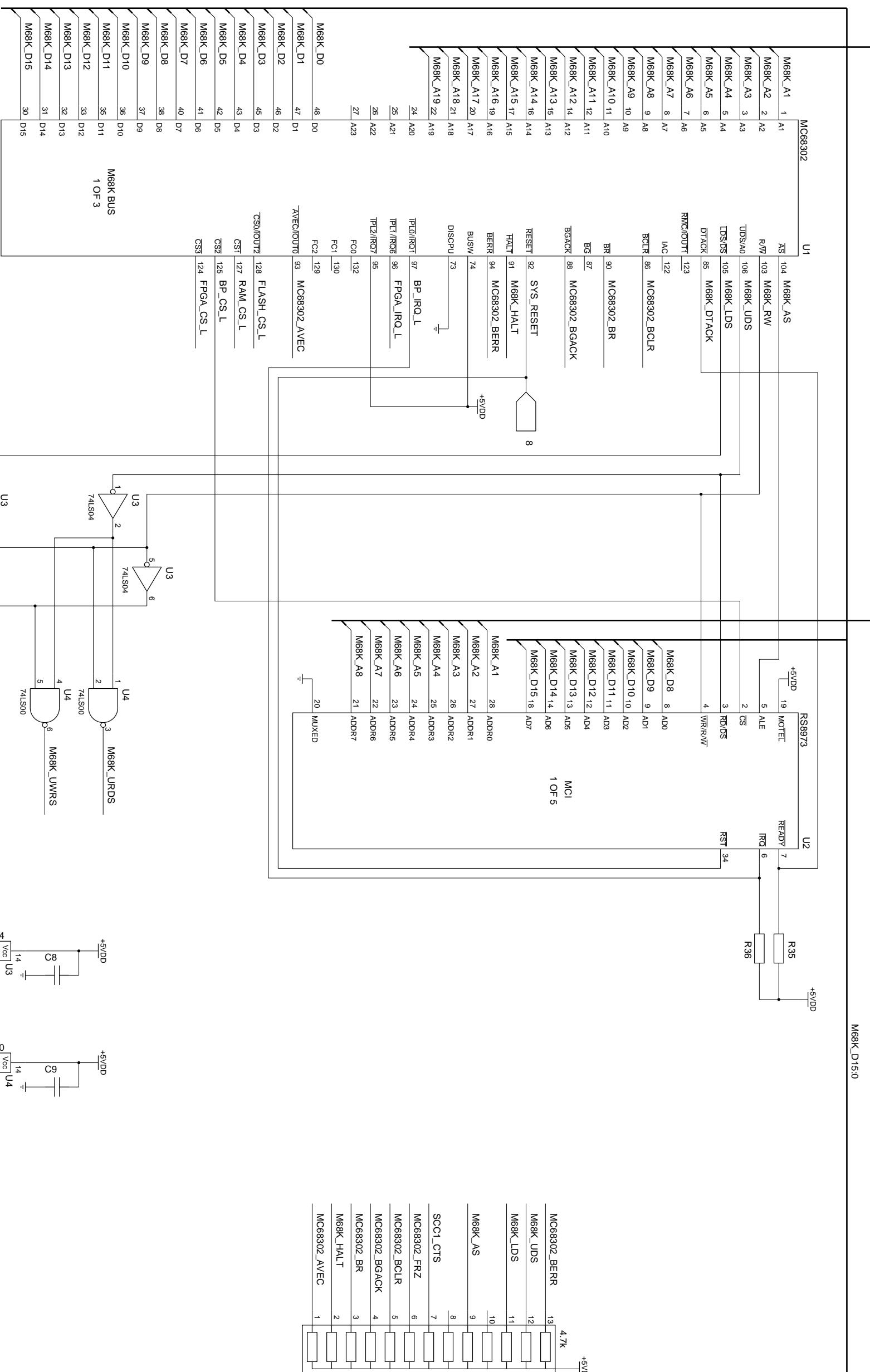


M68K_A19_1

M68K_D15_0

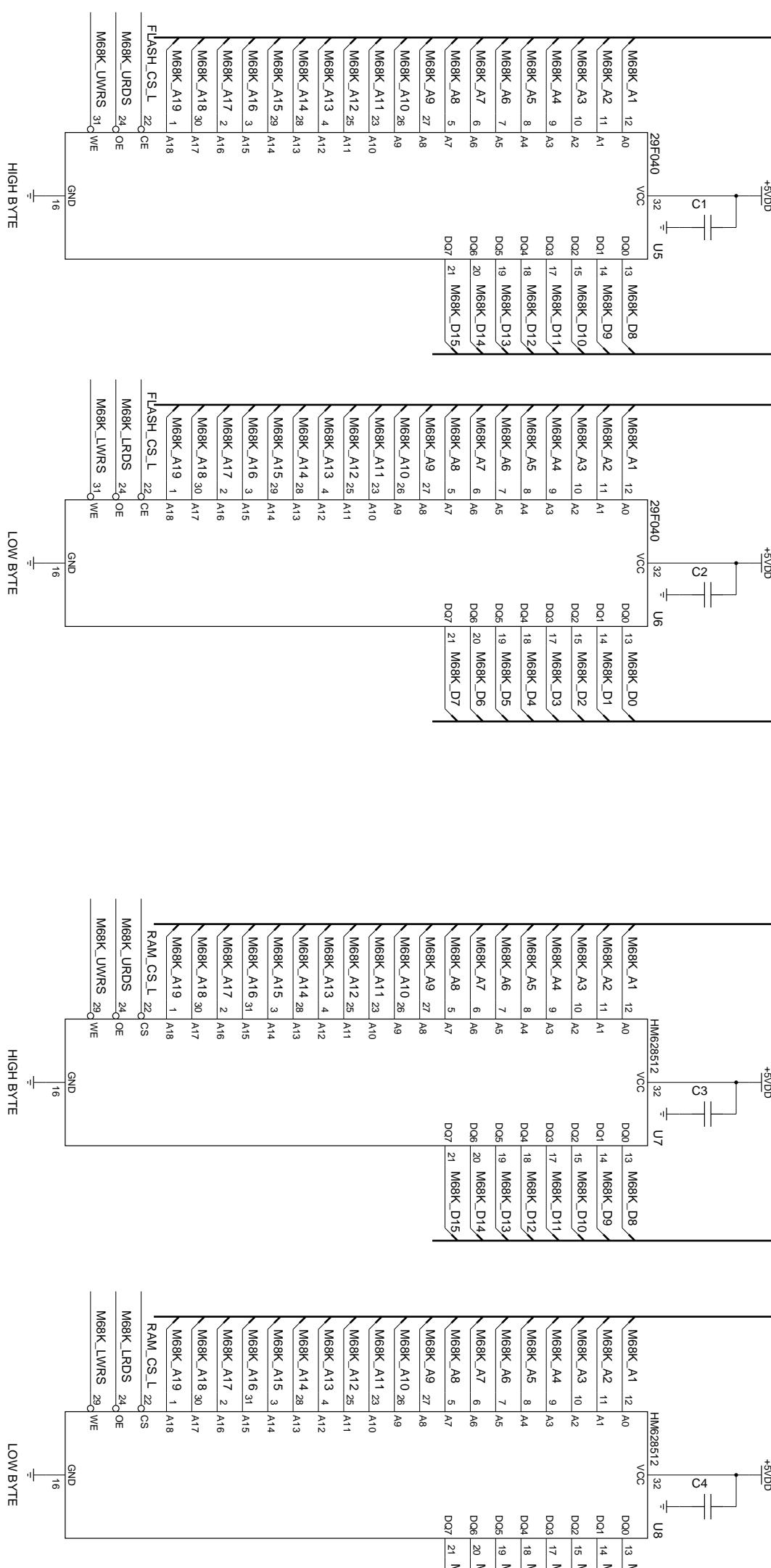


The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit	
TITLE	M68K bus
FILE: OSDCU_01.usch	REVISION: \$Revision: 1.10 \$
PAGE 1 OF 11	DRAWN BY: Michael Sokolov

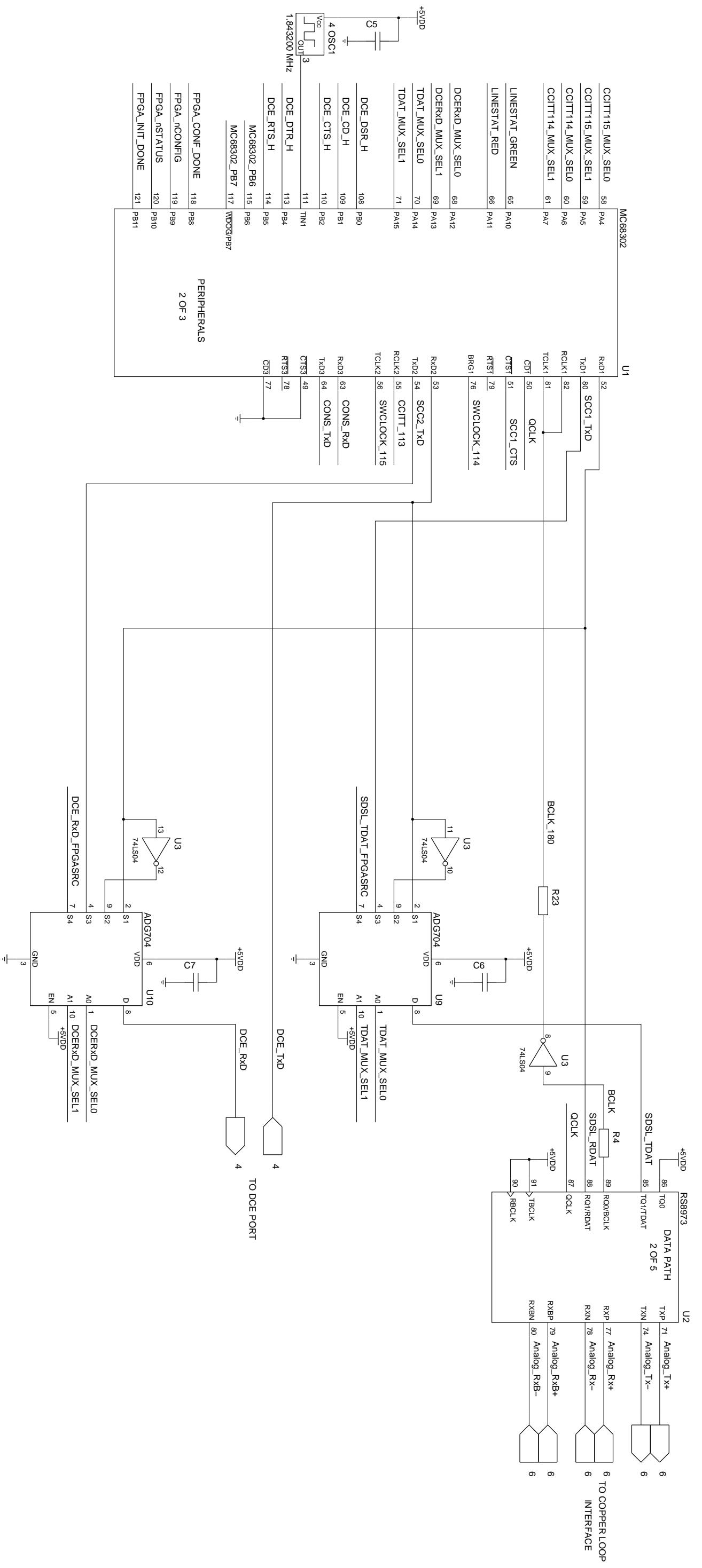
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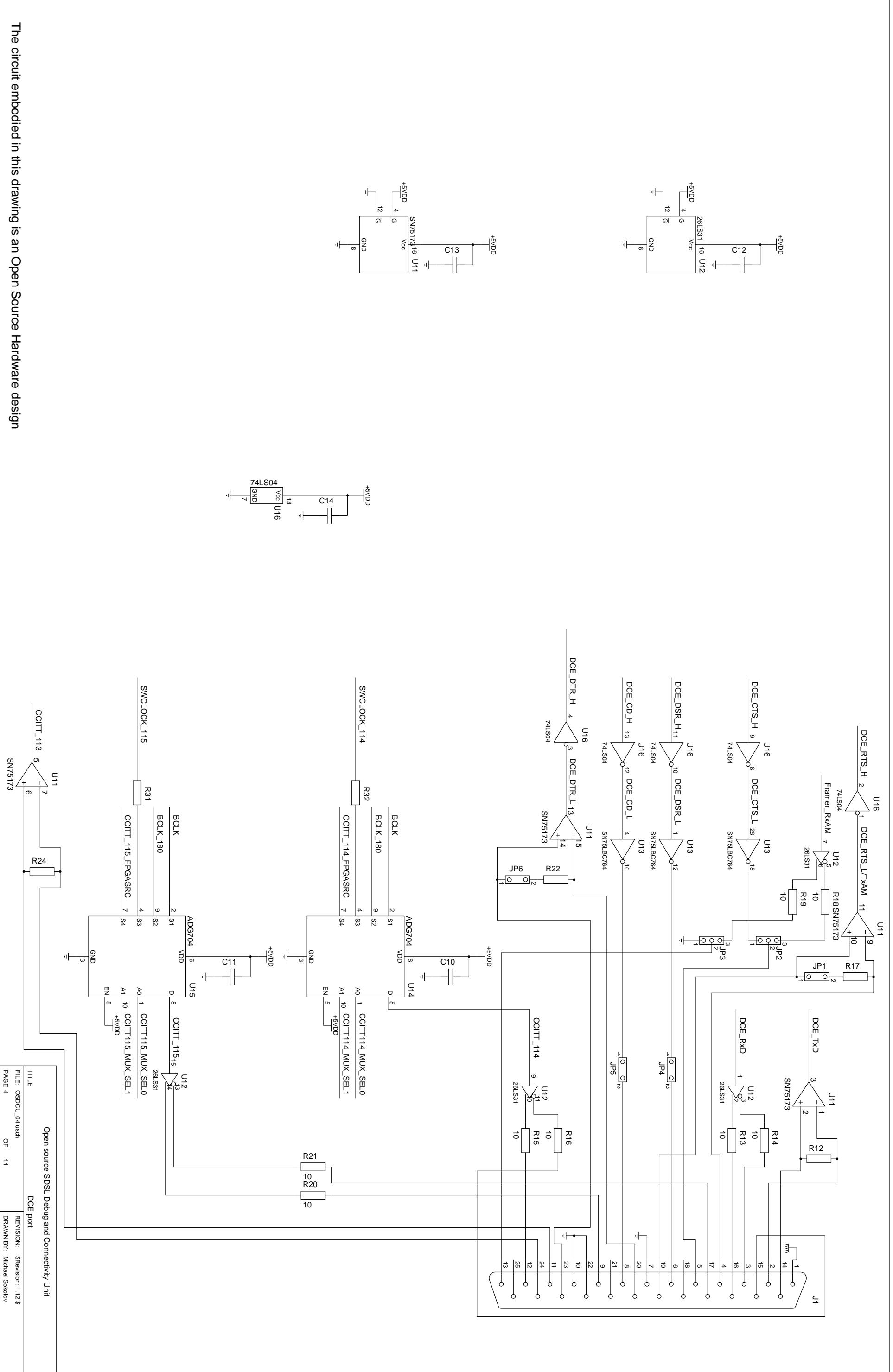
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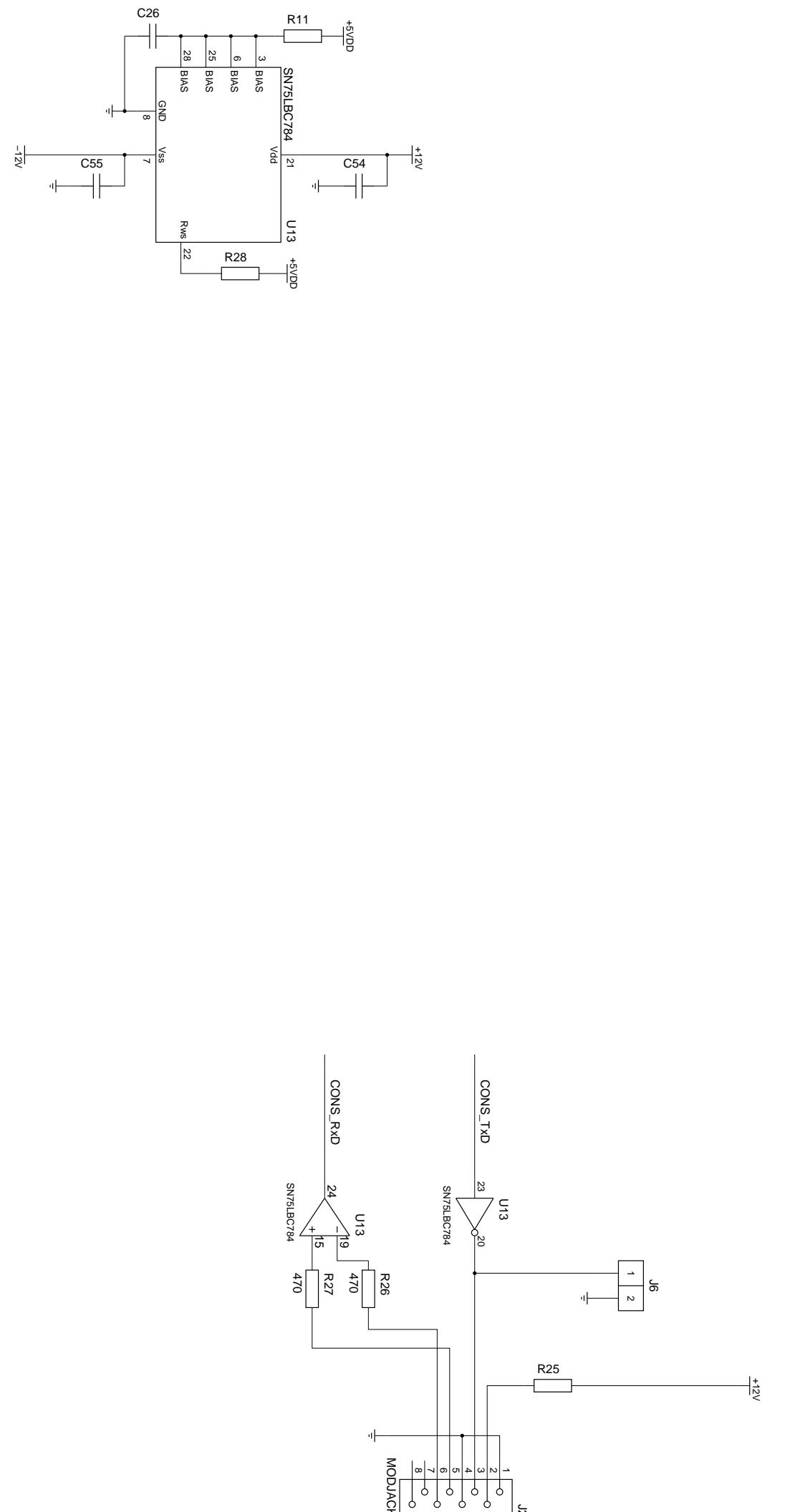


The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit	
TITLE	Flash & RAM
FILE: OSDCU_02.usch	REVISION: \$Revision: 1.3 \$
PAGE 2 OF 11	DRAWN BY: Michael Sokolov

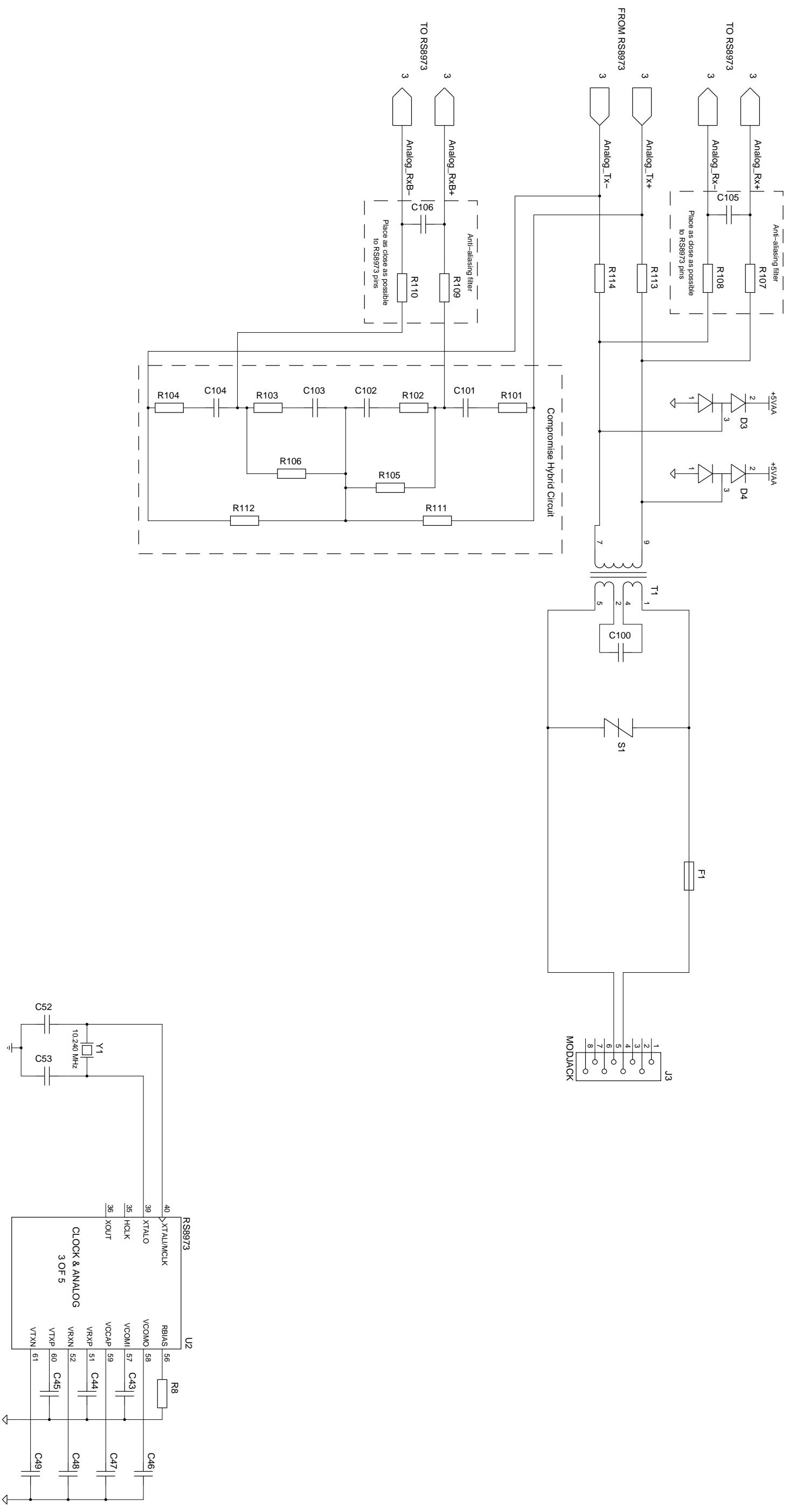






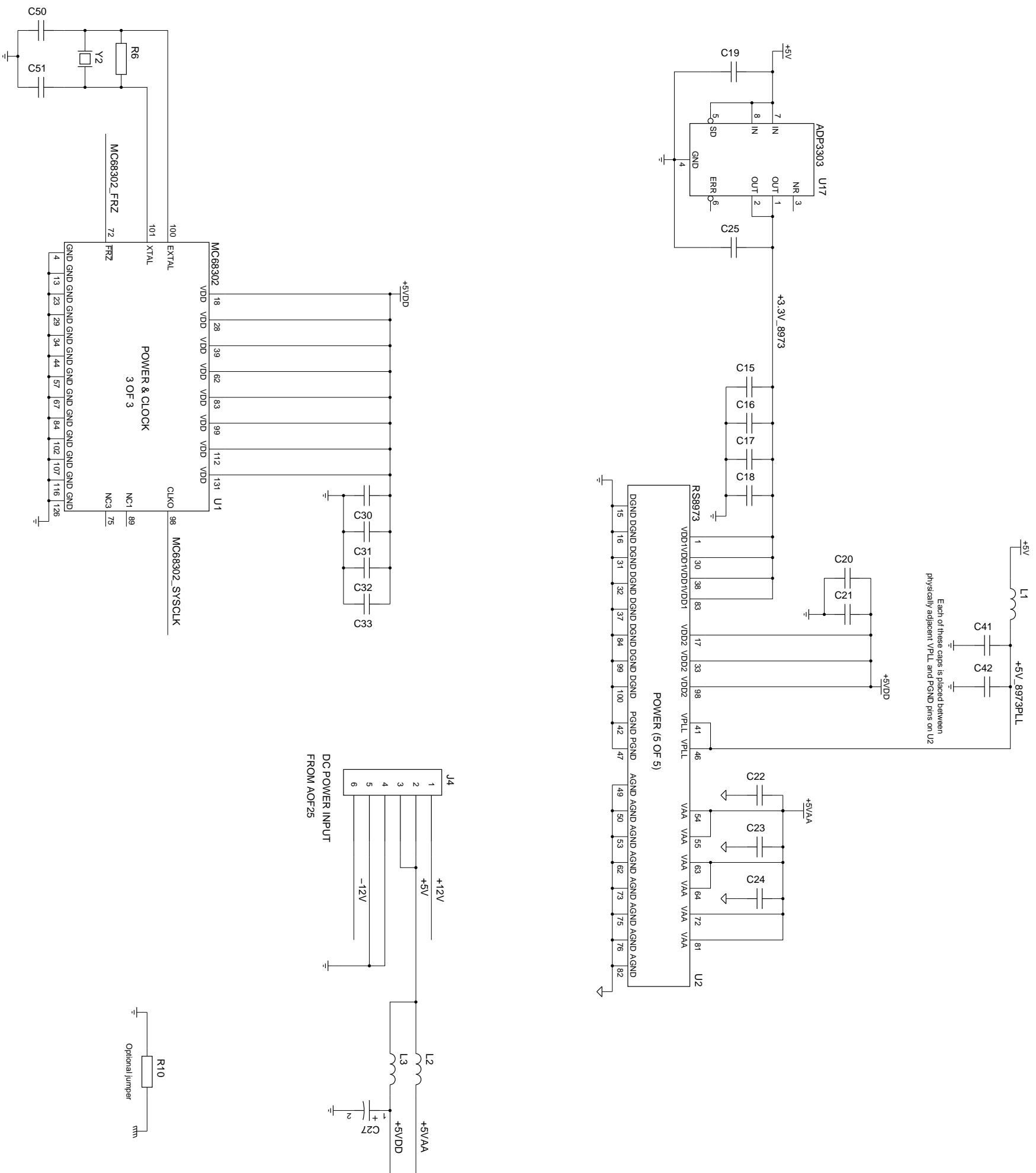
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit	
TITLE	Console port
FILE: OSDCU_05.sch	REVISION: \$Revision: 1.4 \$
PAGE 5 OF 11	DRAWN BY: Michael Sokolov



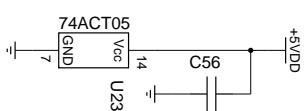
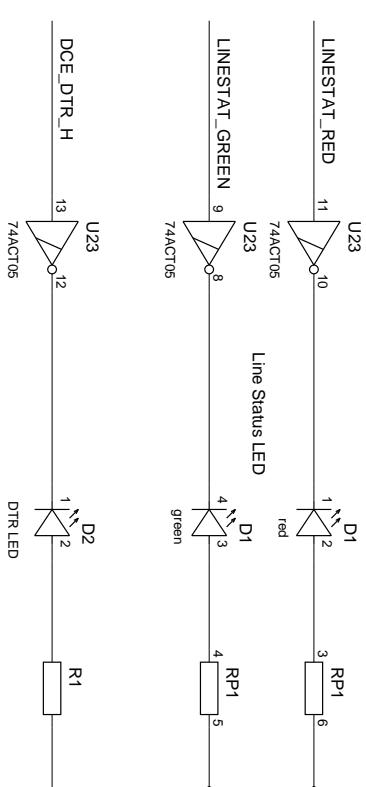
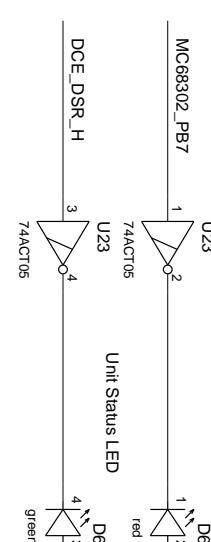
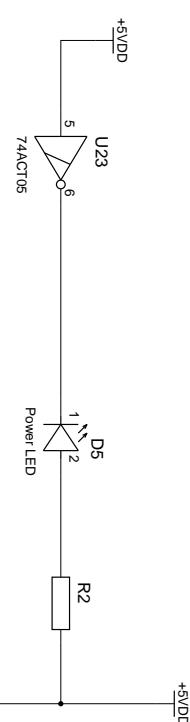
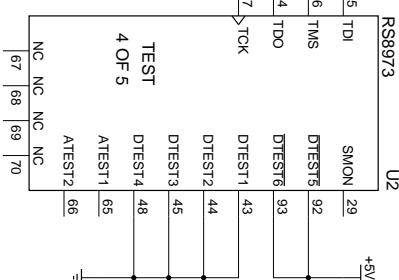
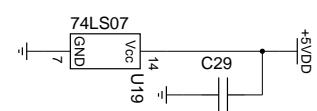
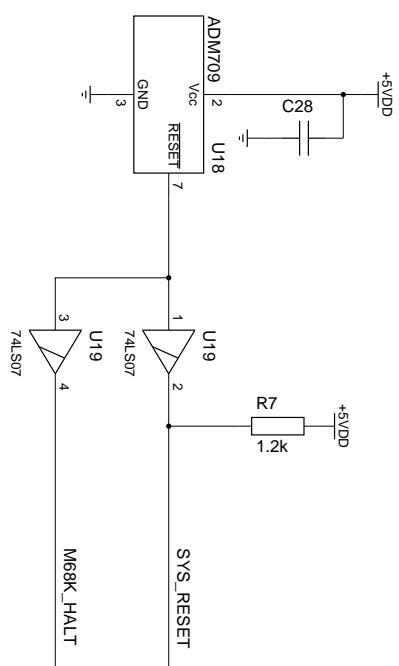
The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit	Copper loop interface
TITLE: OSDCU_06usdch	REVISION: \$Revision: 1.9 \$
PAGE 6 OF 11	DRAWN BY: Michael Sokolov



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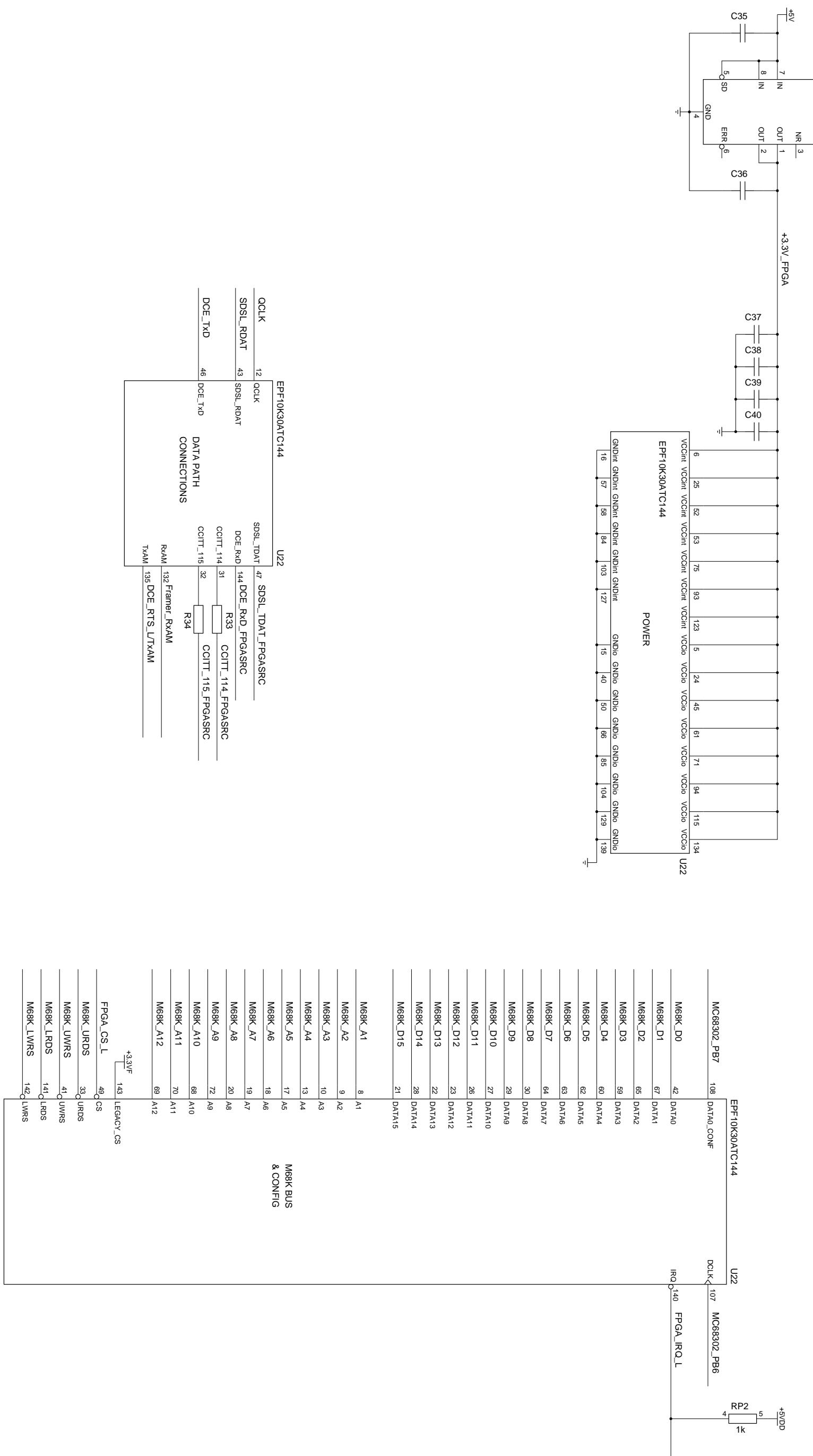
Open source SDSL Debug and Connectivity Unit	
TITLE	Power
FILE: OSDCU_07.usch	REVISION: \$Revision: 1.6 \$
PAGE 7 OF 11	DRAWN BY: Michael Sokolov



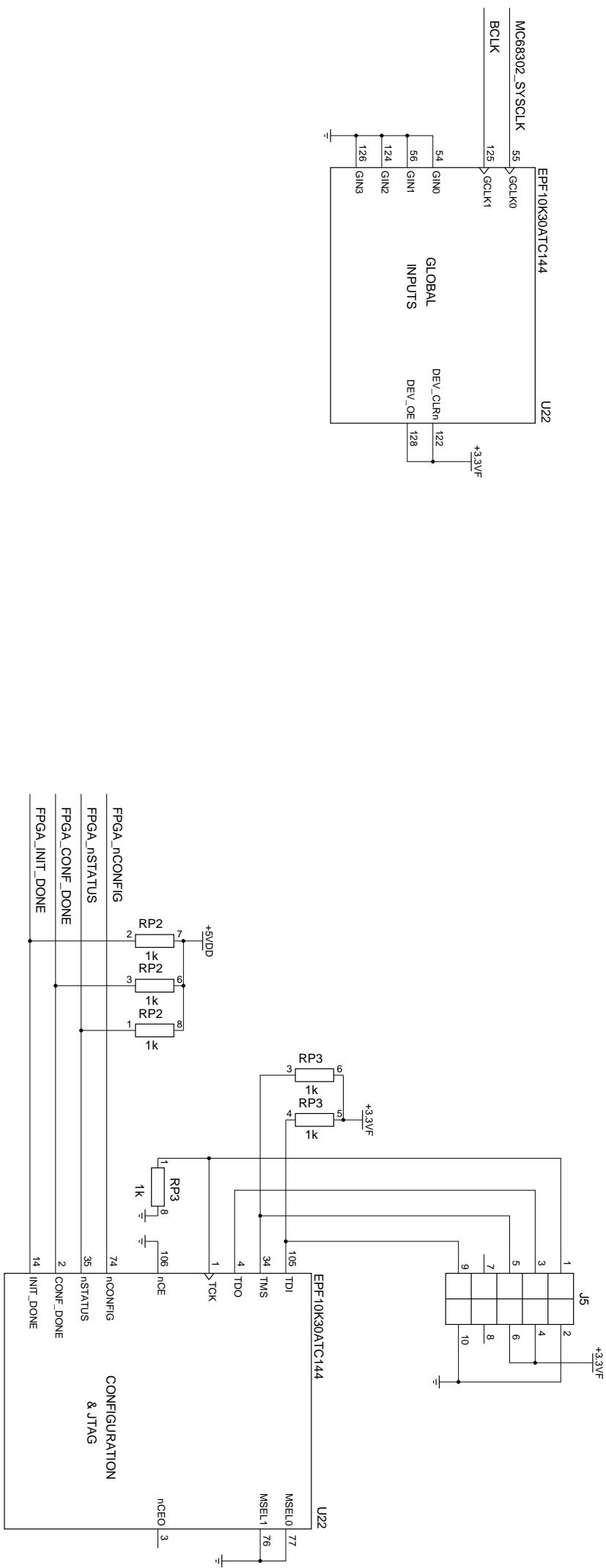
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Open source SDSL Debug and Connectivity Unit

Miscellaneous	
FILE: OSDCU_08.vsch	REVISION: \$Revision: 1.7 \$
PAGE 8 OF 11	DRAWN BY: Michael Sokolov

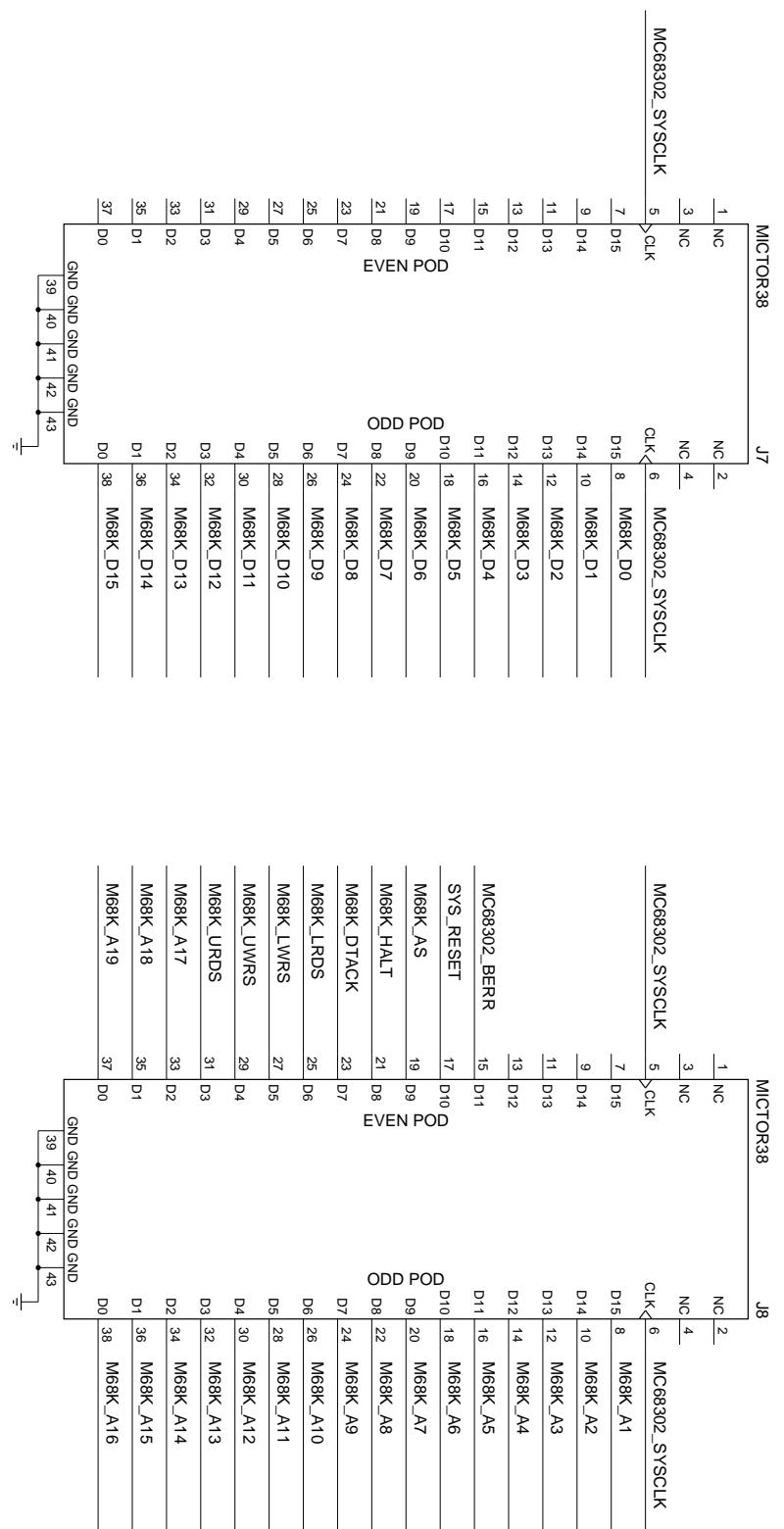


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The circuit embodied in this drawing is an Open Source Hardware design

Open source SDSL Debug and Connectivity Unit	
TITLE	FPGA (2 of 2)
FILE: OSDCU_10usvh	REVISION: \$Revision: 1.10 \$
PAGE 10 OF 11	DRAWN BY: Michael Sokolov



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Open source SDSL Debug and Connectivity Unit	
TITLE	Debug
FILE: OSDCU_11.usch	REVISION: \$Revision: 1.1 \$
PAGE 11 OF 11	DRAWN BY: Michael Sokolov