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Jameco Part Number 280049

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# HM628512A Series

4 M SRAM (512-kword  $\times$  8-bit)

# HITACHI

ADE-203-640B (Z)

Rev. 2.0

Nov. 1997

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## Description

The Hitachi HM628512A is a 4-Mbit static RAM organized 512-kword  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5  $\mu$ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512A is suitable for battery backup system.

## Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
  - Active: 50 mW/MHz (typ)
  - Standby: 10  $\mu$ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

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## HM628512A Series

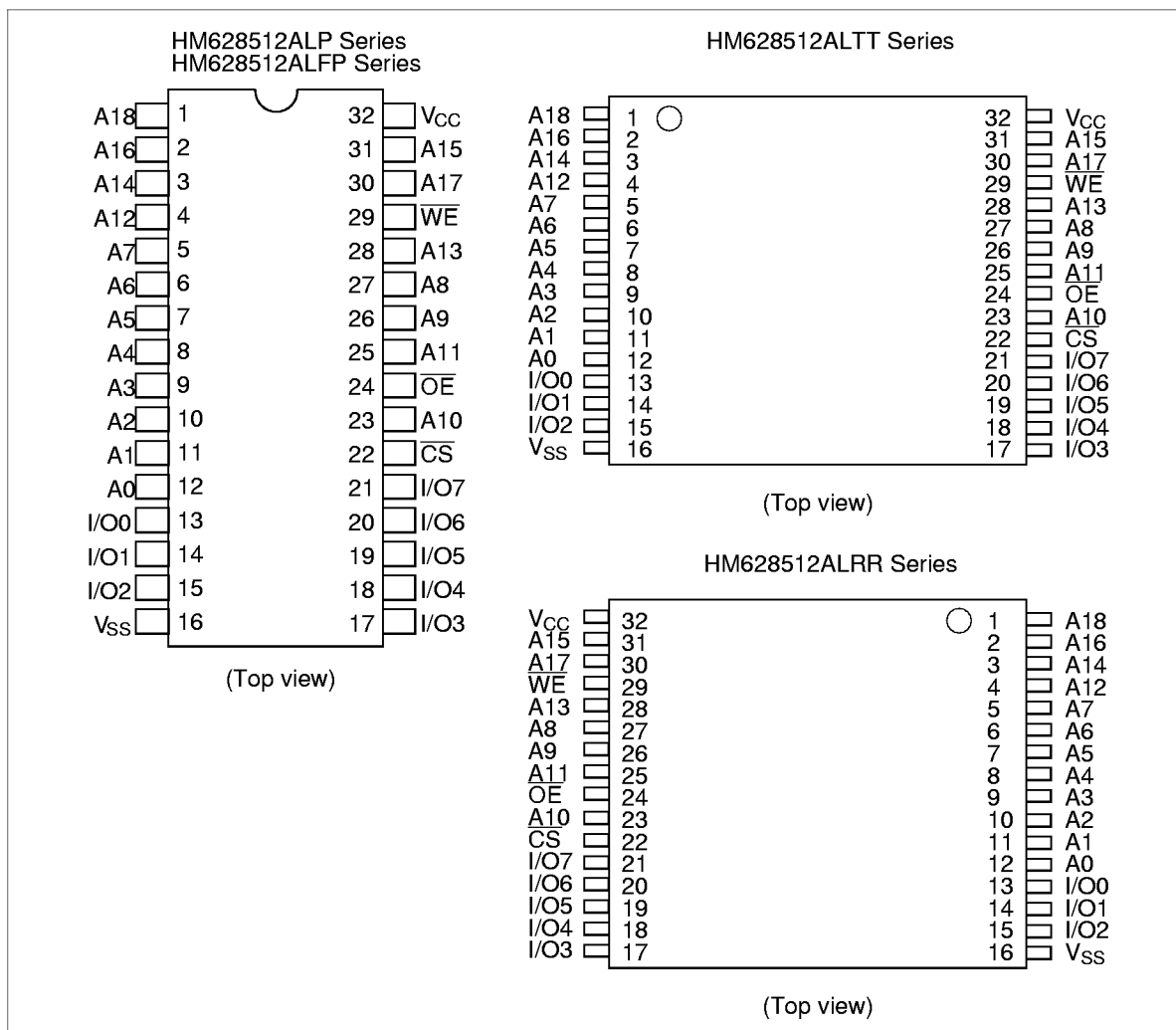
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### Ordering Information

Type No.	Access time	Package
HM628512ALP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512ALP-7	70 ns	
HM628512ALP-5SL	55 ns	
HM628512ALP-7SL	70 ns	
HM628512ALFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512ALFP-7	70 ns	
HM628512ALFP-5SL	55 ns	
HM628512ALFP-7SL	70 ns	
HM628512ALTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512ALTT-7	70 ns	
HM628512ALTT-5SL	55 ns	
HM628512ALTT-7SL	70 ns	
HM628512ALRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512ALRR-7	70 ns	
HM628512ALRR-5SL	55 ns	
HM628512ALRR-7SL	70 ns	

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## Pin Arrangement

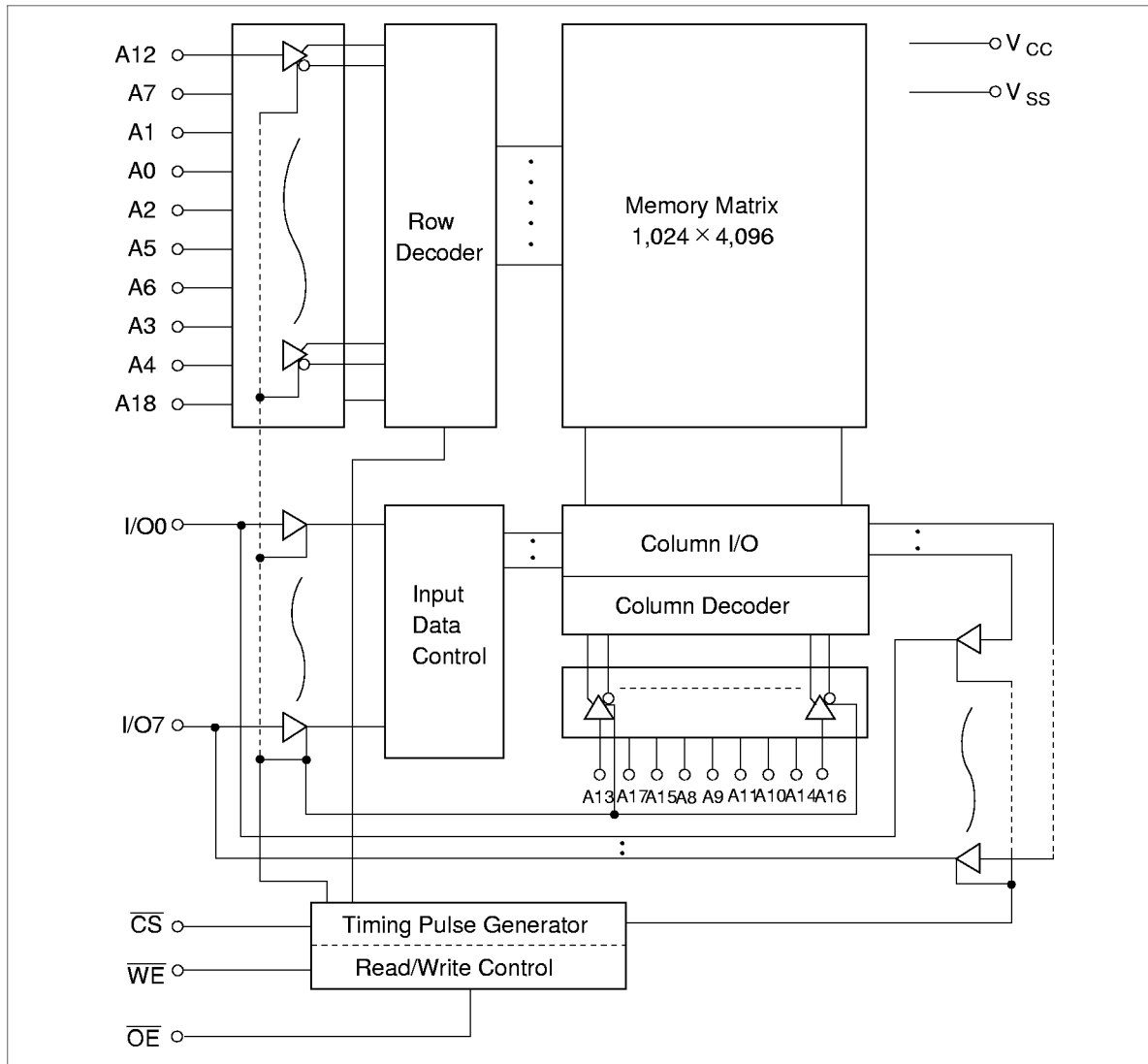


## Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

## HM628512A Series

### Block Diagram



**Function Table**

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
×	H	×	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: ×: H or L

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	−0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	−0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	−55 to +125	°C
Storage temperature under bias	$T_{bias}$	−10 to +85	°C

Notes: 1. −3.0 V for pulse half-width ≤ 30 ns

2. Maximum voltage is 7.0 V

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	−0.3* <sup>1</sup>	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

## HM628512A Series

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ±10% , V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current: DC	I <sub>CC</sub>	—	8	15	mA	$\overline{CS} = V_{IL}$ , others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA
Operating power supply current	HM628512A-5 I <sub>CC1</sub>	—	45	70	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$ , others = V <sub>IH</sub> /V <sub>IL</sub> I <sub>I/O</sub> = 0 mA
	HM628512A-7 I <sub>CC1</sub>	—	40	60	mA	
Operating power supply current	I <sub>CC2</sub>	—	10	20	mA	Cycle time = 1 μs, duty = 100% I <sub>I/O</sub> = 0 mA, $\overline{CS} \leq 0.2$ V V <sub>IH</sub> ≥ V <sub>CC</sub> − 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby power supply current: DC	I <sub>SB</sub>	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I <sub>SB1</sub>	—	2* <sup>2</sup>	100* <sup>2</sup>	μA	V <sub>in</sub> ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2* <sup>3</sup>	50* <sup>3</sup>	μA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = −1.0 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance* <sup>1</sup>	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

Note: 1. This parameter is sampled and not 100% tested.

## HM628512A Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (100 pF) (HM628512A-7)  
1 TTL Gate +  $C_L$  (50 pF) (HM628512A-5)  
(Including scope & jig)

### Read Cycle

		HM628512A					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	55	—	70	—	ns	
Address access time	t <sub>AA</sub>	—	55	—	70	ns	
Chip select access time	t <sub>CO</sub>	—	55	—	70	ns	
Output enable to output valid	t <sub>OE</sub>	—	25	—	35	ns	
Chip selection to output in low-Z	t <sub>LZ</sub>	10	—	10	—	ns	2
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2
Chip deselection to output in high-Z	t <sub>HZ</sub>	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	



## HM628512A Series

### Write Cycle

		HM628512A					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	55	—	70	—	ns	
Chip selection to end of write	t <sub>CW</sub>	50	—	60	—	ns	4
Address setup time	t <sub>AS</sub>	0	—	0	—	ns	5
Address valid to end of write	t <sub>AW</sub>	50	—	60	—	ns	
Write pulse width	t <sub>WP</sub>	40	—	50	—	ns	3, 12
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t <sub>WHZ</sub>	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t <sub>DW</sub>	25	—	30	—	ns	
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns	
Output active from output in high-Z	t <sub>OW</sub>	5	—	5	—	ns	2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2, 7

Notes: 1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

4.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.

5.  $t_{AS}$  is measured from the address valid to the beginning of write.

6.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

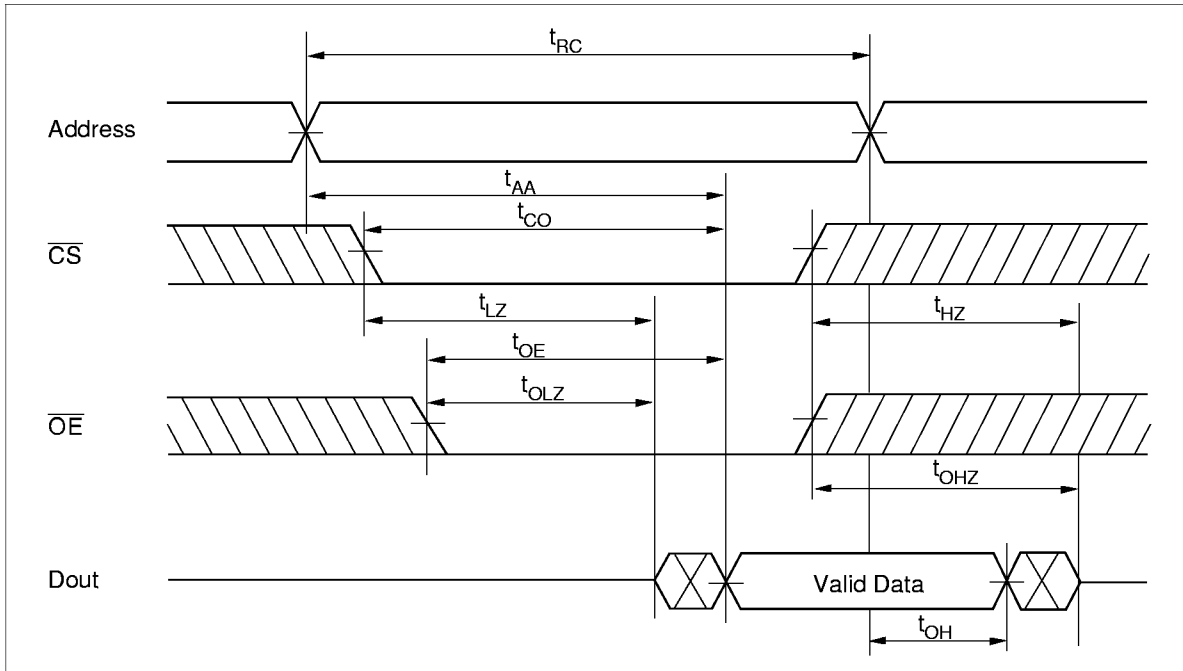
10. Dout is the read data of next address.

11. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

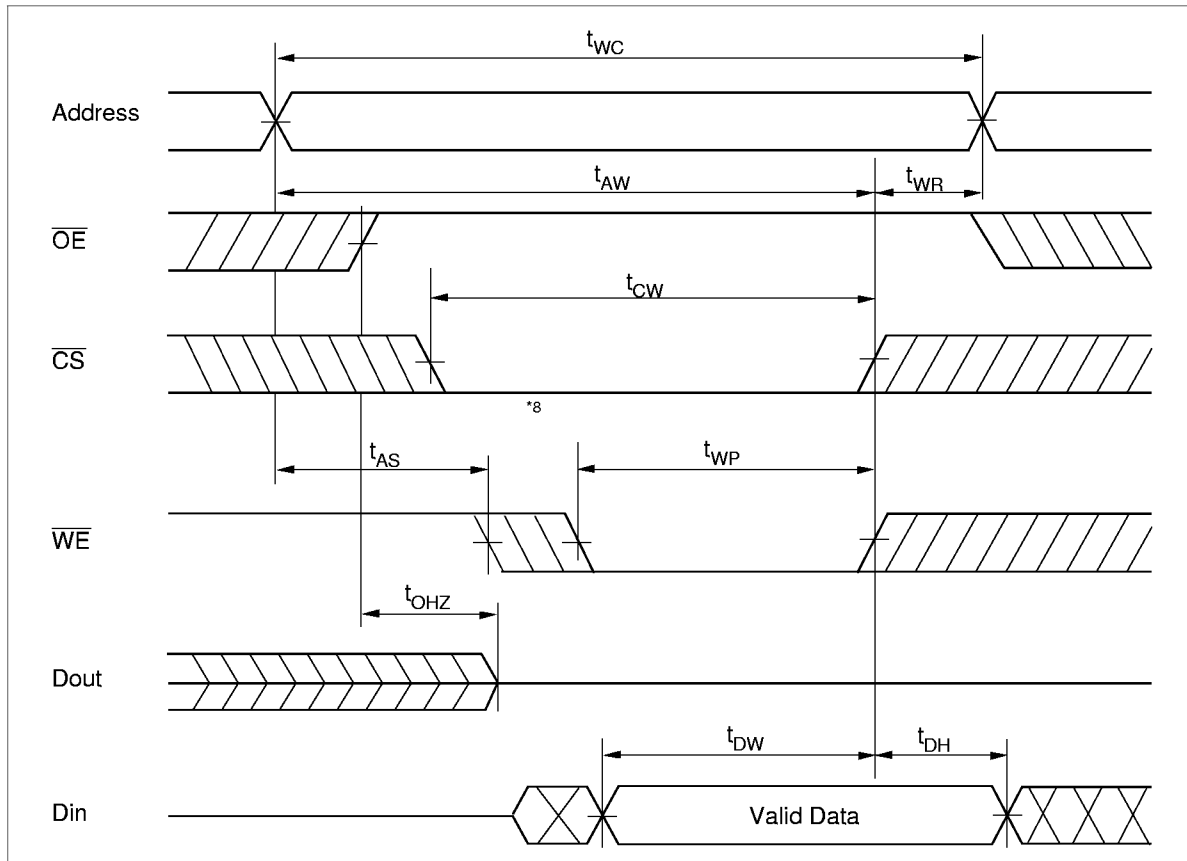
## Timing Waveforms

### Read Timing Waveform ( $\overline{WE} = V_{IH}$ )

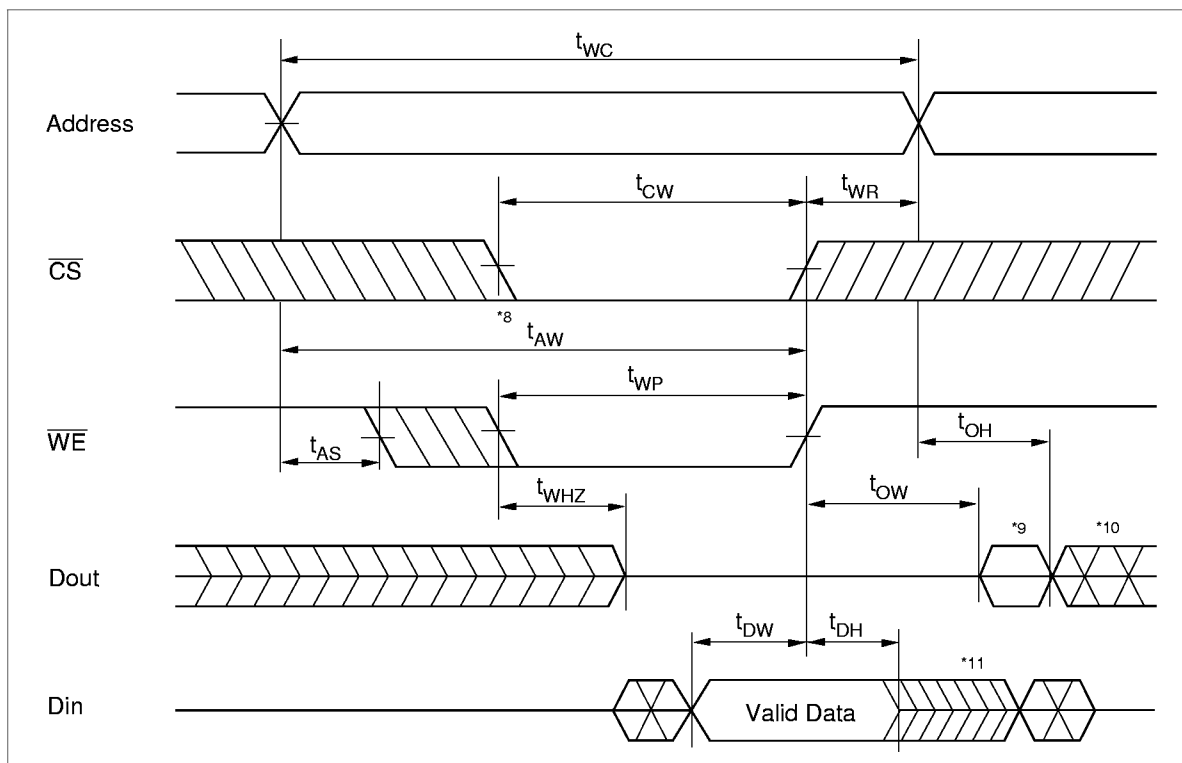


## HM628512A Series

### Write Timing Waveform (1) ( $\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) ( $\overline{\text{OE}}$  Low Fixed)



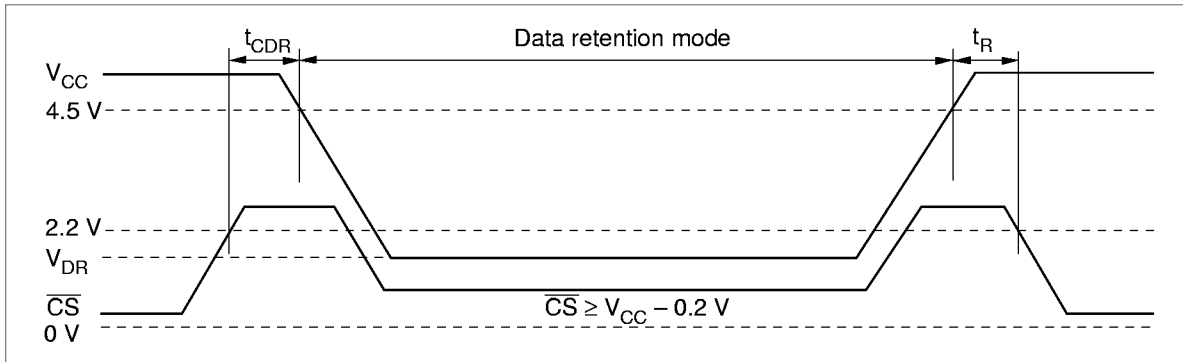
## HM628512A Series

### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions* <sup>3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq 0 \text{ V}$
Data retention current	$I_{CCDR}$	—	1* <sup>4</sup>	50* <sup>1</sup>	$\mu\text{A}$	$V_{CC} = 3.0 \text{ V}$ , $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
		—	1* <sup>4</sup>	15* <sup>2</sup>	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

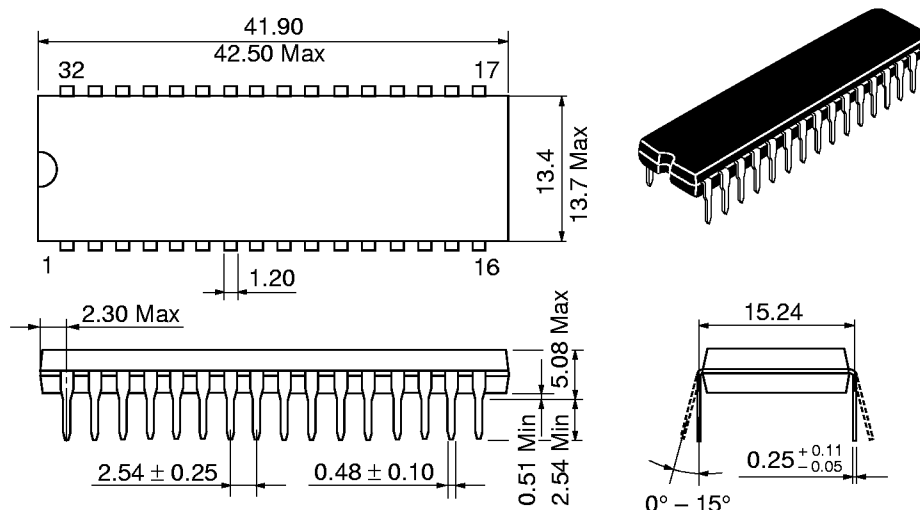
- Notes: 1. For L-version and 20  $\mu\text{A}$  (max.) at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 2. For SL-version and 3  $\mu\text{A}$  (max.) at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 3.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.  
 4. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = 25^\circ\text{C}$  and specified loading, and not guaranteed.

### Low $V_{CC}$ Data Retention Timing Waveform ( $\overline{CS}$ Controlled)



**Package Dimensions**
**HM628512ALP Series (DP-32)**

Unit: mm



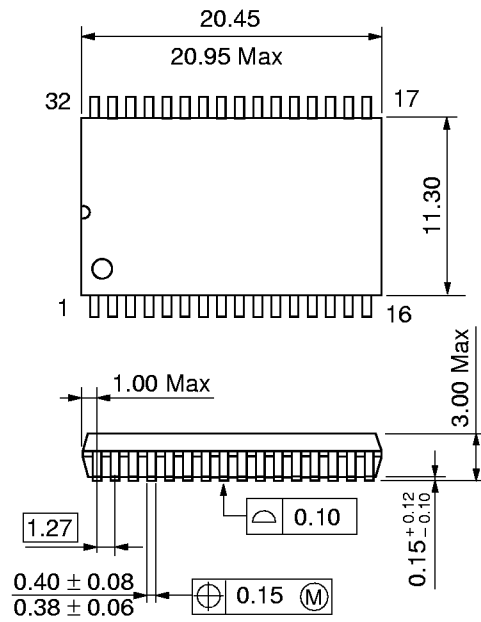
Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

## HM628512A Series

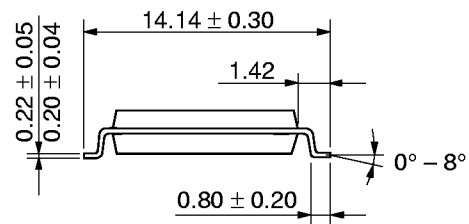
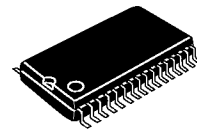
### Package Dimensions (cont.)

#### HM628512ALFP Series (FP-32D)

Unit: mm



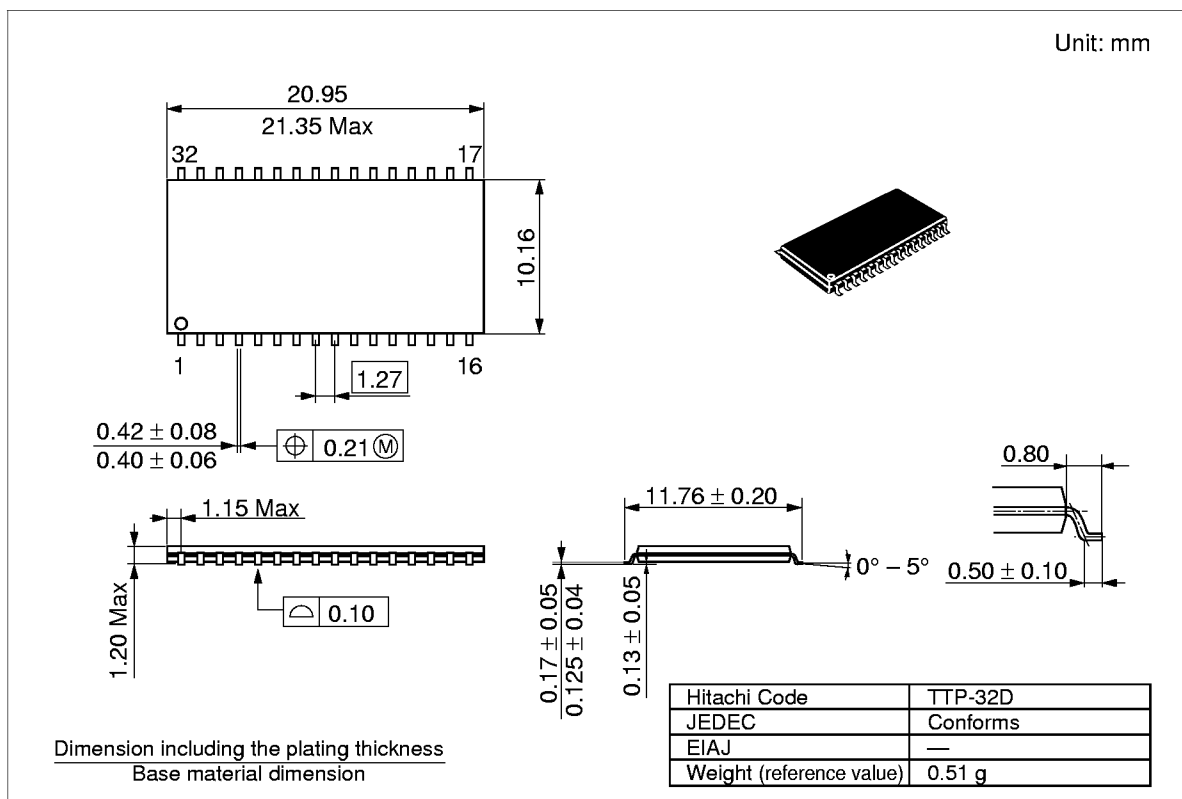
Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

## Package Dimensions (cont.)

### HM628512ALTT Series (TTP-32D)

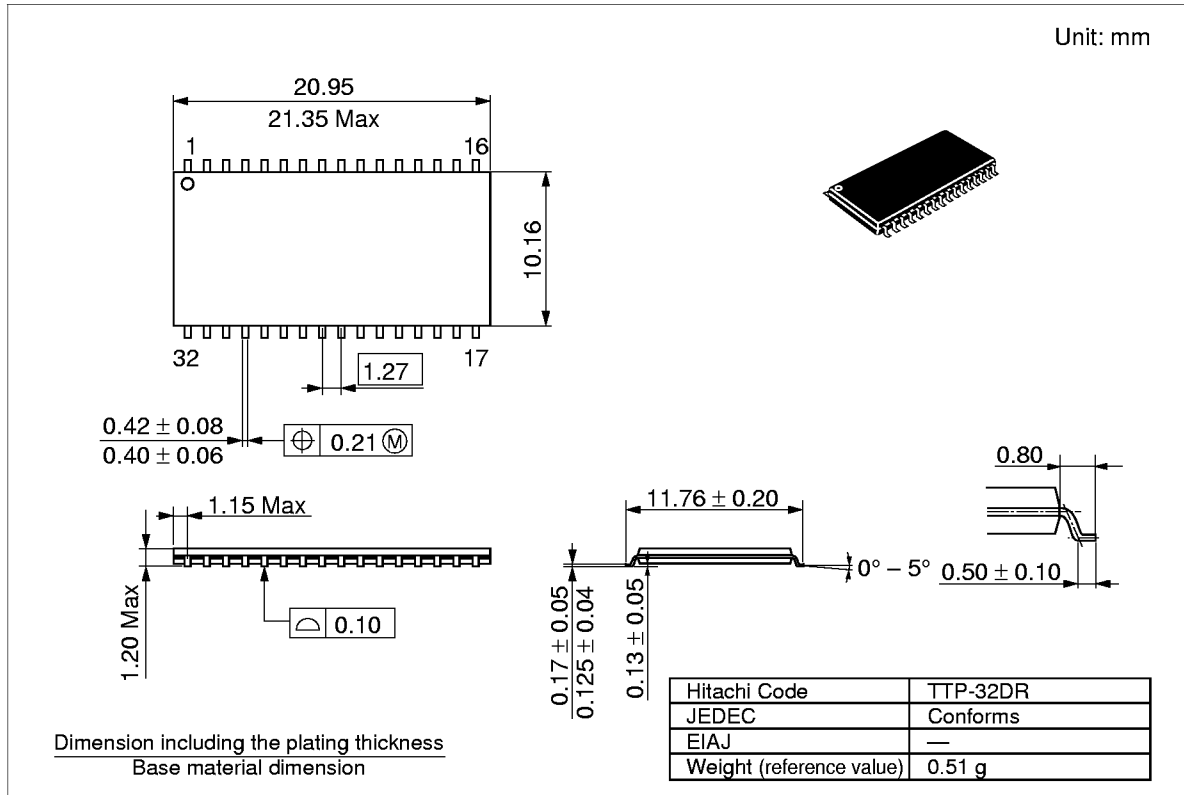




## HM628512A Series

### Package Dimensions (cont.)

#### HM628512ALRR Series (TTP-32DR)



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## HM628512A Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 12, 1996	Initial issue	K. Imato	K. Imato
1.0	Dec. 2, 1996	Deletion of preliminary	K. Imato	K. Imato
2.0	Nov. 1997	Change of Subtitle		