M289XX Layout Guidelines

Application Note

289xx-APP-002-A
Sept. 2003

MINDSPEED™

Revision History

Revision	Level	Date	Description
A	Preliminary	September 2003	Initial release.

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1.0 General PCB Design and Layout Considerations

1.1 Introduction

This document discusses general design and board layout techniques to ensure maximum performance and reliability while limiting undesired emissions (EMI) and susceptibility. The ideas contained in this document are a compilation of recommendations from many experts in the field of EMC. The theory behind some of the concepts is beyond the scope of this paper. Since there are many conflicting methods and practices between experts, Mindspeed has tried to include concepts that have worked for this company, as well as methods mutually agreed upon between experts. The effectiveness of these concepts may be dependent on the particular PCB application. This application note provides guidelines for laying out a PCB and is not intended to take the place of a professional EMI consultant.

1.2 PCB Layout Considerations

1.2.1 Component Placement

Connectors:

- Place connectors first. When using a metal enclosure, mount all of the connectors on the same edge of the PCB.
- Place IO drivers close to the connectors they are supporting.
- Make connector pin assignments after layout is considered. This aids in minimizing current loops.
- Place bulk decoupling and parallel 1 µF capacitors near connectors passing power for each voltage passed.
- Do not place high frequency or critical signals near or between connectors unless they are going through the connectors.

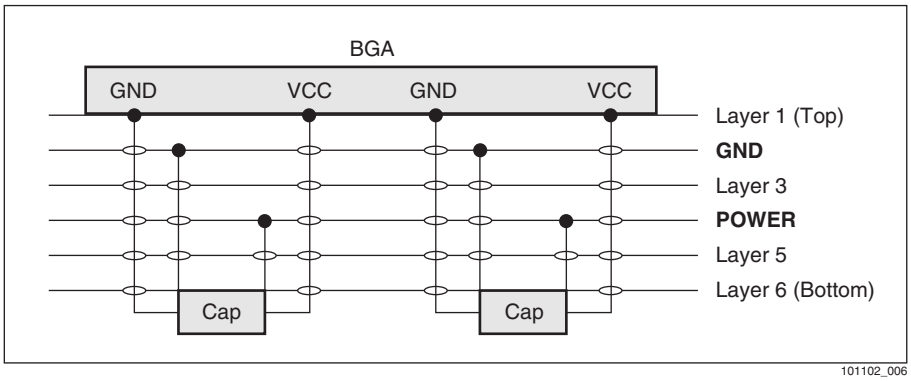
Components:

- Segregate components by voltage requirements when possible. This aids in clean power plane layout.
- Straddle the power plane boundaries when using multi-voltage ICs.
- Place analog components (AFE, hybrid, surge, and line interface) to isolate

them from digital currents.

- Place large components toward the middle of the board, but most importantly, keep them away from external edges of the board.
- Place clock drivers and components supplying critical signals near the ICs they are supplying to minimize critical signal line lengths.
- Place bulk decoupling (based on formula below) and parallel 1 µF capacitors near all DC/DC converters, voltage regulators, and large ICs.
- Repeat bulk decoupling and parallel 1 µF capacitors near large ICs and for every 25 square inches of board space.
- Mount decoupling capacitors as close to the component they are supporting as possible. They must also be on the component side of the board to be most effective.
- For BGA's, mounting the decoupling capacitors on the same side of the board as the component is not always possible if the power and ground are not on the outside row of balls. It may be necessary to drop down to the bottom of the board and route the power and ground signals to capacitors mounted on the bottom. In any case, the power and ground should be routed to the capacitors before going to the power and ground planes (illustrated in Figure 1-1.)
- Tie floating metal, like heat sinks and crystal cases, to the reference plane.

Figure 1-1. Decoupling BGAs



1.3 Routing Traces

1.3.1 Decoupling Capacitors

- Decoupling capacitors (0.001 – 0.1 µF) should be placed as close to the power and return (GND) pins they are supporting as possible. It is better to route power and return (GND) through the capacitor and make the connection to the power and return plane with a via through the capacitor pad. Try to keep return loops, thus series inductance, as small as possible. Thick traces are better (Figure 1-2).

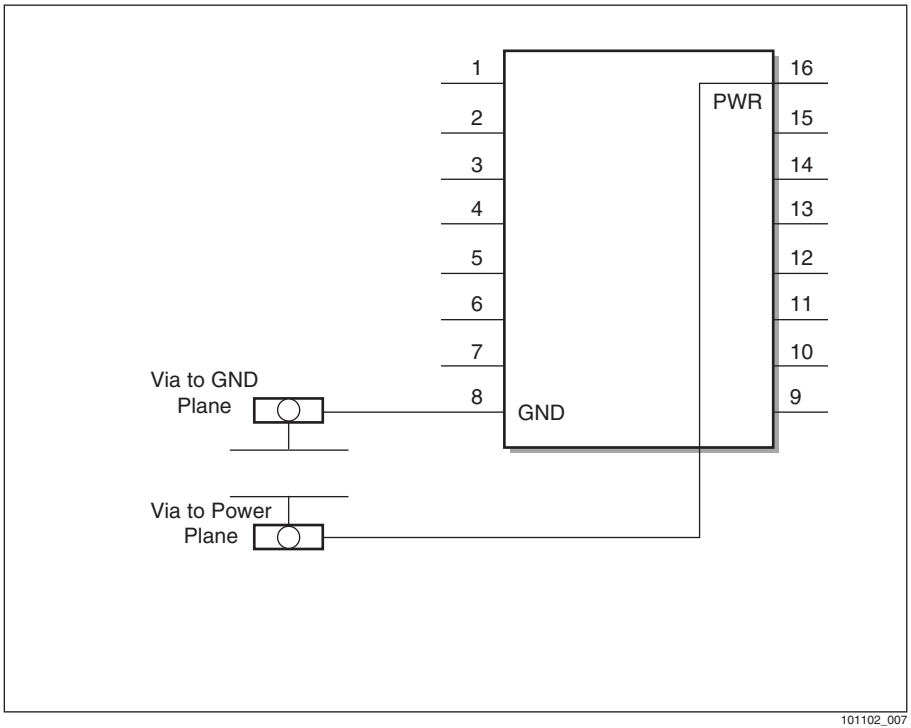
NOTE: Trace lengths, illustrated in Figure 1-2, are exaggerated for clarity.

- BGAs – see Figure 1-1

1.3.2 Signals Entering or Leaving Board Through Connectors

- Use the lowest impedance possible when passing through a connector.
- Buffer all clock, address and control signals passing through connectors with a non-latching part. Buffers must be able to sink 16 mA (e.g., 74244). Static TTL level signals may have their impedance lowered by using ≤2.7 KΩ pull-ups.

Figure 1-2. Decoupling—Mount capacitor



1.3.3 Clocks and Other Critical Signal Traces

- High speed data and clock lines should have a 33 - 50 Ω series resistor at the source and long traces should have a parallel shunt capacitor at the terminating end. A series resistor is preferred over a shunt capacitor because it decreases the current on the signal line and on the DC power bus. A shunt capacitor increases the current. You can always insert a zero ohm or no load the capacitor if signal integrity is adversely affected.
- Use low impedance return paths. The signals and return path should be <0.1 inch apart for critical signal traces and less for extremely critical traces.
- Keep critical traces as short and direct as possible. Keep current loop areas small. Keep clocks and critical traces away from other circuitry, especially analog signals.
- Use wide traces whenever possible. Wide traces have less inductance.
- Do not allow critical signal and clock traces to cross separations in power or ground planes. This could cause cross talk or ringing.
- If possible, bury clock traces between power and ground planes. The clock should route from the driver pin under the chip and down to an inner layer. Very short (<0.1 inch) surface traces should be used to connect to terminating components. The destination end should rise to the surface under the chip.
- Clocks greater than 50 MHz should be routed on an inner layer and controlled impedance should be used.
- Buffer all clock signals passing through connectors with non-latching components.
- Do not route high frequency traces parallel to the major axis of connectors. If this cannot be avoided, keep the trace at least 1” away from the connector, or add a 0.050 inch wide return trace between the connector and the high frequency trace.
- Keep all traces away from the board edges.

1.3.4 Hybrid and Line Interface

- Route line driver/hybrid differential traces in a symmetrical fashion. Traces should be a consistent width, length, and have consistent separation of ≤ one trace width when possible.
- Wider traces have less inductance therefore lower impedance.
- Keep all analog traces clear of digital and clock traces and away from digital and clock current paths.

1.4 DC Power Bus and Return/Reference Planes

1.4.1 Power Bus

- Power plane can be split on one plane to accommodate the different voltage requirements of ICs. However, the gaps between them should be several mm wide to reduce capacitive coupling and provide isolation at high frequencies.
- All power supplies entering through a connector or originating on the board should have a bulk decoupling capacitance (see Section 1.8 for the appropriate capacitor value) and a parallel 1 µF capacitor. Repeat bulk and 1 µF near large integrated circuits (ICs) and for every 25 square inches of board space.
- All ICs should have 0.001 – 0.1 µF capacitor between each power and ground pin pair. ICs with multiple power and ground pins should have a minimum of one capacitor per quadrant. Each separate voltage (i.e. +5 VAA, +3.3, and +5 VDD) requires separate decoupling. Decoupling of all power and return pin pairs is preferred.

1.4.2 Return/Reference Plane

- There should be at least one layer of solid reference (GND) plane.
- The top and bottom layers of the board should be flooded wherever possible, however care should be taken not to short the routing of the decoupling capacitors to the return pins of the ICs. Do not allow any electrically floating metal; connect edges of copper fill to reference plane below. This will help to reduce electric field noise coupling and improve magnetic and electric field containment.
- A minimum 1/8 inch band of copper shall be routed around the perimeter of the circuit board on the top and the bottom plane. A via should be placed about every ½ inch in the center of the trace connecting the top and bottom, to all reference layers in between.
- Do not allow power planes to overlap. Noise may be capacitively coupled from one power bus to another.

1.5 Signal Integrity

There can be a trade-off between having the ideal signal for EMC and having the ideal signal for optimal performance. A signal with excessive capacitance has a rounded transition edge thus reducing the high frequency harmonics associated with EMI. However, too much rounding of the transition edge may adversely effect the integrity of the signal and the performance of the circuit.

When measuring signals in a circuit, it may be necessary to use a FET probe to reduce the effect of the capacitance and inductance of the scope probe on the circuit.

Ringing may indicate excessive trace inductance or an under-dampened resonance condition

Rounding may indicate excessive capacitance on the signal.

Sharp transitions may indicate reflections due to impedance mismatches.

- Use self-shielding for critical traces whenever possible.
- Traces on adjacent layers should be perpendicular to reduce cross talk.
- Connect guard traces to the return plane at both ends. This will provide an additional return path.
- Connect all metal fill areas on all board layers to the return plane to reduce capacitive noise coupling.
- Connect all unused gate inputs to the reference plane or through a 1 KΩ resistor to +VDO to prevent noise transient switching.

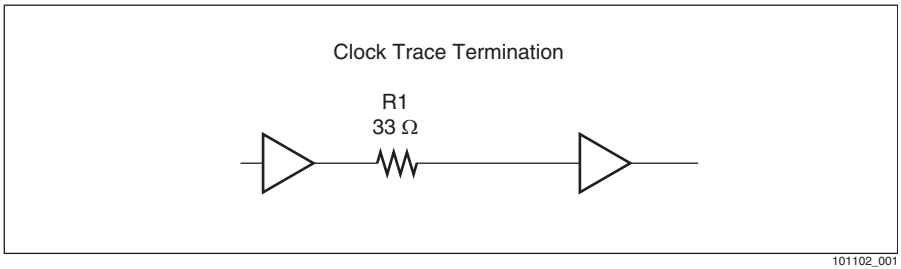
1.6 High Frequency Transmission Lines

The following guidelines do not take board capacitance or trace impedance into consideration. Placeholders for the components should be added to the board and the values can be adjusted for optimal signal performance when the layout is complete.

A signal trace should be treated as a high frequency transmission line when the trace length is > l/20 λ, or the propagation delay > (pulse rise time)/4.

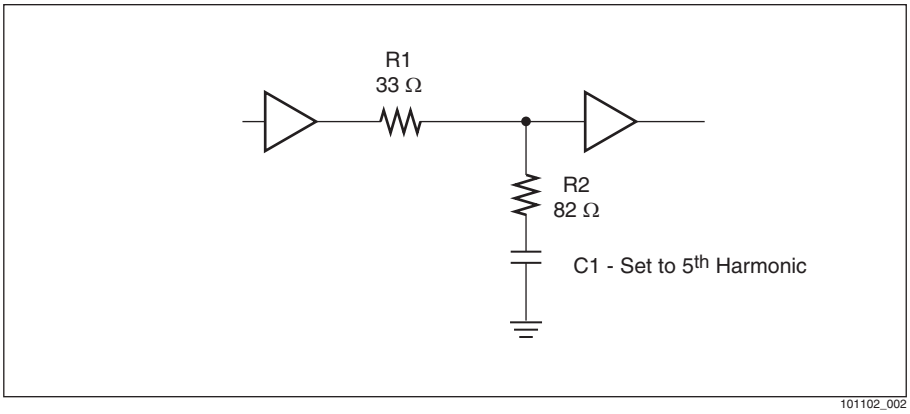
- Clock traces expected to be longer than 0.75” and over 100 MHz should have a 33 Ω series-terminating resistor close to the driver (Illustrated in Figure 1-3.)

Figure 1-3. Series Clock Termination



- Clock traces expected to be over 1” and greater than 1 MHz should have a 33 Ω series terminating resistor near the clock source and RC termination at the end of the trace. For RC termination use an 82 Ω resistor in series with a capacitor calculated for an impedance equal to 82 Ω at the 5th harmonic of the clock frequency (Illustrated in Figure 1-4.)

Figure 1-4. Series/RC (Parallel) Termination



- Example: For a 27 MHz clock: $1/(82 \times 2 \times PI \times 5 \times 27{,}000{,}000) = 14.3$ pf.

  NOTE: If the calculated capacitor is < 8.2 pf, use a lower value resistor for R2 and calculate the capacitive impedance to be equal to that lower value.

- When driving multiple loads, connect a 33 Ω series resistor at the source, and add a RC termination at the last device. Avoid "T" traces.
- Figure 1-5 illustrates improper termination. There is no series or RC termination and there are "T" traces.
- Figure 1-6 illustrates proper termination. Since source and destination are properly terminated, all of the components between them also have the proper termination.

Figure 1-5. Improper Termination

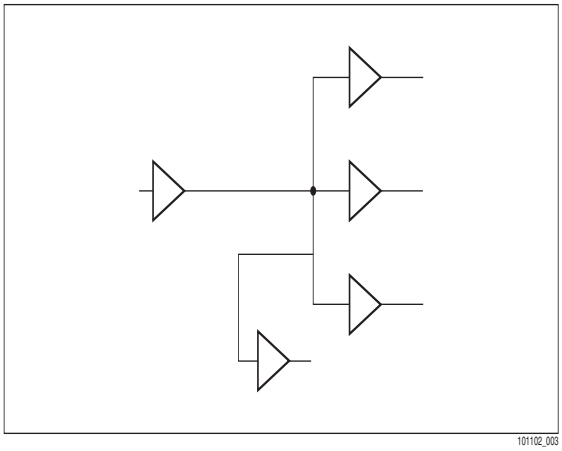
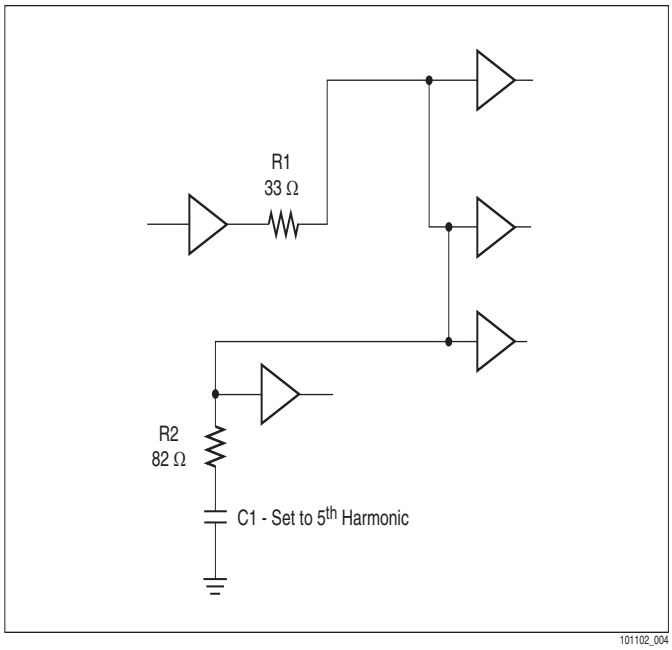


Figure 1-6. Proper Termination



1.7 Reducing Conducted and Radiated Emissions

- Do not split or gap the return plane under or between connectors.
- Use the longest rise time possible for all pulse signals. Most signals have faster rise times then required.
- Slow down the clock if possible. Use a series resistor to lengthen the rise time.
- Use the slowest logic families possible
- Minimize high-speed signal loop areas.

1.7.1 Metal Enclosures

- Metallically or capacitively connect all external metal structures together so they are at the same RF voltage.
- Bond or capacitively connect all wires leaving the enclosure to the enclosure, or use shielded cable connected to the enclosure.
- Bond or capacitively couple circuit board return to the metal chassis at the connector to reduce Common Mode Voltage on the cable leaving the enclosure. This connection reduces the mutual inductance between the inside and outside loop by forming a common boundary.
- Use a common mode choke or center tap transformer on differential mode signals to reduce conducted common mode noise.

1.8 Determining Bulk Capacitance

The power supply charges the bulk capacitor and the capacitor powers the components, therefore, a bulk capacitor is required to maintain enough charge to power the chips it is supporting. The capacitor value selected for this task should be adequate to hold enough energy for at least two power supply cycles. The minimum value should be 4.7 µF. To determine this value, we use the following formula: $C = W_c \times 2/V2$

$W_c = I \times V \times 2/F$

F = Switching frequency of supply
I = Average current
V = Nominal Voltage
Wc = Energy in Joules

Example: A volt supply drawing 1 amp from a 25 kHz switching supply.

$W_c = 1 \times 5 \times 2 / 25{,}000 = .0004$

$C = .0004 * 2/25 = 32\ \mu F$

2.0 Recommended PCB Layout Guidelines for the M289XX

In addition to the General Layout Requirements, the following rules must be followed to achieve optimum performance of the M289XX.

2.1 Bulk Capacitor Placement

Mount all bulk and parallel 1.0 µF capacitors on the component side of the PCB. Route supply traces through the capacitors first and then connect to the respective planes with very short traces or with vias placed directly through the capacitor pads.

- There should be a bulk capacitor and a parallel 1.0 µF capacitor at the point where the supply enters the board and near any large chips.
- A bulk capacitor and a parallel 1.0 µF should be placed on both input and output of and voltage regulators on the PCB.
- Bulk decoupling should be repeated on large boards for every 25^2 inches of board space.

2.2 Decoupling Capacitor Placement

Place 0.1– 0.001 µF ceramic capacitors with a stable temperature coefficient (i.e., NPO, COG, X7R) on the component side of the circuit board between power and return (ground) pin pairs (Table 2-2 below). Place as close to the components and pins they are supporting as physically possible. The pin pairs should be routed to the capacitors and the capacitor pads should be connected to the respective power and ground planes below with vias mounted on the inside edge of the capacitor pads. On the MX289XX BGA package, is be necessary to place some of the decoupling capacitors on the bottom of the board near the vias they are supporting.

NOTE: It may not be possible to decouple all pin pairs with short traces, and in fact, some of the routing may result in larger current loops. If this is the case, do not route these pins to capacitors; instead, tie them directly to the plane and put the decoupling capacitor close by.

2.3 Power Supplies and Return/Reference Planes

The M289XX requires 4 or 5 separate power supply circuits. +1.8 VDD (digital Core for the DSP), +3.3 VDDO (I/O supply for the DSP), 3.3 VAA (AFE core), 12 VAA (Line Driver for the AFE), and an additional +5 VDD can be applied to VGNN (ball R4 of the DSP) to allow the DSP inputs to be 5 V tolerant for interfacing with TTL components. These supplies can be generated by the same source but should be treated as separate supplies with separate bulk decoupling capacitors for each.

There should be at least one (preferably more) solid reference plane covering an entire layer of the board. This layer should be adjacent to the power plane layer.

Both the top and bottom layer of the board should be flooded with copper wherever possible. This copper should be tied to the reference layers(s) below.

NOTE: No copper islands should be left floating.

Place an 1/8 inch thick trace around the outside perimeter on both sides of the entire board and tie it to the return plane with a via every ½ inch. Do not route any signals outside of this perimeter.

The bottom of the MX289XX (AFE) contains an exposed copper pad/heat sink and should be soldered to an exposed metal island on the top layer of the board. This island can be used as a quiet analog ground and all of the return pins from the AFE can be routed to it. See chapter *Electrical and Mechanical Specifications* of the M28975 data sheet contains a procedure for the proper layout and solder assembly of the LGA package. This procedure must be followed to ensure optimal performance of the AFE.

2.4 UTOPIA II Bus

When routing the UTOPIA II bus, keep the signal/control lines as short as possible, provide close returns (reference plane), and proper termination.

When the UTOPIA II bus is supporting multiple interfaces, the ATM_RX_CLAV and the ATM_TX_CLAV should have 750-Ω pull-down resistors added.

When the UTOPIA interface is not used, certain pull-ups and pull-downs should be provided to ensure proper operation of the DSP (see Table 2-1).

Table 2-1. Pull-ups and Pull-downs

Pull-ups	Pull-downs	Pull-up or Down
ATM_RX_ENB ATM_TX_ENB	ATM_TX_SOC	ATM_TX_DAT(0:16) ATM_TX_ADDR(0:4) ATM_RX_ADDR(0:4) ATM_TX_PRTY ATM_TX_CLAV

2.4.1 Crystal

Mount the crystal as close to balls R1 and P2 on the MX289XX (DSP) as possible. Use wide traces and bury them if necessary. (See Chapter 1.0 for layout requirements)

2.5 Analog Section

2.5.1 AFE/Hybrid Placement

The AFE/hybrid should be placed in a quiet area of the PCB away from all digital and clock signals. The exposed copper pad on the ELQFP should be soldered to an analog reference island on the top layer of the board.

NOTE: Follow the ELQFP layout and solder procedure, described in *Electrical and Mechanical Specifications* Chapter of the M28975 data sheet.

2.5.2 Hybrid Layout and Routing

Layout hybrid components symmetrically. The traces should be short, direct, equally wide and of the same length. They should flow symmetrically and be close together whenever possible. Mount the anti-alias filter components as close to the AFE as physically possible. The traces coming from pins 20–23 of the AFE should be kept very short. If this cannot be achieved, they must be routed as differential pairs and guarded on both sides with analog returns on an inside layer to increase noise immunity.

Table 2-2. Decoupling capacitor Placement—Pin Pairs (1 of 2)

AFE Power (8927 AFE)	AFE Return
3	2
11	10
13	12
33	32
38	—
41	43
45	43
DSP Power (8945 DSP) CABGA	**DSP Return CABGA**
E1	E4
F1	F3
J3	H3
J1	L3
M4	K1
N2	P1
R2	R3
N6	R6

Table 2-2. Decoupling capacitor Placement—Pin Pairs (2 of 2)

N9	N8
N11	R9
R10	P11
M14	L15
J12	K13
H14	G13
G15	F14
D12	F15
B12	A11
D9	C10
B8	C7
A7	B6
D4	A6

2.5.3 Level Shifting Capacitor Placement

The M28927-XX AFE/LD uses a push/pull class D amplifier to generate its line driver output. Level shifting capacitors are required to maintain the proper DC level at the inputs of the class D amplifier. Parasitic reactive elements at these inputs can shift the input signal, causing a signal overlap and excessive current draw from the Line Driver circuitry. This excessive current draw can lead to reduced life expectancy or, in extreme cases, eventual failure of the M28927-XX AFE/LD. To eliminate this effect, the Level Shifting capacitors must be mounted on the component side of the PCB as close to the M28927-XX AFE/LD level shifting pins (pins 39 & 40, and 46 & 47) as physically possible. The routed traces should be short (<2mm, 0.08 inch and as thick as the pin pads (~0.25mm, 0.01 inch). Ideally, the capacitors should be mounted across the pin pair pads.

2.5.4 Recommended Surge Protection and Layout

This surge protection circuit has been tested on our M289XXEVM and is compliant with all Belcore GR 1089 and ITU-T K20 & K21 lightning surge and power cross longitudinal and metallic tests. The signal traces on the line side of the transformer must be a minimum of .025 inch wide and be spaced at least 0.1 inch from any other metal or traces. The SIDACtors can be a triple SIDACtor component (as shown), or made up of three separate single SIDACtor components. It is not necessary to eliminate the return plane in this area, however to eliminate the possibility of arching during a surge event, there should not be any copper flood on the top and bottom layer of the PCB in the area between the line transformer and the line connector.

Figure 2-1. Surge Protection Topology

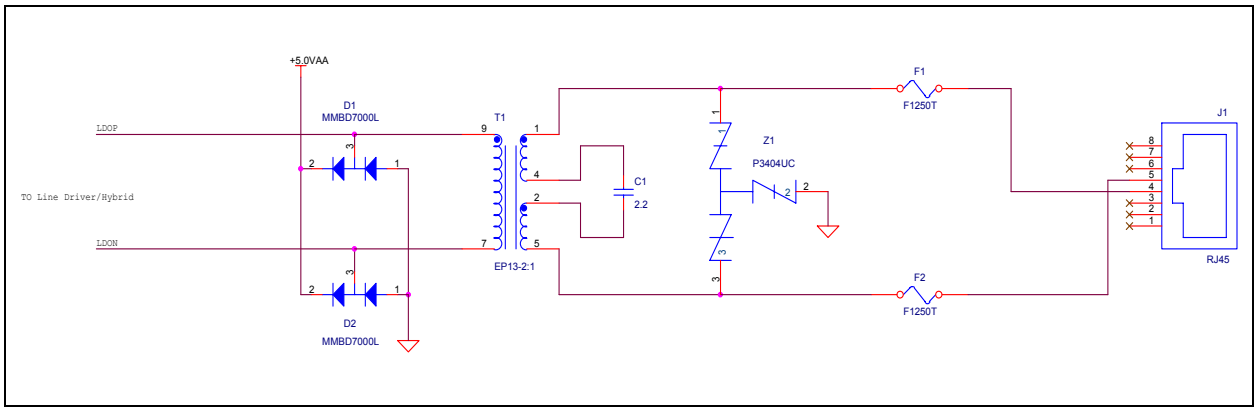


Table 2-3. Surge Protection Scheme Bill of Materials

Bill of Materials

QTY	REF DES	VENDOR	PART NUMBER
2	D1, D2	Motorola	MMBD7000L
1	C1	Any Vendor	1 - 2.2uF, 50V
1	T1	Midcom	50772
1	Z1	Teccor	P3404UC
2	F1, F2	Teccor	F1250T
1	J1	Any Vendor	RJ-45

NOTE: If primary protection is available, A Teccor F0500T should be used in place of the F1250T

NOTE: Components may vary dependending on application and protection standard requirements.

Appendix A. BOM, Layout, and Schematics

Table A-1. Bill of Materials for the M289XX EVM Line Card , Page 1 of 2

M28975 EVM Line Card Bill of Materials
Revised: Thursday, Sep 04, 2003
PCB Revision: BT02-D135-011
Assembly Revision: BT02-D130-081
Hybrid: H306
Mindspeed Technologies
4000 MacArthur Blvd
Newport Beach, CA 92660

#	QTY	REF DES	MFG	PART NUMBER	DESCRIPTION
1	29	C1,C2,C5,C6,C7,C8,C9,C10,C11,C12,C13, C14,C15,C16,C17,C18,C19,C29,C30,C31, C32,C33,C62,C63,C82,C84,C86,C87,C88	PANASONIC	ECJ-1VB1C104K	CAP, 0.1UF, 16V, X7R, 0603, 20%
2	4	C20, C22, C23, C25	TDK	C1608X5R1A105KT	CAP, 1.0UF, 10V, X5R, 0603,10%
3	25	C3,C4,C26,C34,C35,C36,C37,C38,C39,C40,C41,C42,C 43,C44,C45,C46,C47,C48,C49, C50,C51,C52,C53,C54,C55	PANASONIC	ECJ-0EB1C103K	CAP, 0.01UF, 16V, X7R, 0402, 10%
4	2	C21,C24	PANASONIC	ECJ-1VC1H331J	CAP, 330PF, 50V, NPO, 0603, 5%
5	2	C27,C28	PANASONIC	ECJ-1VC1H220J	CAP, 22PF, 50V, NPO, 0603, 5%
6	2	C56,C58	TDK	C2012COG1E103J	CAP, 0.01UF, 50V,COG, 0805, 5%
7	1	C57	TAIYO YUDEN	EMK316BJ225MC	CAP, 2.2UF, 16V, X7R, 1206, 10%
8	2	C59,C61	TDK	C3225COG1H393J	CAP, 0.039UF, 50V COG, 1210, 5%
9	1	C60	TDK	C2012COG1H272J	CAP, 0.0027 UF, 50V COG, 0805, 5%
10	6	C65,C68,C74,C77,C79,C99	AVX	TAJC226M016	CAP, 22UF, 16V, TANT, 2312_C, 20%
11	6	C66,C69,C75,C78,C81,C100	PANASONIC	ECJ3YB1E105K	CAP, 1.0UF, 25V, X7R, 1206, 10 OR 20%
12	1	C83	AVX	TACR475M010R	CAP, 4.7UF, 6.3V OR 10V, TANT, 0805, 20%
13	8	C91,C92,C93,C94,C95,C96,C97,C98	PANASONIC	ECJ-0EC1H150J	CAP, 15PF, 50V, NPO, 0402, 5%
14	2	C102,C103	PANASONIC	ECJ-0EB1H152K	CAP, 100PF, 25V, NPO, 0402, 5%
15	2	C104,C105	TDK	C3216X5R0J103MT	CAP, 10.0UF, 6.3V, X7R, 1206, 20%
16	1	C106	TDK	C2012COG2A472J	CAP, 0.0047UF, 25V, COG, 0805, 5%
17	5	D1,D9,D10,D12,D13	PANASONIC	LN1371G	LED, GREEN, 20MA, GULL WING-S TYPE
18	7	D2,D3,D4,D5,D6,D7,D8	PANASONIC	LN1271R	LED, RED, 20MA, GULL WING-S TYPE
19	2	D15, D16	MOTOROLA	MMBD70000LT1	DIODE, DUAL SWITCHING, SOT 23
20	1	Q1	ONSEMI	MMBT2484LT1	TRANSISTOR, NPN, SOT-23
21	2	F1, F2	TECCOR	FUS60ASMD036	FUSE, TELELINK
22	1	Z2	TECCOR	P3403AC	Sidactor, TO-220, Balanced Three Chip
23	2	L1A, L2A	TOKO	FSLB2520-6RM8 or 8M	INDUCTOR, 6.8 UH, +/- 20%, DCR .065, 0805
24	2	L3,L4	TDK	MMZ1608Y102B	BEAD, FERRITE, DCR 0.6, Z 1000 OHM, 190MA, 0603
25	1	J6	MOLEX/BEAU	830502	CONN, TERMINAL BLOCK, 2 POSITION
26	1	J7	MOLEX	95040-2881/ MOL950-40-2881	CONN, RJ45, INTERNAL SHIELD, RIGHT ANGLE
27	2	J8, J10	MOLEX	71741-0001 or 71741-0002	CONN, MEZZANNINE, 2 X 42, SMT
28	1	J9	MOLEX	71436-2164	CONN, MEZZANNINE, 2 X 32, SMT
29	1	P1	MOLEX	83619-9003	CONN, MICRO D, DUAL - 9-PIN
30	19	R92,R93,R94,R95,R96,R97,R98,R125,R126,R127,R128 ,R129,R130,R131,R132,R133, R134,R135,R136	KOA	RM73Z1E000	RES, ZERO OHM, 0402
31	3	R167,R168,R169	KOA	RM73Z2A000	RES, ZERO OHM, 0805
32	4	R72,R73,R74,R75	KOA	RK73H2A8R25F	RES, 8.25 OHM, 0805, 1%

Table A-1 (cont'd): Bill of Materials for the M289XX EVM Line Card , Page 2 of 2

33	41	R14,R15,R16,R17,R18,R19,R20,R21,R22, R23,R24,R25,R26,R27,R28,R29,R30,R31, R32,R33,R34,R35,R36,R52,R53,R54,R55, R56,R57,R58,R59,R60,R61,R62,R64,R65, R66,R67,R68,R165,R166	KOA	RK73H1E33R2F	RES, 33.2 OHM, 0402, 1%
34	8	R44,R45,R46,R47,R48,R49,R50,R51	KOA	RK73H1E82R5F	RES, 82.5 OHM, 0402, 1%
35	4	R77,R78,R80,R81	KOA	RK73H1E3090F	RES, 309 OHM, 0402, 1%
36	9	R101,R155,R156,R157,R158,R159,R160, R161,R162	KOA	RK73H1E3320F	RES, 332 OHM, 0402, 1%
37	1	R172	KOA	RM73B1ETE331J	RES, 330 OHM, 0805, 5%
38	2	R100,R103	KOA	RK73H1E4990F	RES, 499 OHM, 0402, 1%
39	4	R3, R6, R9, R12	KOA	RK73H1E6040F	RES, 604 OHM, 0402, 1%
40	2	R37,R38	KOA	RK73H1E7500F	RES, 750 OHM, 0402, 1%
41	2	R70,R121	KOA	RK73H1ET1001F	RES, 1K OHM, 0402, 1%
42	1	R104	KOA	RK73H1E1211F	RES, 1.21K OHM, 0402, 1%
43	1	R79	KOA	RK73H1E1911F	RES, 1.91K OHM, 0402, 1%
44	16	R39,R40,R41,R42,R43,R63,R90,R91,R116, R117,R118,R119,R120,R124,R153,R154	KOA	RK73H1E1002F	RES, 10K OHM, 0402, 1%
45	1	R1	KOA	RK73H1E1102F	RES, 11K OHM, 0402, 1%
46	26	R106,R107,R108,R109,R110,R111,R112, R113,R114,R115,R137,R138,R139,R140, R141,R142,R143,R144,R145,R146,R147, R148,R149,R150,R151,R152	KOA	RK73H1ET1003F	RES, 100K OHM, 0402, 1%
47	2	R170, R171	Philips	2322-706-7-3242	Res, 32,400, 1/16W, 1%, 0402
48	1	SW1	GRAYHILL	97S04SR	SWITCH, SPST, SM, 4 POSITION DIP
49	1	SW3	PANASONIC	EVQPHP03T	SWITCH, PUSH BUTTON, MINI
50	1	T1	MIDCOM	50772	XFMR, 2:1, EP13, THROUGH HOLE
51	1	U1	MINDSPEED	M28927-29P	IC, AFE, 48 ETQFP
52	1	U2	MINDSPEED	M28945-13	IC, DSP, 13MM, 176 PIN CABGA
53	1	U3	MAXIM	MAX3232EEAE	IC, RS-232 TRANSCEIVER, 16SSOP, 3.3V
54	1	U4	MOTOROLA	MC74AC541DW	IC, OCTAL TRI-STATE BUFFER, 20 SOP-W, 3.3V
55	1	U5	TI	SN74LVTH273PWR (LXH273)	IC, OCTAL D FLIP-FLOP W/ CLEAR,20SSOP, 3.3V
56	1	U6	MOTOROLA	SN74HCT32D	IC, QUAD, 2-INPUT OR GATE, SOIC-14, 3.3V
57	1	U8	PHILIPS	74LVQ138D	IC, 1 OF 8 DECODER/DEMUX, SOIC-16, 3.3V
58	1	U9	MOTOROLA	SN74HC08D	IC, QUAD, 2-INPUT AND GATE, SOIC-14, 3.3V
59	1	Y1	GED	PKHC4922.11840155	XTAL, 22.1184 MHZ, HC49, 15.5 PF, 32 PPM
60	1	Y1 INSULATOR	CTS	700-9001	INSULATOR, CRYSTAL, HC49
61	1	PCB		BT02-D135-011	PCB, BLACK
					NO LOAD: JP1-JP7, J3, J12-J14, J16-J22, J24-J29, J30,J31,L1,L2,R2,R4,R5,R7,R8,R10,R11,R13,R71,R83-R89,R99,R163,R164,R173,T2,Z1,

Figure A-1. Component Side

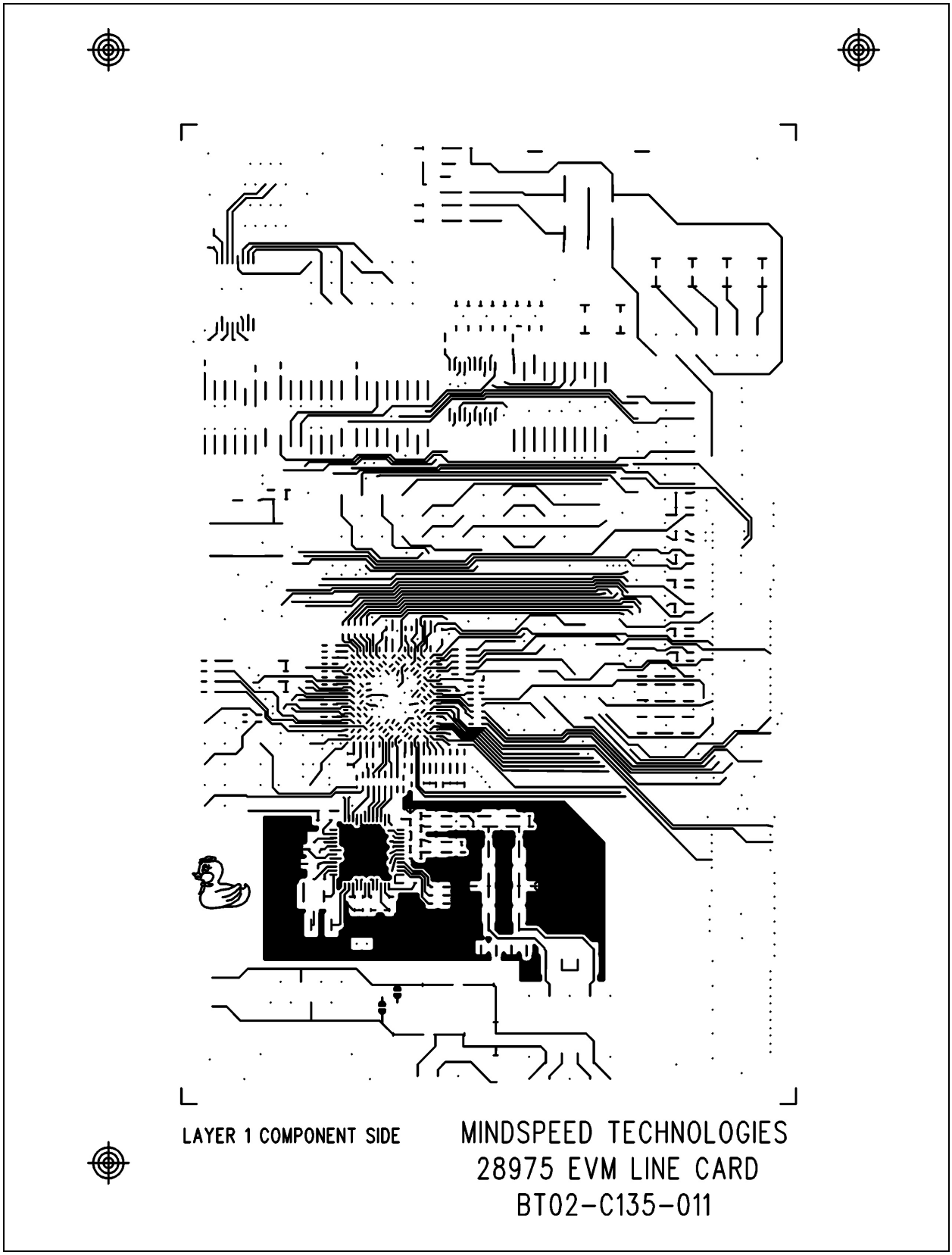


Figure A-2. Layers 2, 4, and 7 Ground Plane

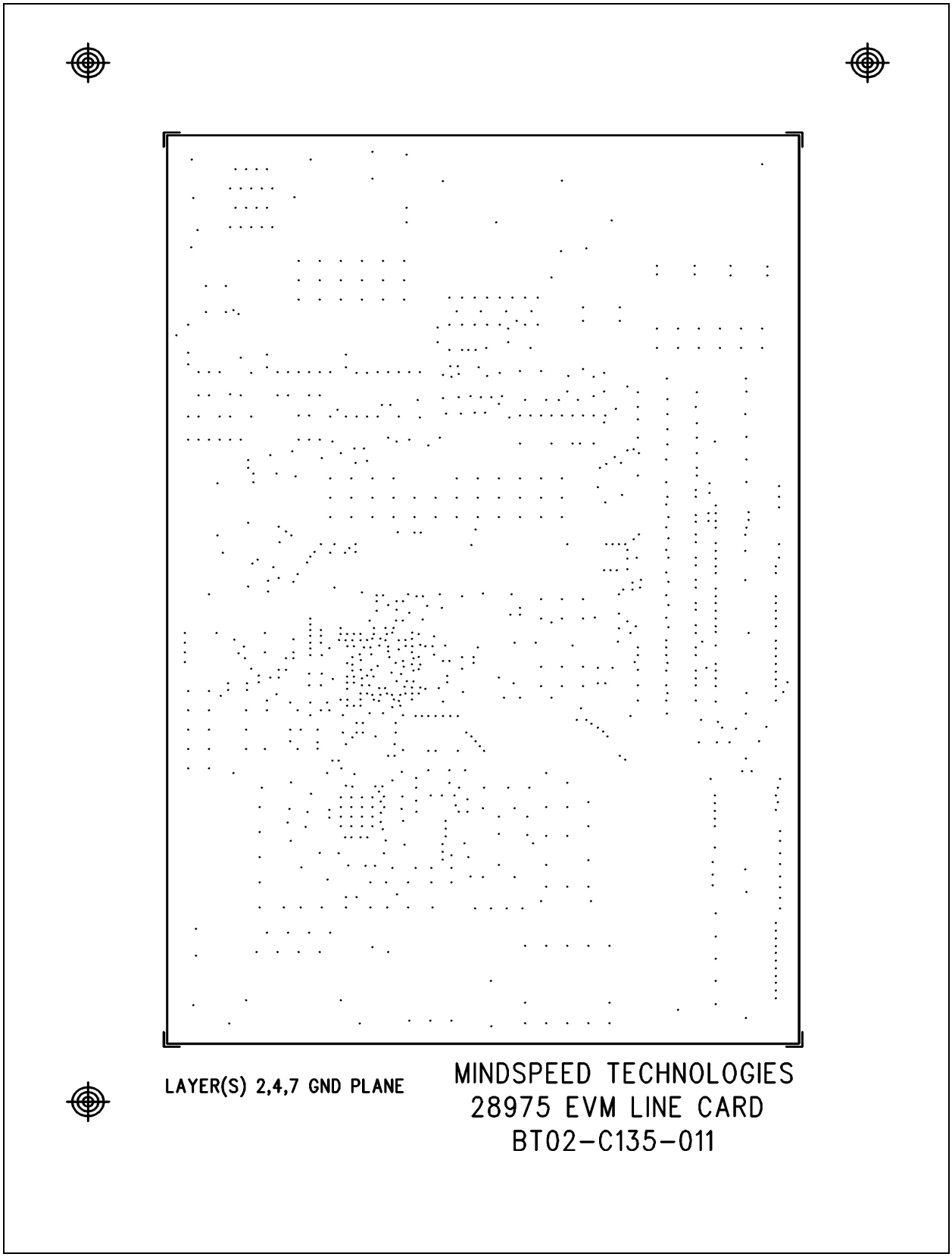


Figure A-3. Layer 3 Internal Signal

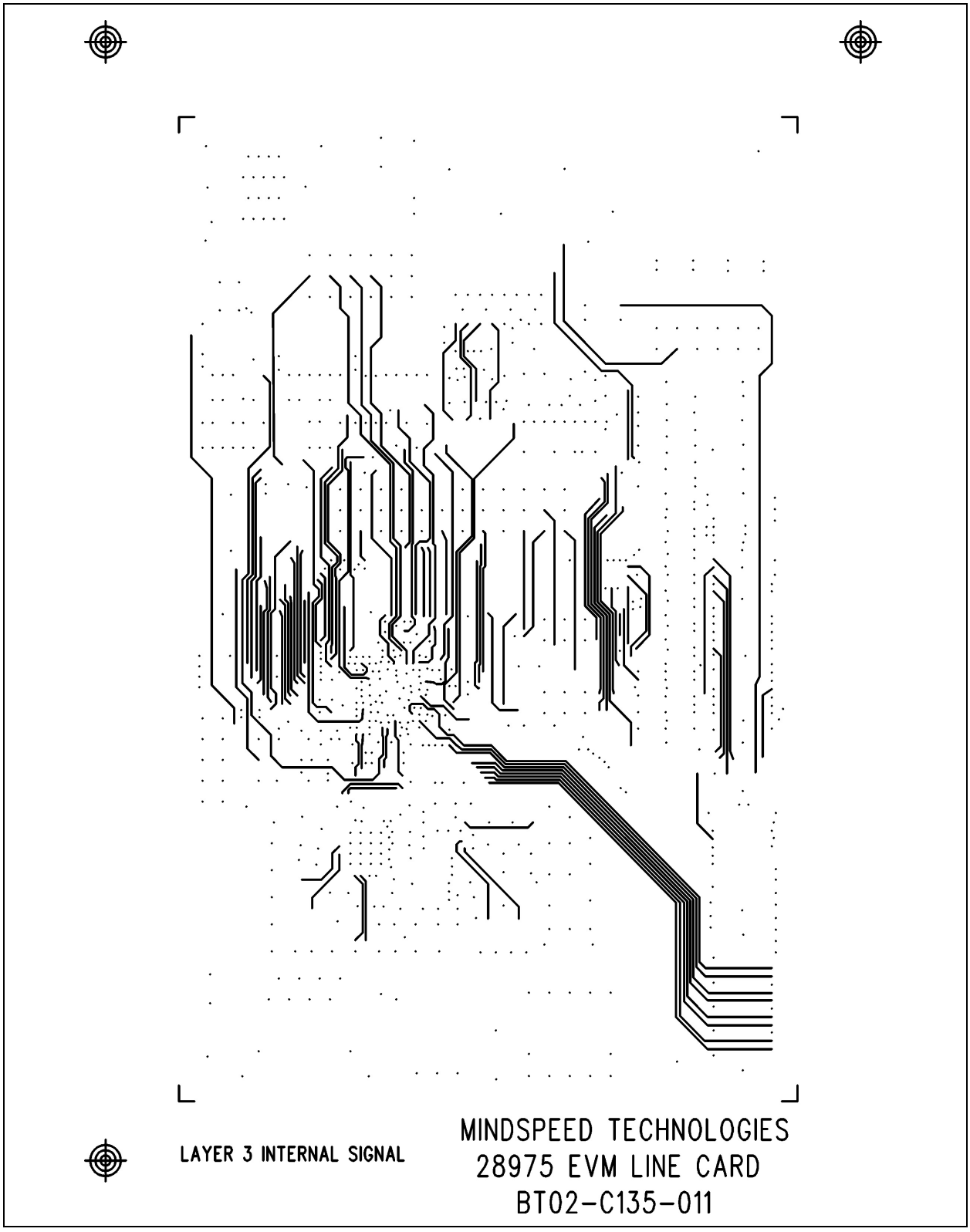


Figure A-4. Layer 5 Power Plane

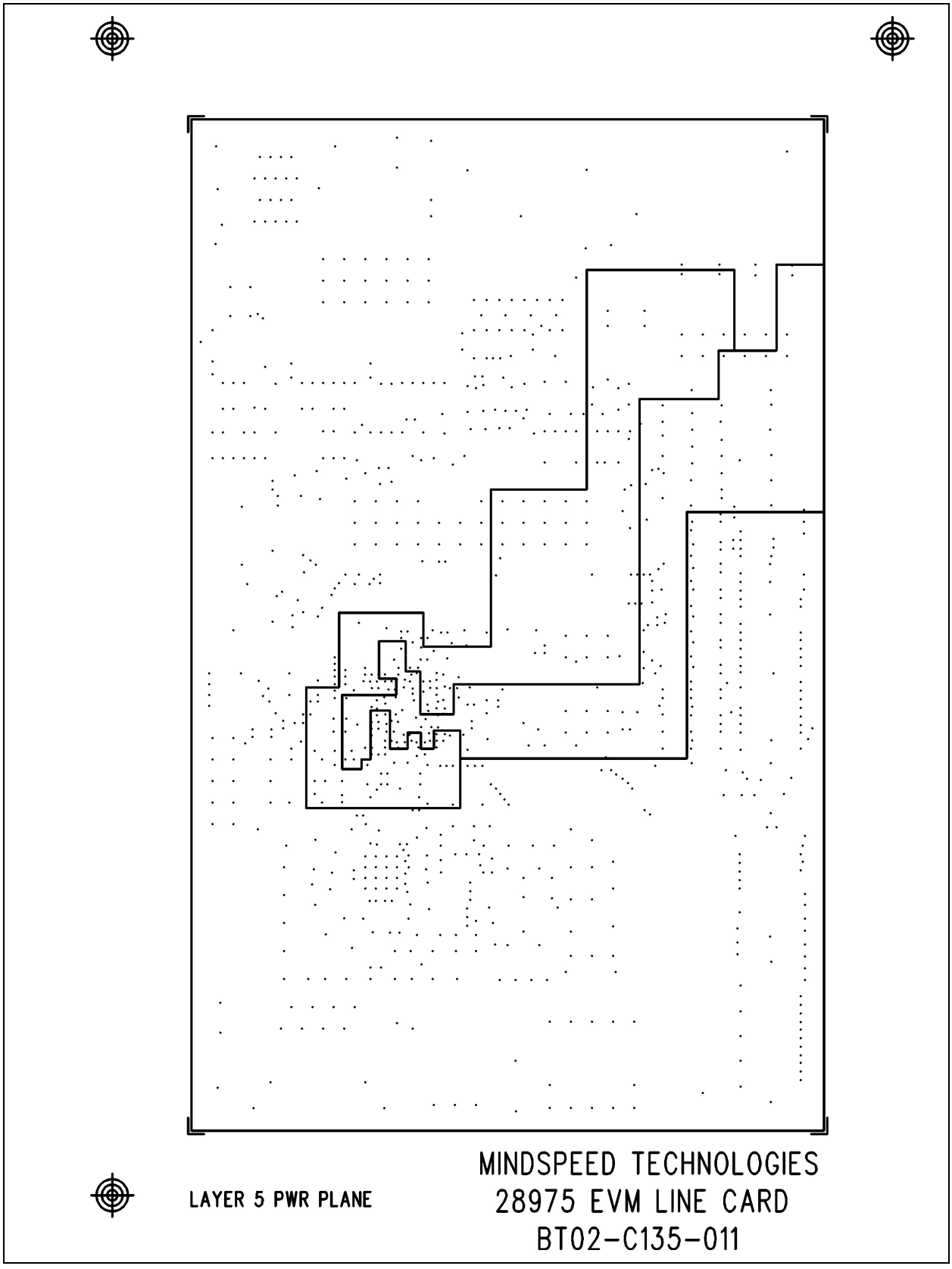


Figure A-5. Layer 6 Internal Signal

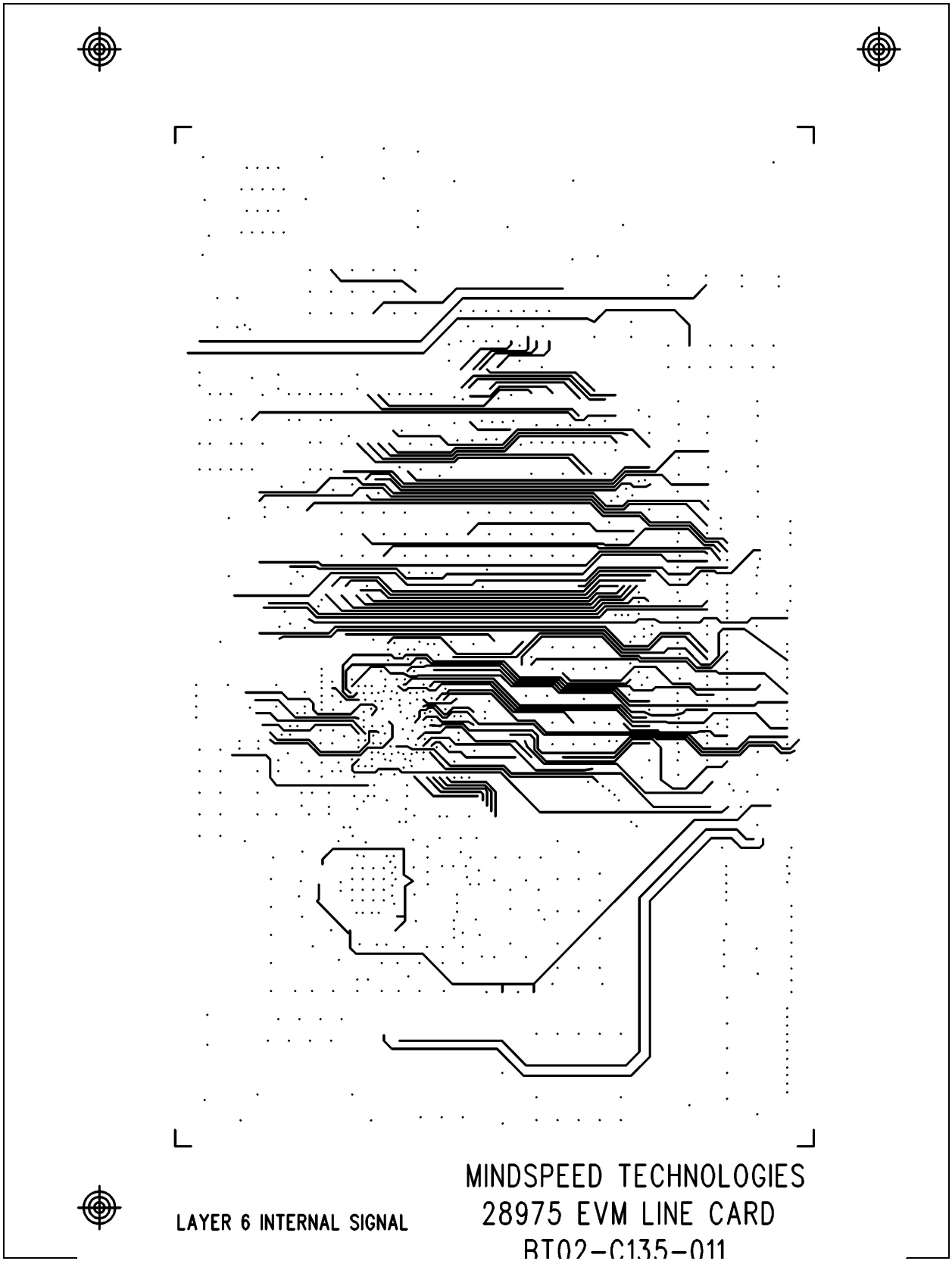


Figure A-6. Layer 8 Circuit Side

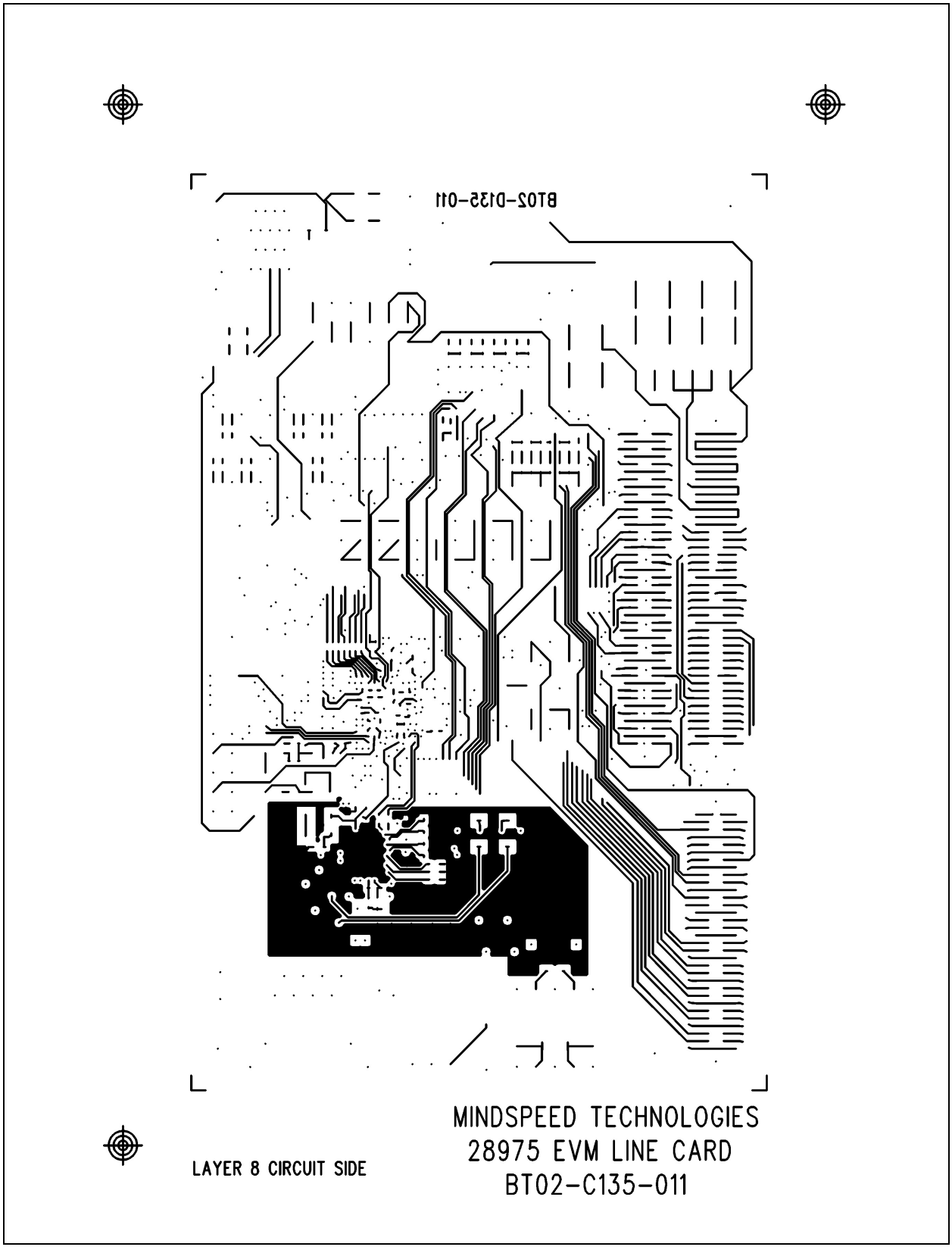


Figure A-7. Circuit Side Solder Mask

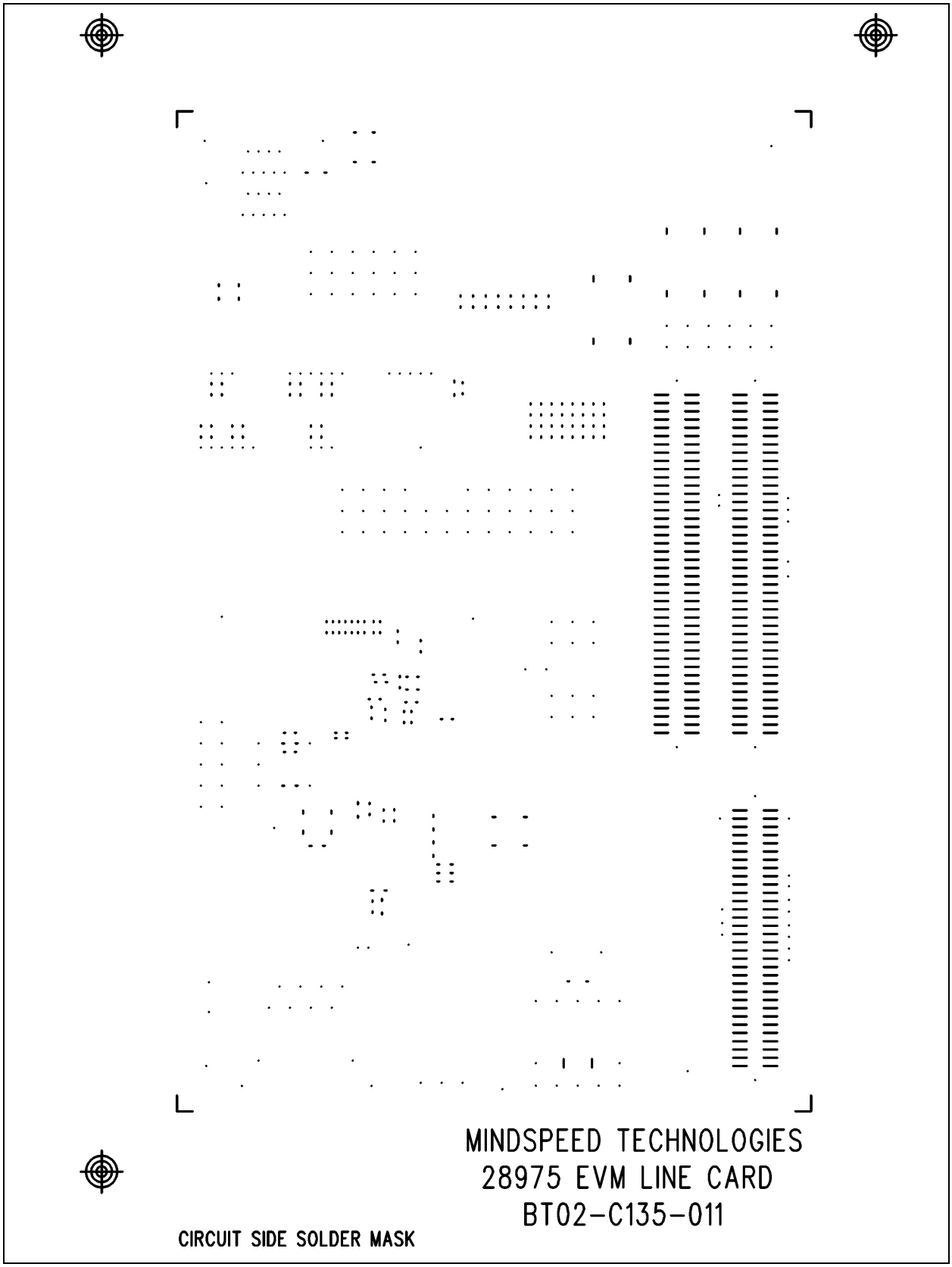
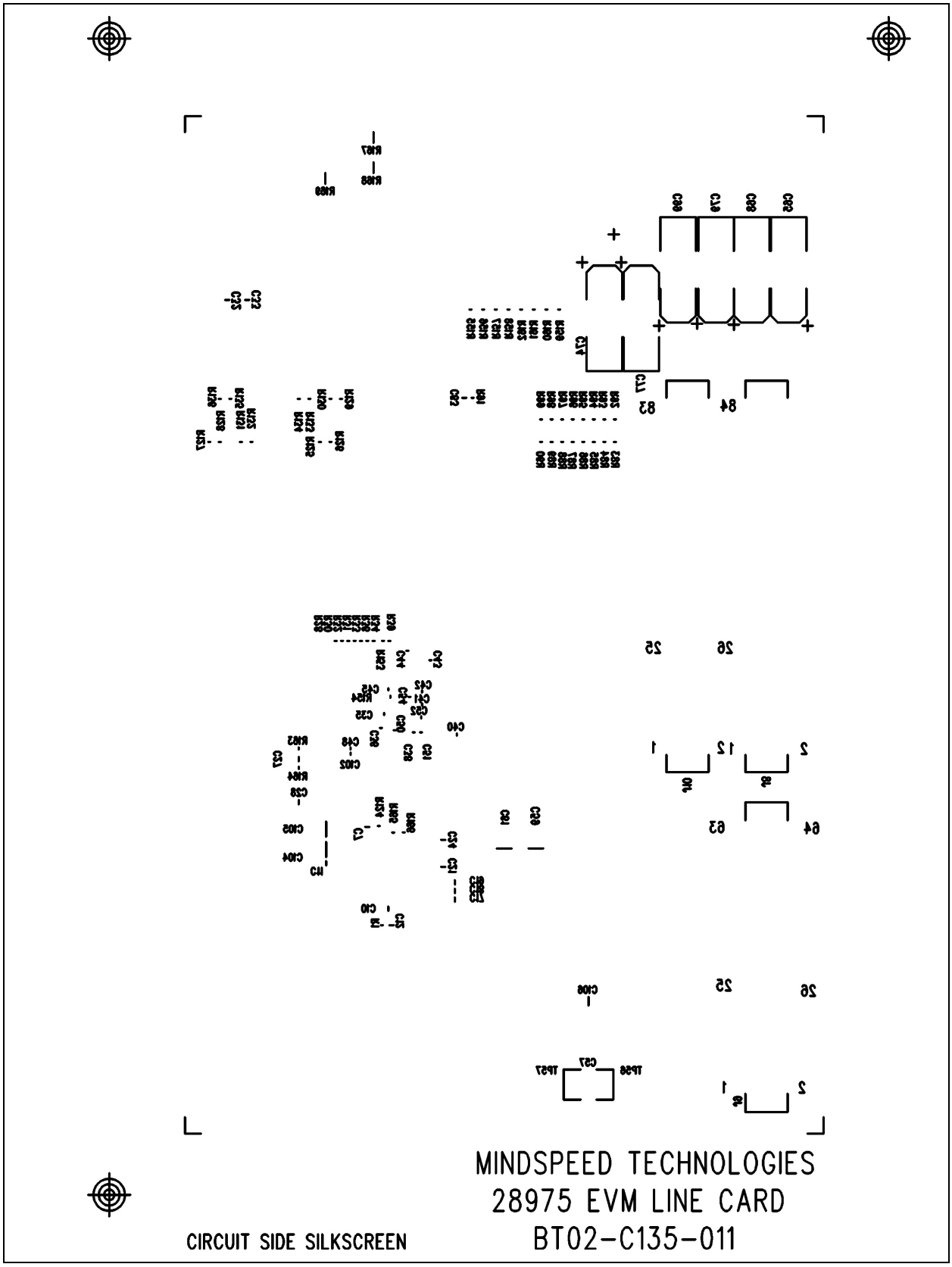
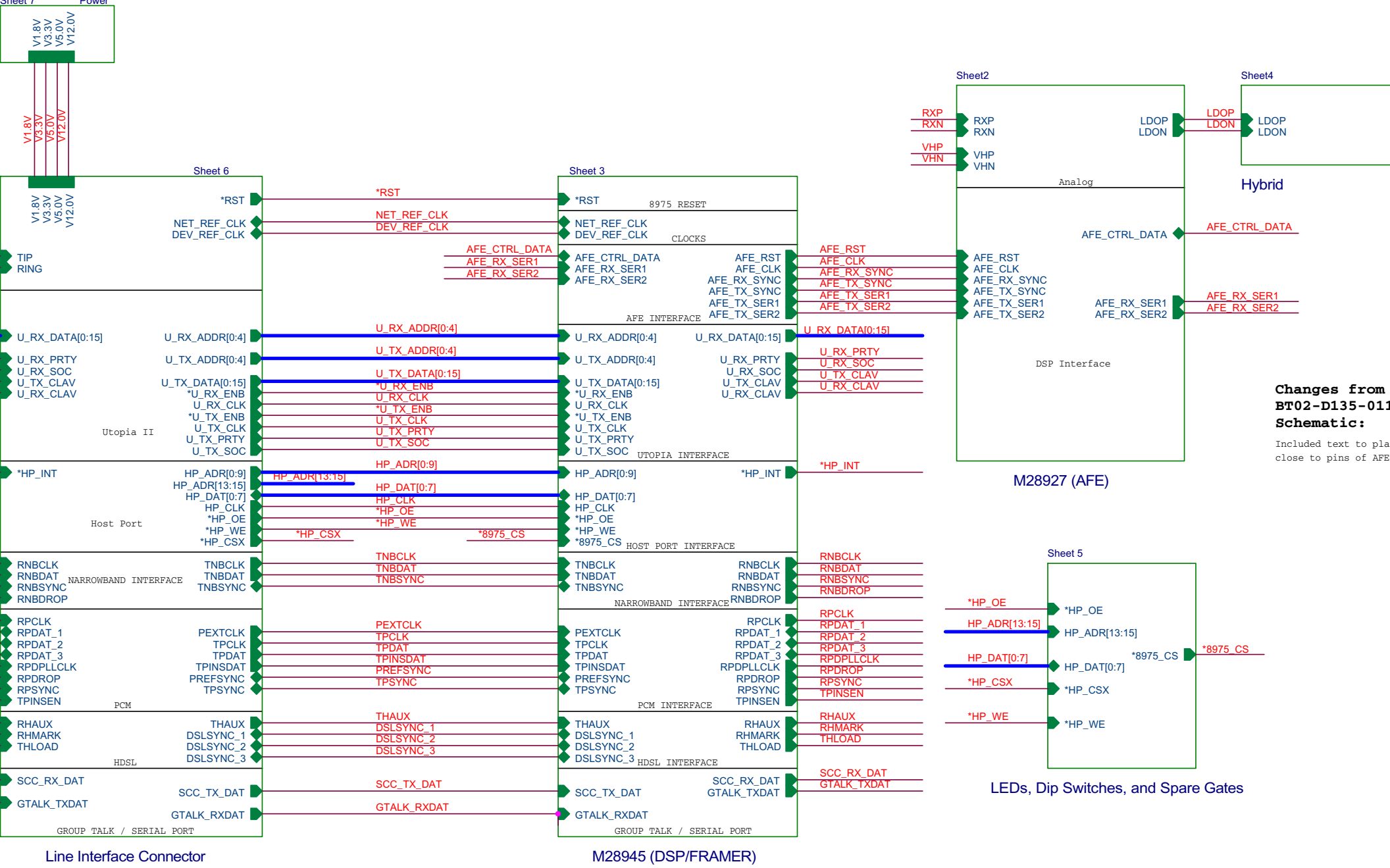


Figure A-8. Circuit Side Silkscreen





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8975 EVM Line Card -009

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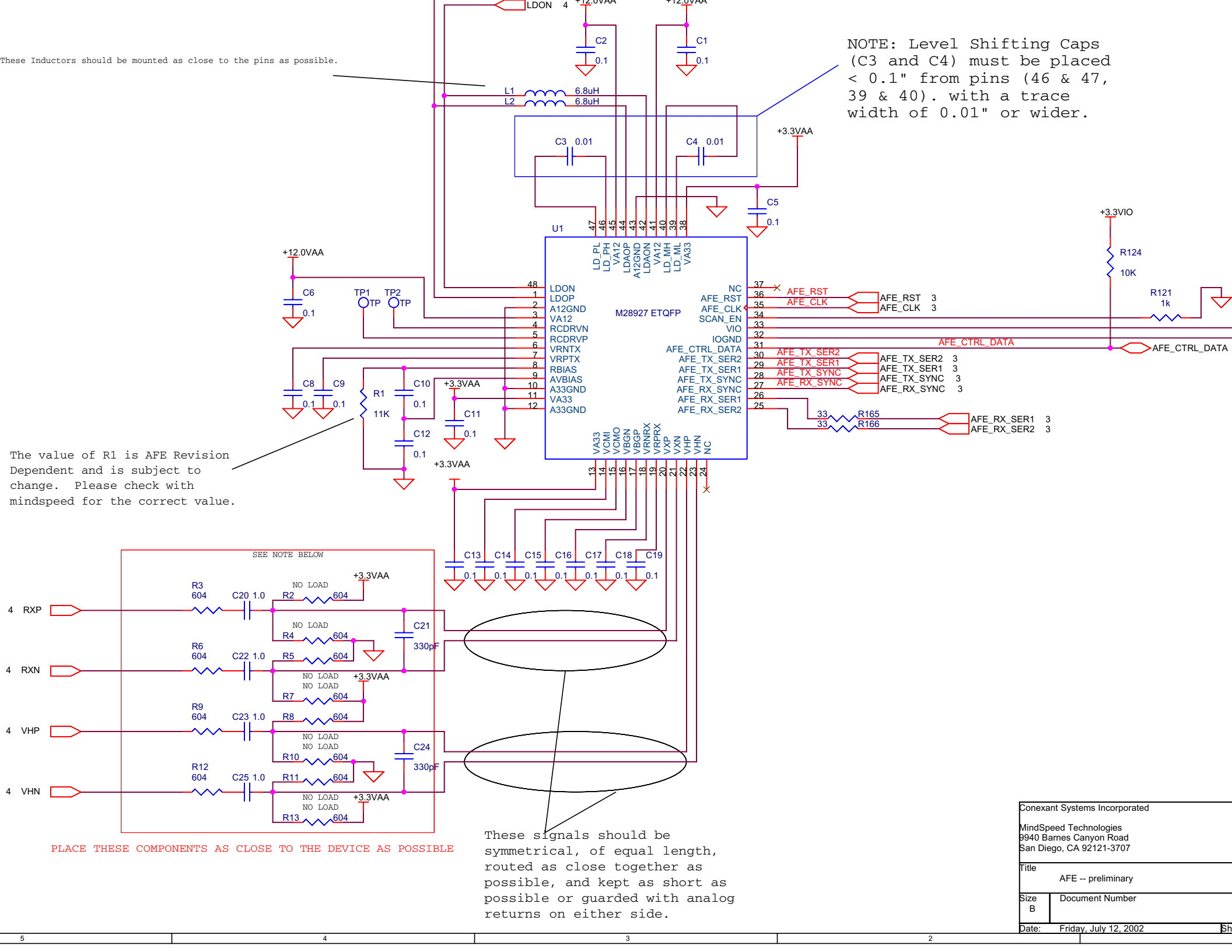

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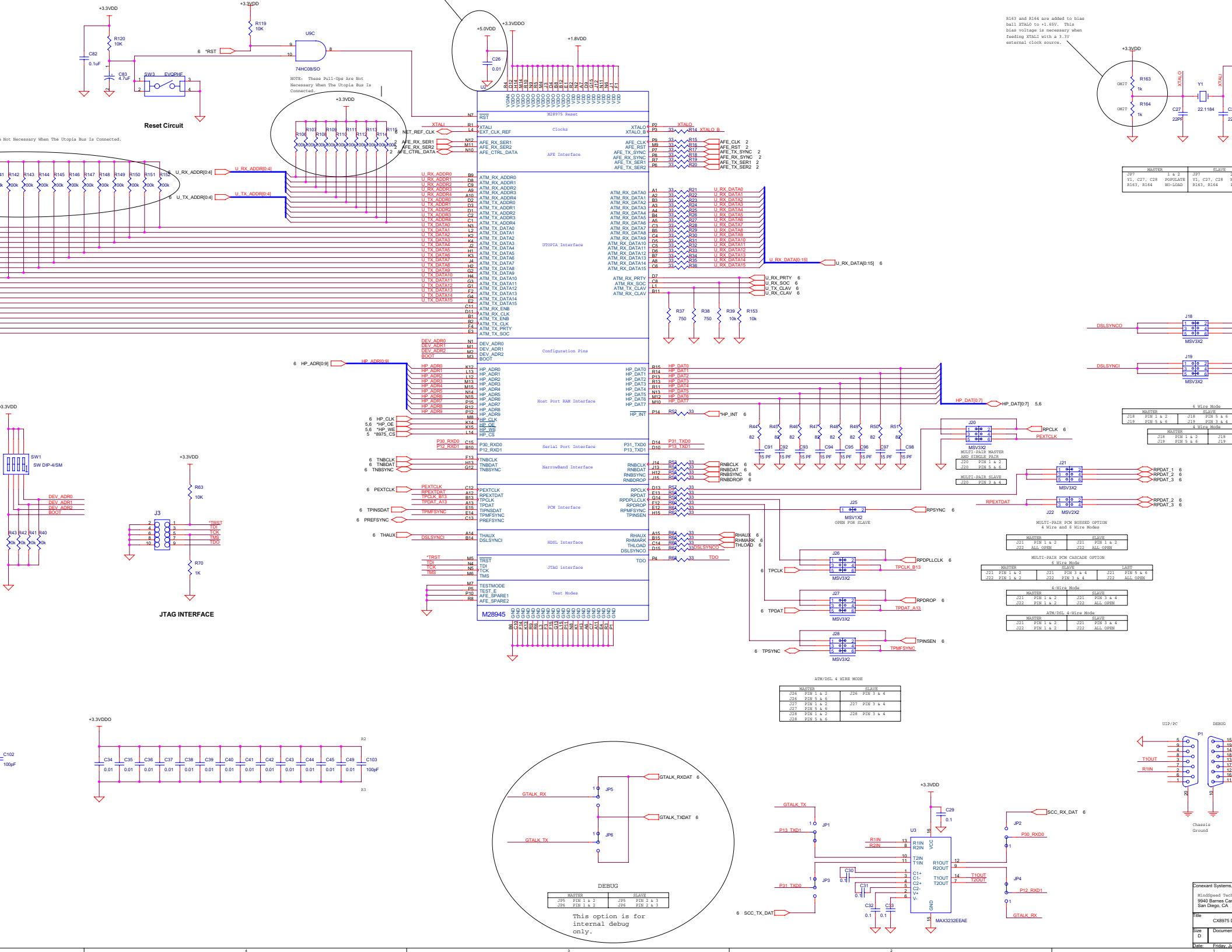
Reset Circuit
JTAG INTERFACE
DEBUG
M28945
M28975 Reset
Clocks
AFE Interface
UTOPIA Interface
Configuration Pins
Host Port RAM Interface
Serial Port Interface
NarrowBand Interface
PCM Interface
HDSL Interface
JTAG Interface
Test Modes
This option is for internal debug only.
MAX3232EEAE
R163 and R164 are added to bias ball XTALO to +1.65V. This bias voltage is necessary when feeding XTALI with a 3.3V external clock source.
NOTE: These Pull-Ups Are Not Necessary When The Utopia Bus Is Connected.
ATM/DSL 4 WIRE MODE
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MindSpeed Tech
9940 Barnes Can
San Diego, CA
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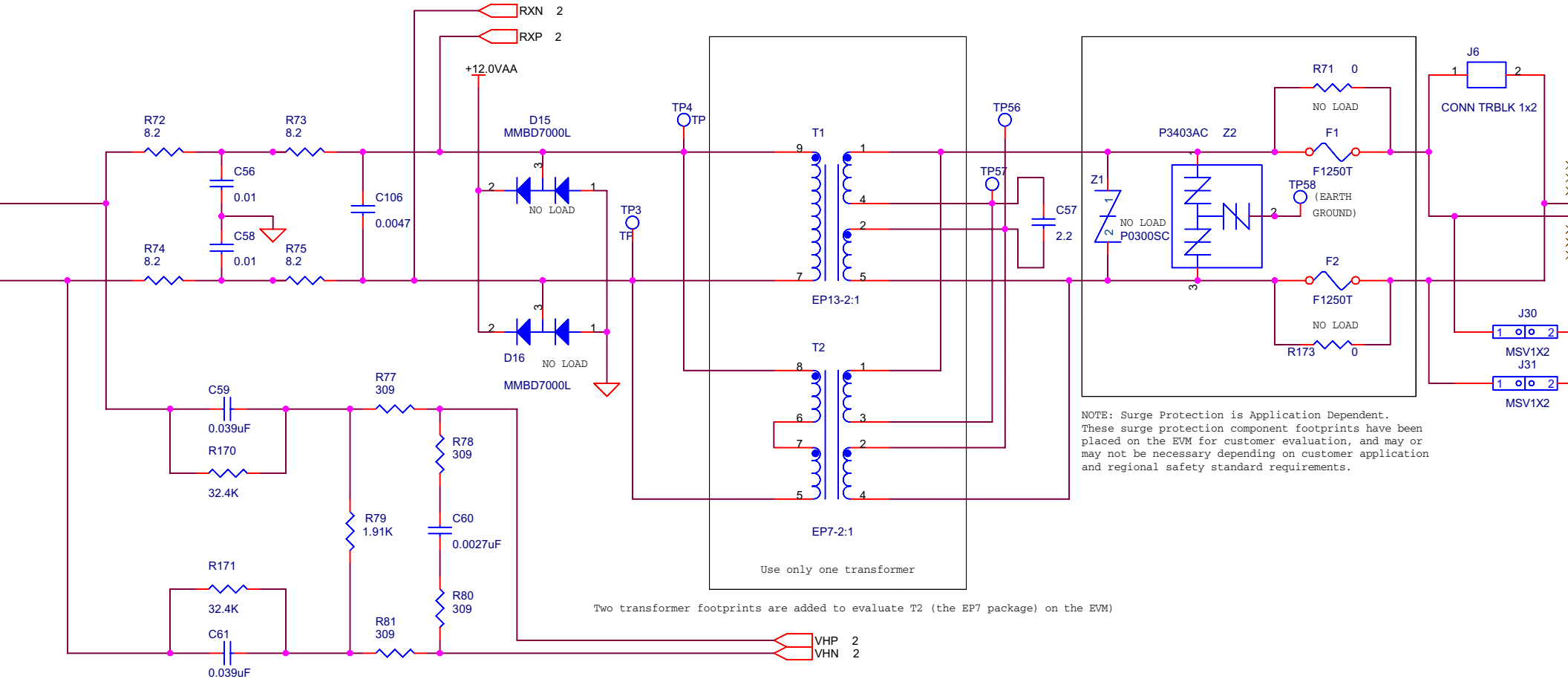

NOTE: Surge Protection is Application Dependent. These surge protection component footprints have been placed on the EVM for customer evaluation, and may or may not be necessary depending on customer application and regional safety standard requirements.

Hybrid #	R170/R171	R79
H305	No Load	2.2 Kohm
H306	32.4Kohm	1.91 Kohm

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Title: HYBRID -- preliminary

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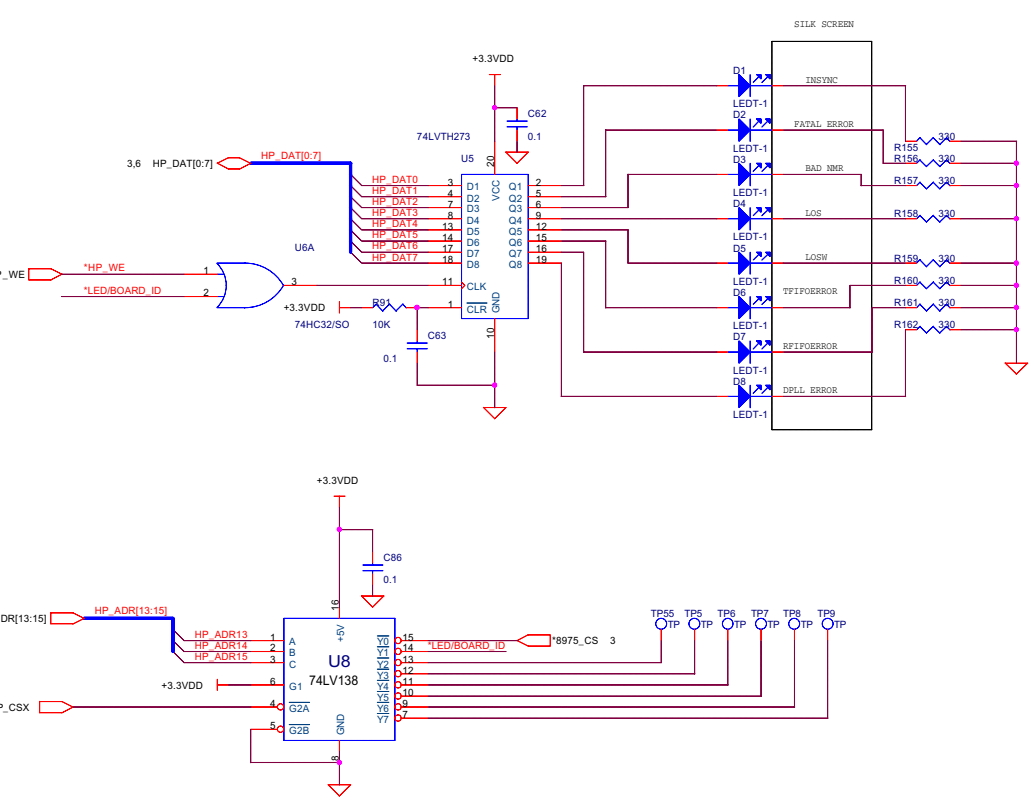

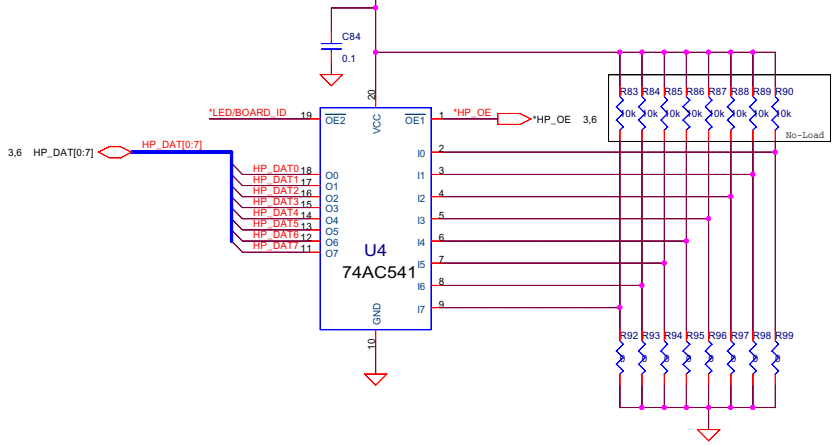

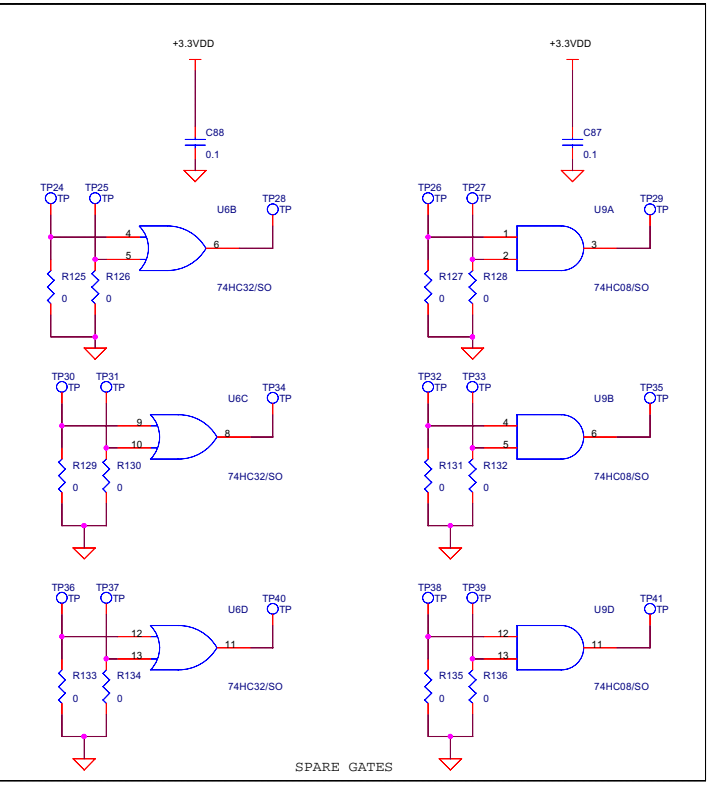

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Title: LEDs and DIP SWITCHES

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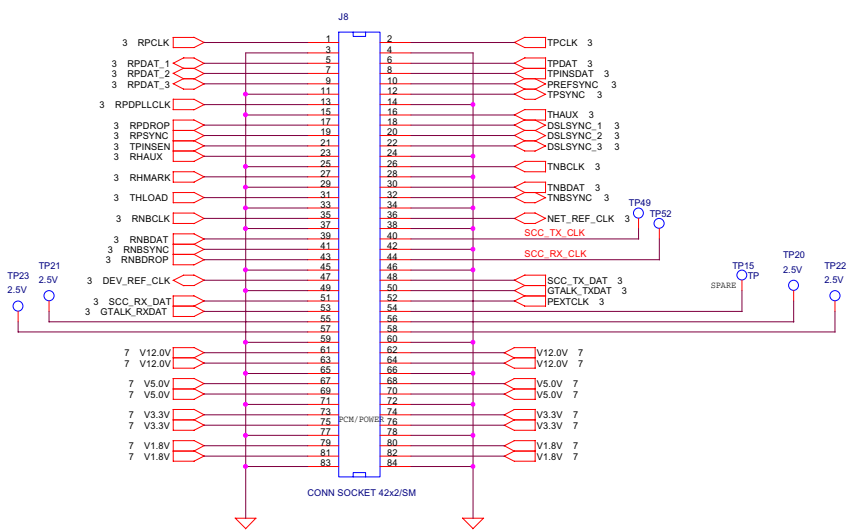

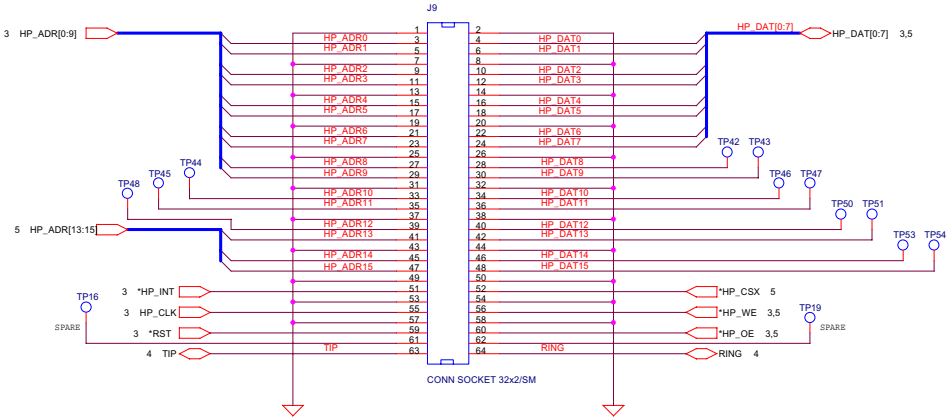

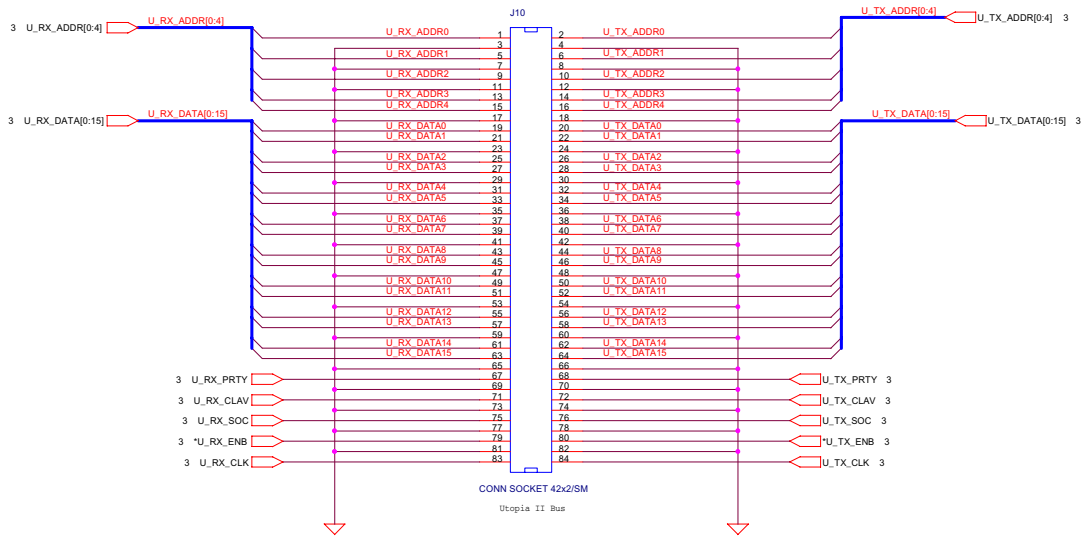

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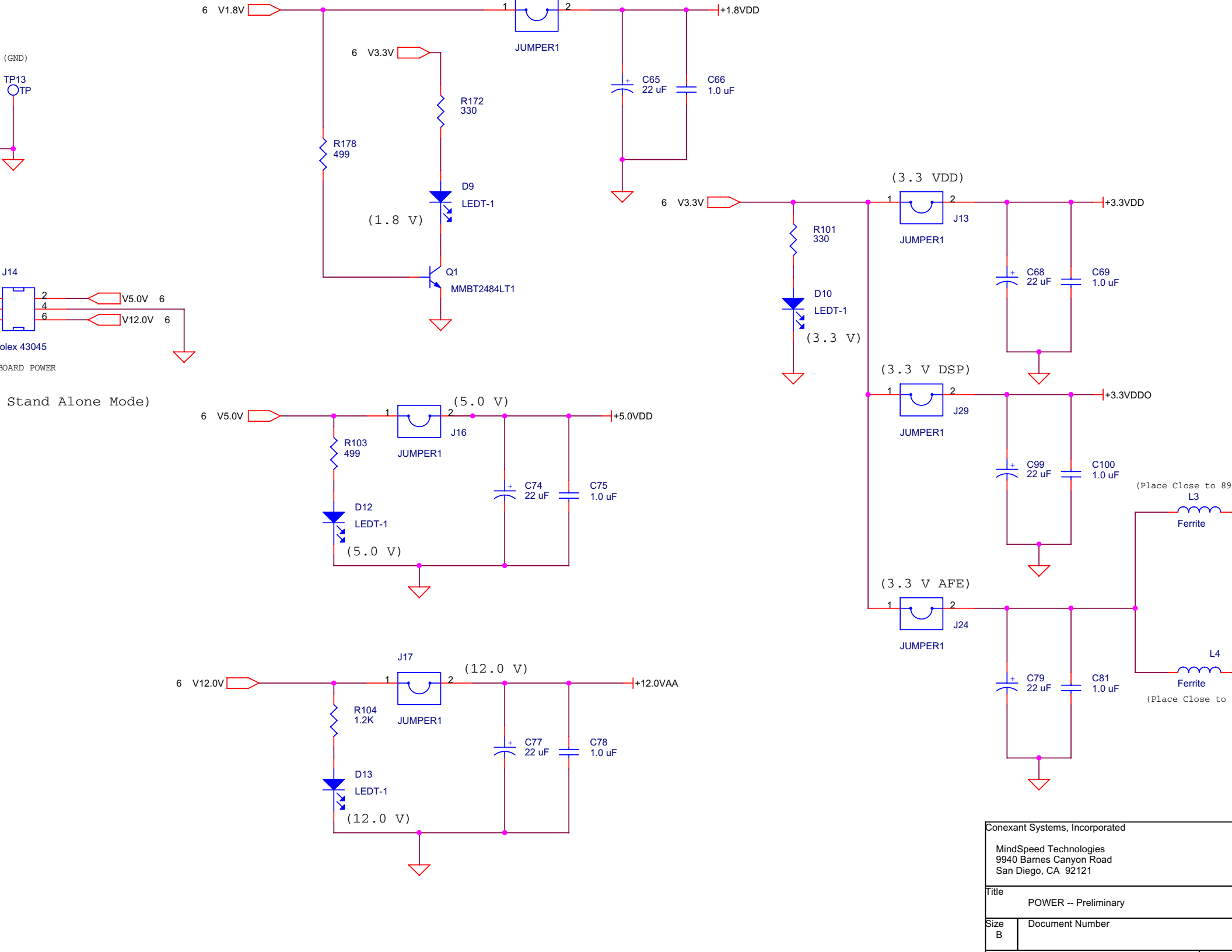
Title: Mother Board/Daughter Card Interface Connector

Size: C | Document Number

Date: Friday, July 12, 2002 | Sheet 6 of 7



Conexant Systems, Incorporated MindSpeed Technologies 9940 Barnes Canyon Road San Diego, CA 92121	
Title POWER -- Preliminary	
Size B	Document Number

Appendix B. References

Tom Van Dolen, Phd., *Circuit Board Layout to Reduce Electromagnetic Emission and Susceptibility*, Rolla, MO 2000.

Chuck Hubbard. *EMC Control*, Creative Date Devices, Camarillo, CA 1999.

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