MINDSPEED™

289xx-PBD-002-A
January, 2005

M28945/46/47/50 Non-conformance Information

Product Bulletin

Products Affected: M28945, M28946, M28947 and M28950

CLAD Malfunction

Description:

During G.shdsl mode training, one out of million times the Clock Rate Adapter block (CLAD) may generate a higher frequency clock, which will result in malfunction of the CLAD block or the device itself.

Scenario 1: Host interface functions normally but CLAD block fails

Workaround:

If the device fails to activate within ten retries, self-test will be performed inside the device to detect the CLAD lockup. If the self-test fails, the host port ram register 0x3C0 bit 5 will be set to a 1, equivalent to API 0x85 (DSL_STATUS). Upon detecting the bit the host processor should assert the reset pin on the device and download the firmware code. See reference API 0x85 as described below.

Scenario 2: Device lockup

Workaround:

If the device fails to acknowledge the api commands, the host processor should assert the reset pin on the device and download the firmware code.

<table>
<tr><th colspan="4">DSL Status</th><th>C</th><th>R</th></tr>
<tr><td colspan="6">This command queries the DSL Status registers. These status bytes provide dynamic information about the ZipWirePlus system.</td></tr>
<tr><th colspan="2">C Constant</th><th>Opcode</th><th>Type</th><th>Incoming Bytes</th><th>Outgoing Bytes</th></tr>
<tr><td colspan="2">_DSL_STATUS</td><td>0x85</td><td>Status</td><td>1</td><td>8</td></tr>
<tr><th colspan="6">Incoming Parameters</th></tr>
<tr><th>Byte</th><th>Content</th><th colspan="4">Description</th></tr>
<tr><td>1</td><td>Reserved</td><td colspan="4">Set to 0x00 for future compatibility.</td></tr>
<tr><th colspan="6">Outgoing Parameters</th></tr>
<tr><td>1</td><td>STATUS_1</td><td colspan="4">The STATUS_1 contains basic status of the system. The Host Processor should only be required to poll this one status register to see if the system is functioning, i.e., simple Go / No Go. See STATUS_1: DSL Status Bit Definitions for complete definition.</td></tr>
<tr><td></td><td></td><td colspan="4">STATUS_1: DSL Status Bit Definitions</td></tr>
<tr><td></td><td></td><td>Status_1 Bit</td><td colspan="2">Description</td><td>Bit Definition</td></tr>
<tr><td></td><td></td><td>7-6</td><td colspan="2">Activation Status</td><td>00 = Idle (_ASM_STAT_IDLE)
01 = Normal Operation (_ASM_STAT_SUCCESS)
10 = Deactivated (_ASM_STAT_DEACTIVAT E D)
11 = In-Progress (_ASM_STAT_IN_PROGR E SS)</td></tr>
<tr><td></td><td></td><td>5</td><td colspan="2">Fatal Error</td><td>0 = No
1 = Yes</td></tr>
<tr><td></td><td></td><td>4</td><td colspan="2">NMR OKLine Quality</td><td>0 = No (poor line quality)
1 = Yes (good line quality)</td></tr>
<tr><td></td><td></td><td>3</td><td colspan="2">Reserved</td><td>Reserved</td></tr>
<tr><td></td><td></td><td>2</td><td colspan="2">LOSWLoss of Sync Word</td><td>0 = No
1 = Yes</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">Reserved</td><td>Reserved</td></tr>
<tr><td></td><td></td><td>0</td><td colspan="2">LOSLoss of Signal</td><td>0 = No
1 = Yes</td></tr>
</table>

<table>
<tr><td>2</td><td>STATUS_2</td><td colspan="3">This byte contains ATM Operation and Maintenance (OAM) Parameters.</td></tr>
<tr><td rowspan="6"></td><td rowspan="6"></td><td colspan="3">STATUS_2: OAM Bit Definition</td></tr>
<tr><td>Status_2 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7-3</td><td>Reserved</td><td>Reserved.</td></tr>
<tr><td>2</td><td>nlcd : Near-End Loss of Cell Delineation failure.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>1</td><td>ncld : Near-end Loss of Cell Delineation defect.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>0</td><td>nhec : Near-end Header Error Control anomaly.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>3</td><td>STATUS_3</td><td colspan="3">See STATUS_3: Startup Failure Status Bit Definition for a list of the Startup Failure Status bit definitions.</td></tr>
<tr><td rowspan="6"></td><td rowspan="6"></td><td colspan="3">STATUS_3: Startup Failure Status Bit Definition</td></tr>
<tr><td>Status_3 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7</td><td>Activation Time-Out.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>6</td><td>Failed 3 (or n) consecutive startup attempts. N is an API command.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>5-4</td><td>Reserved.</td><td>Reserved.</td></tr>
<tr><td>3-0</td><td>Activation FailureResult will be latched until next successful or failed startup attempt.</td><td>0 = None
1 = Bad NMR
2 = Unable to Frequency Lock
3 = Failed Pre-Activation Startup
4 = Unable to detect Sync Word
5 = Failed Pair ID</td></tr>
</table>

<table>
<tr><td rowspan="10">4</td><td rowspan="10">STATUS_4</td><td colspan="3">See STATUS_4: DSL Framer Status Bit Definitions for a list of DSL Framer Status bit definitions.</td></tr>
<tr><td colspan="3">STATUS_4: DSL Framer Status Bit Definitions</td></tr>
<tr><td>Status_4 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7-6</td><td>DSL Sync State.</td><td>00 = Out-of-Sync
01 = Acquiring Sync
10 = In-Sync
11 = Losing Sync</td></tr>
<tr><td>5</td><td>Tip/Ring Reversal</td><td>0 = No
1 = Yes</td></tr>
<tr><td>4</td><td>Receive FIFO Error.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>3</td><td>Transmit FIFO Error.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>2</td><td>Transmit Stuff Error.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>1</td><td>DPLL Erroronly valid in DPLL Closed Loop mode.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>0</td><td>DPLL Lockedonly valid in DPLL Closed Loop mode.</td><td>0 = Not locked
1 = Locked, DPLL Stable</td></tr>
<tr><td rowspan="11">5</td><td rowspan="11">STATUS_5</td><td colspan="3">See STATUS_5: ATM PHY Status Bit Definitions for a list of ATM PHY status bit definitions.</td></tr>
<tr><td colspan="3">STATUS_5: ATM PHY Status Bit Definitions</td></tr>
<tr><td>Status_5 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7</td><td>Parity error</td><td>0 = No
1 = Yes</td></tr>
<tr><td>6</td><td>SOCStart of Cell error</td><td>Reserved</td></tr>
<tr><td>5</td><td>Transmit FIFO overflow error</td><td>0 = No
1 = Yes</td></tr>
<tr><td>4</td><td>Receive FIFO overflow error</td><td>0 = No
1 = Yes</td></tr>
<tr><td>3</td><td>Cell Sent</td><td>0 = No
1 = Yes</td></tr>
<tr><td>2</td><td>Bus Conflict error</td><td>0 = No
1 = Yes</td></tr>
<tr><td>1</td><td>Reserved</td><td>0 = No
1 = Yes</td></tr>
<tr><td>0</td><td>LOCD Loss of cell delineation.</td><td>0 = No
1 = Yes</td></tr>
</table>

<table>
<tr><td>6</td><td>STATUS_6</td><td colspan="3">DSL Framer status bit definitions</td></tr>
<tr><td></td><td></td><td colspan="3">STATUS_6: DSL Framer status bit definitions</td></tr>
<tr><td rowspan="4"></td><td rowspan="4"></td><td>Status_8 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7–2</td><td>Reserved.</td><td>Reserved</td></tr>
<tr><td>1</td><td>Invalid TNBCLK Detected</td><td>0 = No
1 = Yes</td></tr>
<tr><td>0</td><td>Invalid TPCLK Detected</td><td>0 = No
1 = Yes</td></tr>
<tr><td>7</td><td>STATUS_7</td><td colspan="3">Reserved.</td></tr>
<tr><td rowspan="10">8</td><td rowspan="10">STATUS_8</td><td colspan="3">Unsolicited Interrupt Bit Definitions. See also _DSL_INTR_HOST_MASK (opcode 0x50)</td></tr>
<tr><td colspan="3">STATUS_8: Unsolicited Interrupt Bit Definitions</td></tr>
<tr><td>Status_8 Bit</td><td>Description</td><td>Bit Definition</td></tr>
<tr><td>7-4</td><td>Reserved.</td><td>Reserved</td></tr>
<tr><td>3</td><td>Dying Gasp -- If HTU-R has a power failure, HTU-R sends power status indicator bits (active low) to HTU-C. HTU-C will report dying gasp unsolicited interrupt to the host</td><td>0 = No
1 = Yes</td></tr>
<tr><td>2</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1</td><td>Activation State Manager (ASM) Transitionthis bit is set when the ASM transitions into the Activate State (normal operation) or when the ASM transitions from the Pending State to the Deactivated State. The host reads the STATUS_1, Activation Status bits to determine the link-up or link-down status.
In summary, this bit only provides link-down to link-up transition and link-up to link-down transition.</td><td>0 = No
1 = Yes</td></tr>
<tr><td>0</td><td>Unsolicited API Commands this bit is set when an API command caused the Unsolicited Interrupt.
The host reads the API Outgoing mailbox to determine the API contents.</td><td>0 = No
1 = Yes</td></tr>
</table>