Orion - Dual Channel

SDSL, HDSL2, HDSL4, or SHDSL - ILD2

Overview

The Conexant Orion™ Digital Subscriber Line (DSL) chip sets provide low power, high density solutions for 2-wire DSL equipment. These chip sets are fully programmable and field upgradeable eliminating the risk of product obsolescence and accelerating the time-to-market for new network services. The Conexant Orion DSL chip sets are fully interoperable with multi-vendor DSL chip set solutions. This interoperability enables dynamic interworking of multiple vendor DSL solutions with the capability to interoperate with products that conform to ANSI and ETSI DSL standards.

Conexant's unique hardware platform supports multiple dual-channel applications including SDSL, HDSL2, and SHDSL, using population options for optimization.

The Orion DSL chip sets incorporate two DSL bit pumps plus framing into a three-chip solution comprised of a dual-channel digital signal processor (DSP) with built-in framer and two Analog Front Ends each with an Integrated Line Driver (ILD2).

The Orion chip sets interface directly with off-the-shelf T1/E1 transceivers eliminating the need for a separate DSL framer to combine and format the two DSL channels into a standard interface. Conexant's DSL Orion chip sets deliver two channels of full duplex transmission up to 2320 kb/s, depending on the application.

The high density Orion dual-channel DSL chip sets are ideal for CO applications, while single-channel versions with integrated framer are also available for CPE applications.

Features

- Dual-channel DSP with framer that fully integrates 2 separate DSL chips into a single device
- Two AFEs, each with an integrated differential line driver
- 2B1Q or PAM line codes
- Supports dual-channel symmetric data rates of 144 kb/s to 2320 kb/s (depending on the application)
- Supports IDSL with optional data interface rates of 64 kb/s, 128 kb/s, and 144 kb/s
- Offers physical layer interoperability with competitive solutions
- Glueless interface to popular microprocessors
- Transmission compliant with ETSI TS 101 135, ITU-T G.991.1, and ANSI TR-28 for single pair 2B1Q, ANSI T1.418 for HDSL2 and ITU-T G.991.2 for SHDSL
- Reference design compatible with Bellcore GR-1089, IEC 60950, UL 1950, ITU-T K.20 and K.21
- Built-in framer provides easy access to EOC and indicator bits (framing can be bypassed completely for dual-channel independent operation)
- Interfaces directly with off-the-shelf single-channel T1/E1 transceivers
- ATM UTOPIA Level 1 and 2 interface
- A single oscillator and hybrid topology supports all speeds
- +2.5V, +3.3V, and +5V power supplies

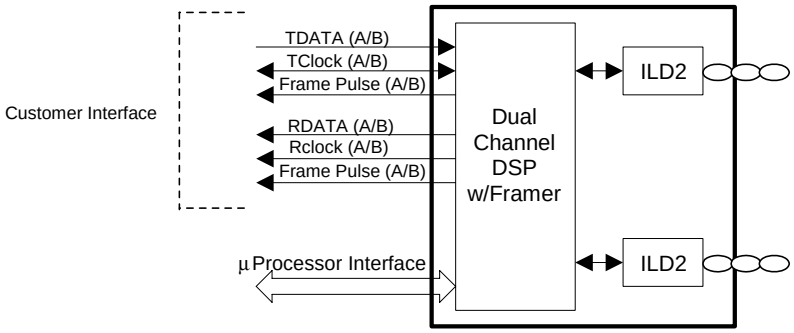


Figure 1: Block Diagram of Orion DSP with Two Single-Channel ILD2s

Introduction

The Conexant DSL chip sets support applications ranging from remote network access, digital pair gain, video conferencing, and cellular base station land-line connectivity, for T1/E1 services. Up to 36 voice circuits may be provisioned over a single copper pair.

Example Applications

- Compatibility with voice/data pair gain systems
- Cellular and microcellular systems
- T1/E1 and fractional T1/E1 DSL transceiver
- Wireless base station connectivity

Related Materials

To accelerate time-to-market, Conexant offers our customers a comprehensive Design Guide which includes details on planning, layout, testing, debugging, and expert tips and recommendations for building a successful DSL product. The Design Guide is distributed as part of a Design Package which includes firmware, transceiver schematics, sample code, transceiver layout Gerber files, and Bill of Materials.

For rapid prototyping, Quick Kits are available. These Quick Kits contain all transceiver design BOM components in kit form so there's no component lead time delay.

The SGDS™ development system, an easy-to-use evaluation and development platform designed to support all Conexant xDSL transceiver solutions, is also available for early product development.

The SGDS also provides an interface to the Conexant Microsoft® Windows® - based Host Interface Program (WHIP). When the SGDS is teamed with WHIP, product evaluation, testing and debugging is achieved with the click of a mouse.

Conexant Transceiver System Overview

- The Conexant Orion DSL chip sets consist of a dual-channel DSP with an on-chip framer, and two single-channel AFEs (with ILD2).
- The single-channel ILD2s filter and digitize the signal received on the telephone line and for the transmit side, generate analog signals from the digital data and filter the analog signals to create the 2B1Q or PAM transmit signal (depending on the line code).
- The Conexant Windows-based Host Interface Program (WHIP) is offered as part of the Conexant transceiver system development package for SDSL 2B1Q, HDSL2, and SHDSL applications. WHIP allows you to test and debug your product design with the click of a mouse. This graphical interface allows you to send commands, perform trace and debug procedures, and initiate a startup on both the CO and CP units. WHIP offers complete flexibility and modularity - you can rearrange windows and toolbars to suit your preferences and design requirements.

Architecture

The interface between the Host and the transceiver consists of the following:

- Transmission Interface (data, clock and synchronization signals)
- Control Interface (microprocessor compatible)
- Diagnostic Interface
- Power Interface
- Loop Interface

System timing is derived from a free running oscillator in the transceiver of the central office (CO). At the customer premises end (CPE), the CPE derives a clock from the received line signal and provides this clock to the CPE transmitter.

The dual-channel chip set also supports Network Timing Recovery (NTR) at the CO end. With this feature enabled, the CO unit will accept a clock at 8 kHz (± 100 ppm) as an input and the STU-R will output a clock that is phase locked to the CO clock. The NTR clock should have a duty cycle of 45-55%. Note that this feature is only available with an UTOPIA interface.

The DSL transceiver supports both T1 and E1 rates, and fractional rates.

Transceiver States

The following is a list of the possible states that the DSL transceiver can be in:

- IDLE mode, where the transceiver is not attempting to start up, pass data, or perform tests
- TEST mode, where the transceiver is either in local analog loopback or local digital loopback and is not passing user data
- STARTUP mode (SDSL only), where the transceiver is attempting a startup of the DSL connection, prior to entering DATA mode
- HANDSHAKE mode (HDSL2 and SHDSL), where a link is established between the CO unit and the CPE unit
- TRAINING mode (HDSL2 and SHDSL), where the transceiver is attempting a startup, prior to entering DATA mode
- DATA mode, where the transceiver has started up and trained and is capable of passing user data

Software Interface

A microprocessor interface that uses simple read/write drivers provides direct access to the Conexant chip set - eliminating the need for complicated register maps and advanced programming. These drivers allow the Host to select rates, adjust transmit power, read signal quality, and perform a variety of other tasks which include reporting the current operational status of the transceiver.

To configure and control the transceiver, Conexant provides hardware-dependent driver examples and Conexant supplied transceiver software modules (TSMs). The TSMs have the ability to allow a single CPU in the Host to control multiple transceivers. This could be a potential cost savings for arrangements where it might be advantageous to put multiple transceivers on one card, such as at the CO.

NOTE:

You will not need a register map of the DSP, as this information is not required to successfully design and implement an STU. As discussed previously, access to the DSP is provided through hardware-dependent I/O routines and Conexant provided TSMs.

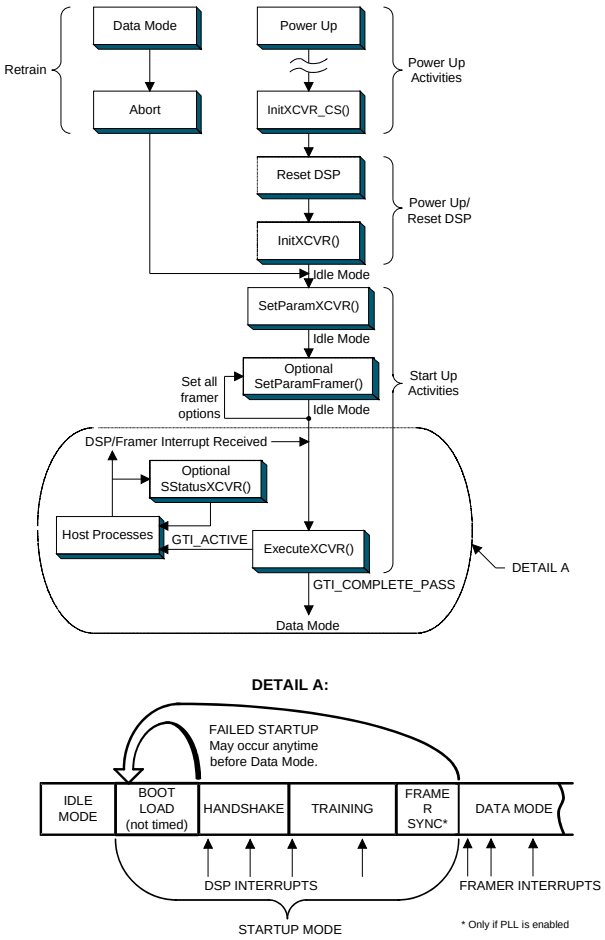


Figure 2: Typical Transceiver Power Up/Start Up Sequence

Transceiver Start Up Sequence

Figure 2 describes a typical sequence from power up to DATA mode for a transceiver. After power is applied to both the Host and the transceiver, the Host calls the `InitXCVR_CS()` and `InitXCVR()` routines to initialize transceiver variables and to initialize the DSP/Framer.

Next, the Host calls the `SetParamXCVR()` routine to set up the parameters that are appropriate for start up of the transceiver.

The `SetParamFramer()` routine is called by the Host to initialize framer options.

After setting up the transceiver parameters, the Host calls the `ExecuteXCVR()` routine to execute the command that was set up using the `SetParamXCVR()` routine. With a successful completion of the `ExecuteXCVR()` routine, the transceiver will now be in DATA mode.

The `SStatusXCVR()` routine is used to track performance and to obtain information from the transceiver about what state the transceiver is in (i.e., monitor start-up, check signal quality, etc.).

Setting Up the Command Parameters [SetParamXCVR()]

The routine `SetParamXCVR()` processes the parameter array structure that will be executed when the `ExecuteXCVR()` routine is called.

The parameter structure will be similar to the following start-up *example*:

```
struct PARAM_XCVR_ARRAY Items;
Items.length = GTI_NUM_OF_CMD_PARAMETERS
Items.item[GTI_ACTION_ITEM]=GTI_STARTUP_REQ;
Items.item[GTI_MODE_ITEM]=GTI_CO;
Items.item[GTI_POWER_SCALE_ITEM]=GTI_DEFAULT_SCALE;
Items.item[GTI_FRAMER_TYPE_ITEM]= GTI_UTOPIA_L2;
                                .
                                .
                                .
```

Table 1 describes the example arguments to the `SetParamXCVR()` routine when performing start-up. This is only a sample subset of possible parameters, provided to illustrate how easy it is to work with the Conexant chip sets.

Table 1: Example SetParamXCVR() Structure

Parameter	Function
GTI_ACTION_ITEM	The action GTI_STARTUP_REQ begins start-up, which, upon successful completion, results in the transceiver changing into DATA mode.
GTI_MODE_ITEM	Mode describes which transceiver the Host is talking to, the CO or CP.
GTI_POWER_SCALE_ITEM	Allows the transmit power to be set in small increments.
GTI_FRAMER_TYPE_ITEM	The framing modes are interface specific. Possible arguments for framing modes, depending on the customer interface, include: No Framing, UTOPIA Level 1, UTOPIA Level 2, T1, E1, and nxDS0 (with the ability to choose continuous DS0 blocks).

Checking the Transceiver Status [SStatusXCVR()]

The `SStatusXCVR()` routine can be executed when in DATA mode, utilizing minimal processing power. To further illustrate the ease of programming Conexant chip sets, Table 2 supplies a few examples of `SStatusXCVR()`.

Table 2: Example SStatusXCVR() Parameters

Parameter	Function
GTI_XMIT_POWER	This action returns the transmitted power.
GTI_START_PROGRESS	The current detailed start-up state of the transceiver is returned.
GTI_BERT_ERROR	The number of bit errors detected during the 511 BERT test is returned.
GTI_RECEIVER_GAIN	Total receiver gain setting can be calculated using the return values from this action.

System Power Requirements

The 160 PBGA Dual-channel DSP/Framer chip requires +2.5V (±5%) and +3.3V (±5%), and the two ILD2 chips require +3.3V (±5%) as well as +5V (±5%). Power requirements, including transceiver power consumption, have a tolerance of ±5%.

The transceiver obtains its power from the power feed in the Host through the power interface. Table 3, Table 4, and Table 5 provide power requirements for the 160 PBGA Dual-channel DSP.

Table 3: Typical SDSL 2B1Q System Power Consumption Per Channel (DSP/Framer in a 160 PBGA)

Line Rate (Kb/s)	Drain Current (mA)			Power/Port (mW)
	2.5VD DSP Core	3.3VD DSP & ILD2	5VA ILD2	
144	40	45	85	674
272	55	45	85	711
400	60	50	90	765
528	70	55	90	807
784	80	55	90	832
1040	95	55	90	869
1168	105	60	90	911
1552	135	65	95	1027
2064	145	70	95	1069
2320	160	70	95	1106

NOTE:

1. *Power per channel based on dual-channel operation*

2. *Based on customer schematic: G-02-2302-1006C-02 using 1:2 transformer*

Add 30 mA at 5VA for unified designs based on SHDSL population option G-02-2302-1006C-03 using 1:4 transformer or HDSL2 population option G-02-2302-1006C-03 using 1:5.4 transformer

3. *Transmit power: 13.5 dbm (nominal at all rates)*

4. *Measured during activation and data mode*

Table 4: Typical HDSL2 System Power Consumption Per Port (DSP/Framer in a 160 PBGA)

Line Rate (Kb/s)	Drain Current (mA)			Power/Port (mW)
	2.5VD DSP Core	3.3VD DSP & ILD2	5VA ILD2	
T1 (1.552)	170	65	150	1390

NOTE:

1. *Power per channel based on dual-channel operation*

2. *Estimates based on Revision C1 of the DSP/ Framer operating at 2.5V*

3. *Based on customer schematic: G-02-2302-1007C-01 using 1:5.4 transformer.*

4. *Transmit power: 16.8 dbm (nominal).*

Table 5: Typical SHDSL System Power Consumption Per Channel (DSP/Framer in a 160 PBGA)

Line Rate (Kb/s)	Drain Current (mA)			Power/Port (mW)
	2.5VD DSP Core	3.3VD DSP & ILD2	5VA ILD2	
144	40	45	125	874
200	45	45	125	886
208	45	45	125	886
272	55	45	125	911
392	60	50	125	940
400	60	50	125	940
528	70	50	125	965
776	80	50	125	990
784	80	50	125	990
1040	95	50	125	1028
1168	105	50	125	1053
1552	135	55	125	1144
2056	145	55	125	1169
2064	145	55	125	1169
2312	160	55	125	1207
2320	160	55	125	1207

NOTE:

1. *Power per channel based on dual-channel operation.*

2. *Estimates based on Revision C1 of the DSP/ Framer operating at 2.5V.*

3. *Based on customer schematic: G-02-2302-1007C-03 using 1:4 transformer.*

4. *Transmit power: 13.5 dbm (nominal).*

Table 6: Maximum Junction Temperature

T_J Maximum
125 °C

Transceiver Power Up Sequence

The recommended power supply sequencing for the Orion chip set is:

- The power on ramp of the 5 V supply must be delayed until the power on ramp of the 3.3 V supply is higher than 2.0V (Refer to Figure 3)

Note that this power sequencing is optimal for the ILD2 chip, especially in environments that power up the chip set below 0 °C. There are no requirements on the power supply sequence for the DSP/Framer.

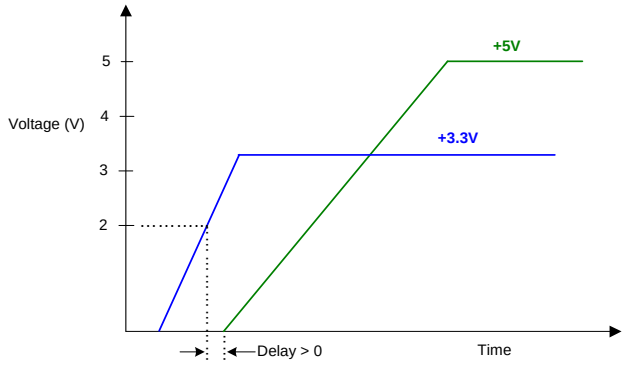


Figure 3: Voltage Ramp

Electrical Interface Specification

All processor interfaces, customer clock and data, and diagnostic interface inputs and outputs associated with the 144 DSP Core are compatible with 5V CMOS and TTL logic, as well as 3.3V CMOS logic. While the DSP is a 3.3V I/O and 2.5V core device, all the above inputs are designed to be 5V tolerant. The Control Interface supports multiplexed, non-multiplexed, and Motorola processor interface modes.

Performance

Conexant has rigorously tested the performance of the DSL chip sets, with the results detailed in Table 7, Table 8 and Table 9.

Table 7: SDSL 2B1Q Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise			
	24 AWG		26 AWG	
	kft	km	kft	km
144	25.4	7.7	21.0	6.4
272	23.6	7.2	19.5	5.9
400	22.4	6.8	17.3	5.2
528	21.3	6.5	16.1	4.9
784	19.1	5.8	15.2	4.6
1040	17.6	5.4	14.4	4.4
1168	15.9	4.8	13.8	4.2
1552	13.3	4.1	12.7	3.9
2064	11.8	3.6	11.1	3.4
2320	11.3	3.4	10.9	3.3

Table 8: HDSL2 Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise			
	24 AWG		26 AWG	
	kft	km	kft	km
T1 (1.552 kb/s)	18.0	5.5	13.5	4.1

Table 9: SHDSL Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise	
	26 AWG	
	kft	km
144	26.0	7.9
200	21.4	6.5
392	19.9	6.0
520	18.7	5.7
776	17.5	5.3
1032	16.6	5.1
1168	15.8	4.8
1544	14.0	4.2
2056	13.0	3.9
2312	12.5	3.8

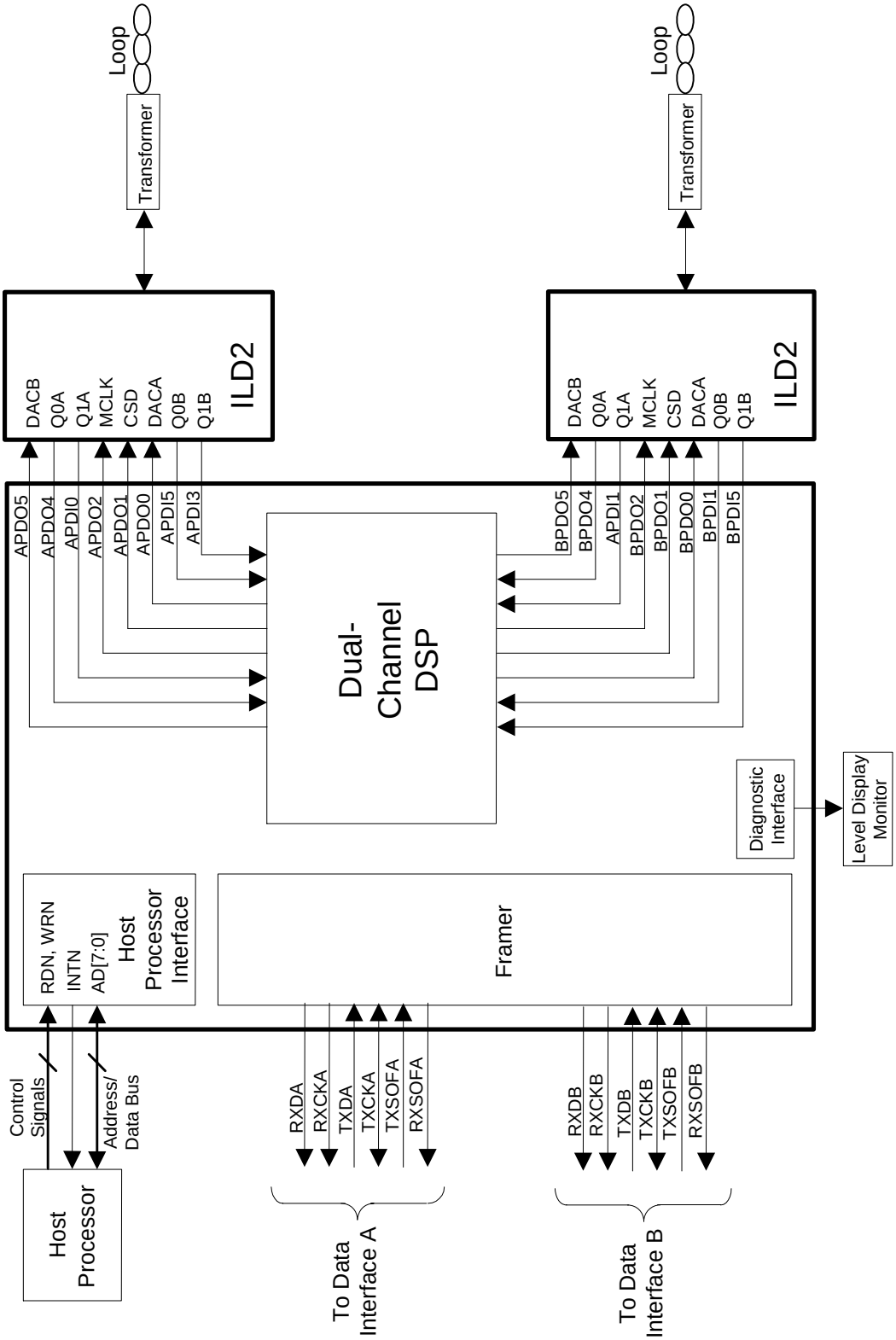


Figure 4: Orion Dual-Channel DSP with Integrated Line Driver Functional Diagram

Dual-Channel DSP/Framer Specifications

Figure 5, a layout view of the 160 PBGA package, depicts the pinout by ball number. A layout view is a top view of the 160 PBGA package as it would be mounted on a PCB. For layout purposes, the balls are shown as if looking through the chip. Table 10 lists the signal descriptions by pin number.

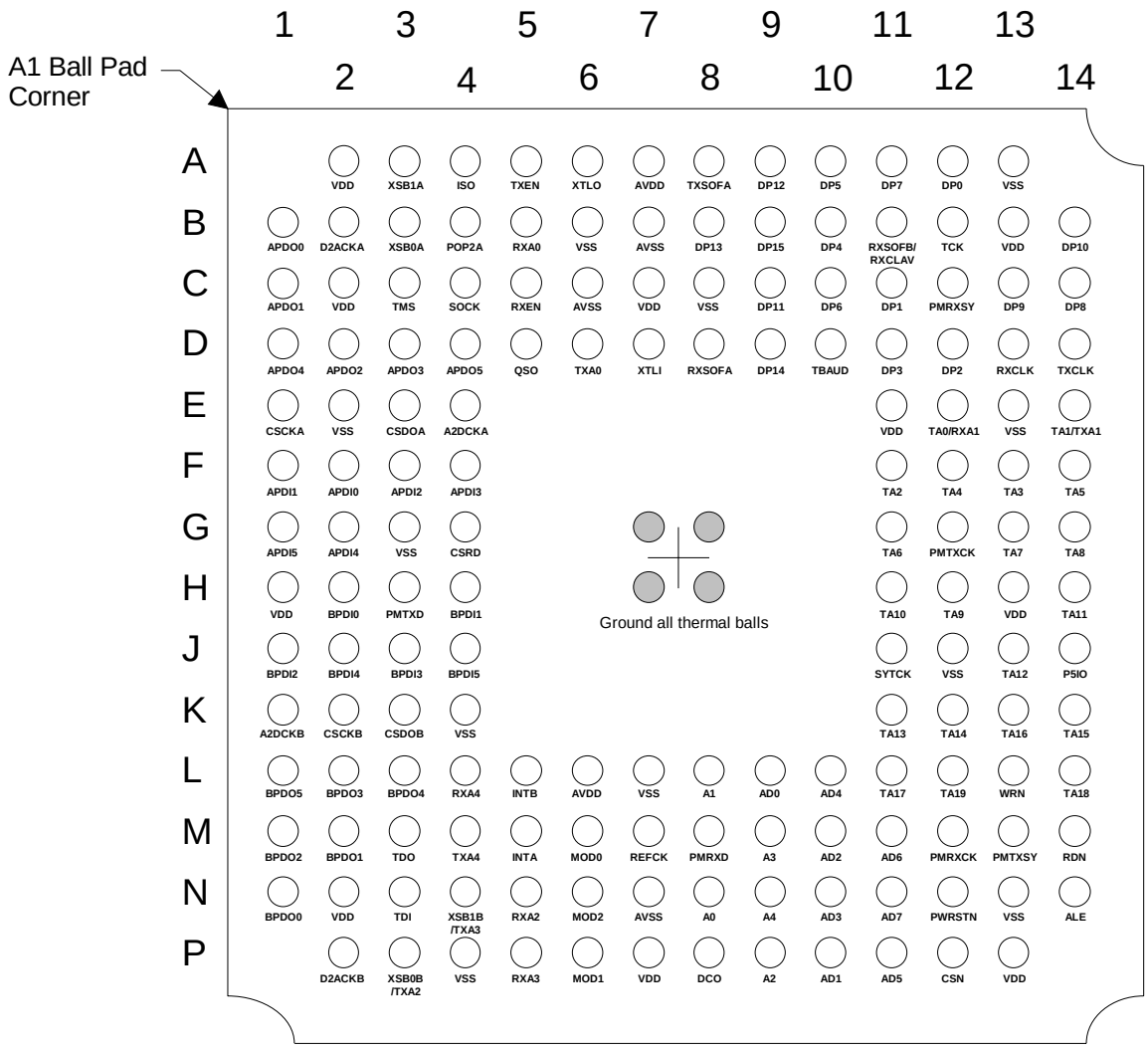


Figure 5: 160 PBGA Dual-Channel DSP/Framer Pin Diagram

Table 10: 160 PBGA Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)		Functional Description
A2	VDD	P		+3.3V supply.
A3	XSB1A	O		**External Strobe1 of DSP A.** One of two strobes from the DSP that are synchronized with the internal signal processing clock.
A4	ISO	O		**ISOA, ISOB - Level Display 1 Serial Data Output.** Serial data for level display 1. Data format is asynchronous with 12 bits of data and start and stop bits.
A5	TXSOFB/TXEN	SERIAL	I	**TXSOFB - Transmit start of Frame for channel B.**
		UTOPIA	I	**TXEN - ATM UTOPIA Level 1 and 2 Transmit Enable** (active low). The ATM layer device uses this pin to throttle the rate at the octet boundary.
A6	XTLO	O		**Not used for this application.** Per application schematic, do not connect.
A7	AVDD	P		**AVDD.** Digital +3.3V supply for VCO.
A8	TXSOFA/TXSOC	SERIAL	I	**TXSOFA - Transmit Start of frame for channel A.**
		UTOPIA	I	**TXSOC - ATM UTOPIA Level 1 and 2 Transmit Start of Cell** (active high). This bit is true on the first byte of the transmitted cell from the ATM to the PHY.
A9	DP12	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	O	RXDT4 - ATM UTOPIA Level 1 and 2 Receive Data. Byte-Wide True Data from the PHY to the ATM device.
A10	DP5	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	I	TXDT5 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
A11	DP7	SERIAL	I/O	Not used for this application. Internally configured as output.
		UTOPIA	I	TXDT7 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
A12	DP0	SERIAL	I	TXDA - Serial transmit data for channel A.
		UTOPIA	I	TXDT0 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
A13	VSS	—		Ground.
B1	APDO0	O		Data Out, Channel A. Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACA for channel A.
B2	D2ACKA	I/O		**Not used for this application.** Per application schematic, do not connect.
B3	XSB0A	O		**External Strobe0 of DSP A.** One of two strobes from the DSP that are synchronized with the internal signal processing clock.
B4	POP2A	O		**Not used for this application.** Per application schematic, do not connect.
B5	PIP/POP/RXA0	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**RXA0 - ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
B6	VSS	—		Ground.
B7	AVSS	—		AVSS. Ground pin for VCO. Connect to digital ground as per schematic.
B8	DP13	SERIAL	O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT5 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
B9	DP15	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT7 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
B10	DP4	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	I	TXDT4 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
B11	RXSOFB/RXCLAV	SERIAL	O	RXSOFB - Receive start of frame for channel B.
		UTOPIA	O	**RXCLAV - ATM UTOPIA Level 1 and 2 Receive Cell Available Signal.** Used by the PHY layer device to indicate that the receive buffer has a new cell.
B12	TCK	I		Boundary-scan clock. TCK is internally pulled up inside the DSP and therefore, requires no external termination.

Pin	Name(s)	Mode(s)		Functional Description
B13	VDD	P		+2.5V supply.
B14	DP10	SERIAL	O	**RXCKB - Receive clock for channel B.** This pin is the same as BRXCK for applications bypassing the on-chip framer.
		UTOPIA	O	**RXDT2 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
C1	APDO1	O		Control Output, Channel A. Control signal transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin CSD for channel A.
C2	VDD	P		+2.5V supply.
C3	TMS	I		Boundary-scan mode select.TMS is internally pulled up inside the DSP and therefore, requires no external termination.
C4	SOCK	O		**Serial Data Clock.** For ISO and QSO data outputs.
C5	PIP/POP/RXEN	SERIAL	I	**Not used for this application.** Terminate with a pull-up resistor.
		UTOPIA	I	**RXEN - Receive Enable** (active low). The ATM layer device uses this pin to throttle the rate at the octet boundary.
C6	AVSS	—		AVSS. Ground pin for VCO. Connect to digital ground as per schematic.
C7	VDD	P		+3.3V supply.
C8	VSS	—		Ground.
C9	DP11	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT3 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
C10	DP6	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	I	TXDT6 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
C11	DP1	SERIAL	I	TXDB - Serial transmit data for channel B.
		UTOPIA	I	TXDT1 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
C12	PMRXSY	—		Not used for this application. Per application schematic, do not connect.
C13	DP9	SERIAL	O	RXDB - Receive serial data for channel B.
		UTOPIA	O	**RXDT1 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
C14	DP8	SERIAL	O	RXDA - Receive serial data for channel A.
		UTOPIA	O	RXDT0 - ATM UTOPIA Level 1 and 2 Receive Data. Byte-Wide True Data from the PHY to the ATM device.
D1	APDO4	I		Data In, Channel A. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0A for channel A.
D2	APDO2	O		Master Clock to ILD2, Channel A. Input to AFE PLL which generates oversampling clocks. Connected to ILD2 pin MCLK for channel A.
D3	APDO3	O		**Not used for this application.** Per application schematic, do not connect.
D4	APDO5	O		Data Out, Channel A. Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACB for channel A.
D5	QSO	O		**QSOA, QSOB - Level Display 2 Serial Data Output.** Serial data for level display 2. Data format the same as ISO.
D6	PIP/POP/TXA0	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**TXA0 - ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
D7	XTLI	I		**Crystal Oscillator Input.** Oscillator input. It accepts a free running external clock at subrate of the internal VCO/PLL (see board recommendations).
D8	RXSOFA/RXSOC	SERIAL	O	**RXSOFA - Receive Start of frame for channel A**.
		UTOPIA	O	**RXSOC - ATM UTOPIA Level 1 and 2 Receive Start of Cell** (active high). This bit is true on the first byte of the transmitted cell from the PHY to the ATM.
D9	DP14	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT6 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.

Pin	Name(s)	Mode(s)		Functional Description
D10	TBAUD/TXCLAV	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	O	TXCLAV - ATM UTOPIA Level 1 and 2 Transmit Cell Available Signal. Used by the PHY layer device to indicate that there is space available for a new cell.
D11	DP3	SERIAL	I/O	Not used for this application. Per application schematic, do not connect.
		UTOPIA	I	TXDT3 - ATM UTOPIA Level 1 and 2 Transmit Data. Byte-Wide True Data from the ATM to the PHY device.
D12	DP2	SERIAL	O	TXCKB - Transmit clock for channel B. Framed = I; unframed = O.
		UTOPIA	I	**TXDT2 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
D13	RXCLK	SERIAL	O	RXCKA - Receive clock for channel A.
		UTOPIA	I	**RXCLK - ATM UTOPIA Level 1 and 2 Receive Clock.** Synchronizes all signal transfers from the ATM to the PHY device.
D14	TXCLK	SERIAL	I/O	**TXCKA - Transmit clock for channel A.** Framed = I; unframed = O.
		UTOPIA	I	**TXCLK - ATM UTOPIA Level 1 and 2 Transmit Clock.** Synchronizes all signal transfers from the ATM to the PHY device.
E1	CSCKA	O		**Not used for this application.** Per application schematic, do not connect.
E2	VSS	—		Ground.
E3	CSDOA	O		**Not used for this application.** Per application schematic, do not connect.
E4	A2DCKA	I/O		**Not used for this application.** Per application schematic, do not connect.
E11	VDD	P		+3.3V supply.
E12	TA0/RXA1	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**RXA1 - ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
E13	VSS	—		Ground.
E14	TA1/TXA1	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**TXA1 - ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
F1	APDI1	I		Data In, Channel B. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1A for channel B.
F2	APDI0	I		Data In, Channel A. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1A for channel A.
F3	APDI2	I		Not used for this application. Per application schematic, pulled low through a 1kΩ resistor to ground.
F4	APDI3	I		Data In, Channel A. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1B for channel A.
F11 F12 F13 F14	TA2 TA4 TA3 TA5	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
G1	APDI5	I		Data In, Channel A. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0B for channel A.
G2	APDI4	I		Not used for this application. Per application schematic, pulled low through a 1kΩ resistor to ground.
G3	VSS	—		Ground.
G4	CSRD	I		**Not used for this application.** Per application schematic, pulled low through a 1kΩ resistor to ground.
G7 G8	VSS	I		Ground.
G11	TA6	I/O		External TDM. Not used for this application. Per application schematic, do not connect.
G12	PMTXCK	—		Not used for this application. Per application schematic, do not connect.
G13 G14	TA7 TA8	I/O		External TDM. Not used for this application. Per application schematic, do not connect.
H1	VDD	P		+2.5V supply.
H2	BPDI0/APDI6	I		Not used for this application. Per application schematic, pulled low through a 1kΩ resistor to ground.
H3	PMTXD	—		Not used for this application. Per application schematic, do not connect.

Pin	Name(s)	Mode(s)		Functional Description
H4	BPDI1/APDI7	I		Data In, Channel B. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0B for channel B.
H7 H8	VSS	I		Ground.
H11 H12	TA10 TA9	I/O		External TDM. Not used for this application. Per application schematic, do not connect.
H13	VDD	P		2.5V supply.
H14	TA11	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
J1 J2 J3	BPDI2/APDI8 BPDI4/APDI10 BPDI3/APDI9	I		Not used for this application. Per application schematic, pulled low through a 1kΩ resistor to ground.
J4	BPDI5/APDI11	I		Data In, Channel B. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1B for channel B.
J11	SYTCK	O		Not used for this application. Per application schematic, do not connect.
J12	VSS	—		Ground.
J13	TA12	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
J14	P5IO	I		Programmable Input Pin.
K1	A2DCKB	I/O		**Not used for this application.** Per application schematic, do not connect.
K2 K3	CSCKB CSDOB	O		**Not used for this application.** Per application schematic, do not connect.
K4	VSS	—		Ground.
K11 K12 K13 K14	TA13 TA14 TA16 TA15	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
L1	BPDO5/APDO11	O		Data Out, Channel B. Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACB for channel B.
L2	BPDO3/APDO9	O		**Not used for this application.** Per application schematic, do not connect.
L3	BPDO4/APDO10	I		Data In, Channel B. Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0A for channel B.
L4	RXA4	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
L5	INTB	O		**Interrupt of DSP B.** Carries interrupts from internal DSP framer. The polarity of the interrupt level is programmable with default to inactive open-drain. Internally generated status can be enabled to activate the interrupt pin. Used during start-up for code downloads for core B, and EOC interrupts in data mode. INTA and INTB are both required. Both can be declared open-drain and tied together, if desired.
L6	AVDD	P		**AVDD.** Digital +3.3V supply for VCO.
L7	VSS	—		Ground.
L8	A1	I		**Address Bus**. Bits 4 through 0 (Pins N9, M9, P9, L8, and N8, respectively). Host Address bus in the non-multiplexed mode. A[4:3] are used to select between the two internal 8 byte address spaces.
L9 L10	AD0 AD4	I/O		Multiplexed Address and Data Bus. AD[7:0] are pins N11, M11, P11, L10, N10, M10, P10 and L9, respectively. AD[4:0] = Address inputs in multiplexed mode. See A[4:0] for usage.
L11 L12	TA17 TA19	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
L13	WRN	I		**Write Not.** Active low write pulse. This signal is used as a standard processor data write control signal.
L14	TA18	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
M1	BPDO2/APDO8	O		Master Clock to ILD2, Channel B. Input to AFE PLL which generates oversampling clocks. Connected to ILD2 pin MCLK for channel B.
M2	BPDO1/APDO7	O		Control Output, Channel B. Control signal transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin CSD for channel B.
M3	TDO	O		Boundary-scan data out.

Pin	Name(s)	Mode(s)		Functional Description
M4	TXA4	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**TXA4- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
M5	INTA	O		**Interrupt of DSP A.** Carries interrupts from internal DSP framer. The polarity of the interrupt level is programmable with default to inactive open-drain. Internally generated status can be enabled to activate the interrupt pin. Used during start-up for code downloads for core A. INTA and INTB are both required. Both can be declared open-drain and tied together, if desired.
M6	MOD0	I		**Host Bus Mode.** Bits 2 through 0 (Pins N6, P6 and M6, respectively). These input pins define the host bus control modes: 000 = Non-multiplexed processor mode 001 = Motorola mode where RDN is R/W and WRN is DSN 01X = reserved for testing 100 = Multiplexed processor mode 101 = reserved for testing.
M7	REFCK	I/O		**Reference Clock.** Used to pass network timing reference.
M8	PMRXD	—		Not used for this application. Per application schematic, do not connect.
M9	A3	I		**Address Bus**. Bits 4 through 0 (Pins N9, M9, P9, L8, and N8, respectively). Host Address bus in the non-multiplexed mode. A[4:3] are used to select between the two internal 8 byte address spaces.
M10 M11	AD2 AD6	I/O		Multiplexed Address and Data Bus. AD[7:0] are pins N11, M11, P11, L10, N10, M10, P10 and L9, respectively. AD[4:0] = Address inputs in multiplexed mode. See A[4:0] for usage.
M12 M13	PMRXCK PMTXSY	—		Not used for this application. Per application schematic, do not connect.
M14	RDN	I		**Read Not.** Active low read pulse. This signal enables data bus output buffers during read operations.
N1	BPDO0/APDO6	O		Data Out, Channel B. Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACA for channel B.
N2	VDD	P		+3.3V supply.
N3	TDI	I		Boundary-scan data in.TDI is internally pulled up inside the DSP and therefore, requires no external termination.
N4	XSB1B/TXA3	SERIAL	I/O	No Connect. For serial interface applications, this pin is used for debug purposes only.
		UTOPIA	I/O	**TXA3- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
N5	RXA2	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
N6	MOD2	I		**Host Bus Mode.** Bits 2 through 0 (Pins N6, P6 and M6, respectively). These input pins define the host bus control modes: 000 = Non-multiplexed processor mode 001 = Motorola mode where RDN is R/W and WRN is DSN 01X = reserved for testing 100 = Multiplexed processor mode 101 = reserved for testing.
N7	AVSS	—		**AVSS.** Ground pin for VCO. Connect to digital ground as per schematic.
N8 N9	A0 A4	I		**Address Bus**. Bits 4 through 0 (Pins N9, M9, P9, L8, and N8, respectively). Host Address bus in the non-multiplexed mode. A[4:3] are used to select between the two internal 8 byte address spaces.
N10 N11	AD3 AD7	I/O		Multiplexed Address and Data Bus. AD[7:0] are pins N11, M11, P11, L10, N10, M10, P10 and L9, respectively. AD[4:0] = Address inputs in multiplexed mode. See A[4:0] for usage.
N12	PWRSTN	I		**Power Reset Not.** Low active. DSP hardware reset that after deactivation still leaves the internal circuits in the software reset mode. In addition, all outputs are forced into high impedance mode when active. Also functions as **RSTN** for **JTAG** control.
N13	VSS	—		Ground.
N14	ALE	I		**Address Latch Enable.** In the processor mode, this pin is an input that indicates an active address cycle on the multiplexed bus.
P2	D2ACKB	O		**Not used for this application.** Per application schematic, do not connect.

Pin	Name(s)	Mode(s)		Functional Description
P3	XSB0B/TXA2	SERIAL	I/O	**No Connect.** For serial interface applications, this pin is used for debug purposes only.
		UTOPIA	I/O	**TXA2- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
P4	VSS	—		**Ground**.
P5	RXA3	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
P6	MOD1	I		**Host Bus Mode.** Bits 2 through 0 (Pins N6, P6 and M6, respectively). These input pins define the host bus control modes: 000 = Non-multiplexed processor mode 001 = Motorola mode where RDN is R/W and WRN is DSN 01X = reserved for testing 100 = Multiplexed processor mode 101 = reserved for testing.
P7	VDD	P		+2.5V supply.
P8	DCO	I/O		**DCO.** Pull up as per application schematic.
P9	A2	I		**Address Bus**. Bits 4 through 0 (Pins N9, M9, P9, L8, and N8, respectively). Host Address bus in the non-multiplexed mode. A[4:3] are used to select between the two internal 8 byte address spaces.
P10 P11	AD1 AD5	I/O		Multiplexed Address and Data Bus. AD[7:0] are pins N11, M11, P11, L10, N10, M10, P10 and L9, respectively. AD[4:0] = Address inputs in multiplexed mode. See A[4:0] for usage.
P12	CSN	I		**Chip Select.** Active low in µP mode.
P13	VDD	P		+2.5V supply.

Boundary-Scan Testing

Four pins are provided for compliance to IEEE Standard 1149.1 (JTAG) for boundary scan testing. These DSP pins are used to control and communicate with the boundary-scan logic. JTAG support is available only in Revision “C1” of the DSP/Framer. Table 11 provides a list of the four JTAG pins:

Table 11: Boundary-Scan Pins

160 PBGA DSP/Framer Revision “C1” Pin #	JTAG Description
C3	TMS - Test Mode Select
N3	TDI - Test Data Input
M3	TDO - Test Data Output
B12	TCK - Test Clock

Table 12: Dual-Channel DSP/Framer Electrical Characteristics

Parameters	Min	Nom	Max	Unit	Test Conditions/Comments
Absolute Maximum Ratings					
Power Supply, V_{DD} (3.3V)	—	—	3.6	V	
Power Supply, AV_{DD} (3.3V)	—	—	3.6	V	
Power Supply, V_{DD} (2.5V)	—	—	2.75	V	
Input Voltage	GND – 0.3	—	5.5	V	
Storage Temperature	–40	—	125	℃	
Junction Temperature	—	—	125	℃	
Recommended Operating Conditions					
Power Supply, V_{DD} (3.3V)	3.13	3.3	3.47	V	
Power Supply, AV_{DD} (3.3V)	2.75	3.3	3.47	V	
Power Supply, V_{DD} (2.5V)	2.38	2.5	2.63	V	
Input Voltage	GND – 0.3	3.3	5.5	V	
Operating Temperature	–40	25	85	℃	
Digital Specifications					
I/O Levels	TTL and/or CMOS compatible				
Digital Inputs					
Input Low Voltage, V_{IL}	–0.3	0	0.8	V	For all inputs except XTLI. For XTLI, the maximum V_{IL} is VDD/2.
Input High Voltage, V_{IH}	2.0	3.3	5.25	V	
Digital Outputs					
Output Low Voltage, V_{OL}	—	0	0.4	V	Current sink, I_{OL}, ≤ 6 mA for all non-UTOPIA pins Current sink, I_{OL}, ≤ 10 mA for all UTOPIA pins
Output High Voltage, V_{OH}	2.4	3.3	—	V	Current load, I_{OH}, ≤ 6 mA for all non-UTOPIA pins Current load, I_{OH}, ≤ 10 mA for all UTOPIA pins
DC Specifications					
Input Leakage Current, I_{LI}	—	—	10	µA	Input voltage, V_I, between 0 volts and V_{DD}
High-Z Leakage Current, I_{LO}	—	—	10	µA	Output voltage, V_O, between 0 volts and V_{DD}
Input Capacitance, C_{IN} (f_c = 1 MHz)	—	6	—	pF	
I/O Capacitance, C_{IO} (f_c = 1 MHz)	—	10	—	pF	

Note: All of the following pins are 5V tolerant:

All Input (I) signal pins except XTLI

All Input/Output (I/O) signal pins

No Output (O) signal pins except INTA and INTB

Table 13: Clock Specifications for XTLI Pin

Timing Parameters			Voltage	
Duty Cycle	**Rise Time Maximum (nsec)**	**Fall Time Maximum (nsec)**	**Overshoot Maximum**	**Undershoot Maximum**
40 - 60%	4	4	3.3V + 5%	100 mV below ground

Note the following layout guidelines:

1. We recommend not more than 4 DSPs per clock source.
2. The clock source distribution network should be routed in a star pattern ensuring equal distances to all DSPs.
3. Place a series termination resistor as close to the clock source as possible.
4. Refer to the “Critical Clock and Signal Layout Guidelines” section in Chapter 3 of the Design Guide for further information.

Customer Data Interface

The customer data interface includes data signals, control signals, and address signals. The Conexant 160 PBGA DSP has an on-chip programmable framer for handling multiple TC layer framing formats. The supported, software selectable, framing formats include Serial Mode and Asynchronous Transfer Mode (ATM) UTOPIA Level 1 and Level 2. Please note only one UTOPIA Level 1 interface is supported per dual channel DSP/Framer. Table 14 lists corresponding pins for both Serial and UTOPIA Modes.

Table 14: 160 PBGA DSP Data Interface Pin Usage

Pin Name	Pin Number	UTOPIA Mode		Serial Mode	
DP0	A12	I	TXDT0	I	TXDA
DP1	C11	I	TXDT1	I	TXDB
DP2	D12	I	TXDT2	I/O	TXCKB
DP3	D11	I	TXDT3	I/O	Not used
DP4	B10	I	TXDT4	I/O	Not used
DP5	A10	I	TXDT5	I/O	Not used
DP6	C10	I	TXDT6	I/O	Not used
DP7	A11	I	TXDT7	I/O	Not used
DP8	C14	O	RXDT0	O	RXDA
DP9	C13	O	RXDT1	O	RXDB
DP10	B14	O	RXDT2	O	RXCKB
DP11	C9	O	RXDT3	I/O	Not used
DP12	A9	O	RXDT4	I/O	Not used
DP13	B8	O	RXDT5	O	Not used
DP14	D9	O	RXDT6	I/O	Not used
DP15	B9	O	RXDT7	I/O	Not used
TXCLK	D14	I	TXCLK	I/O	TXCKA
TXSOFA/TXSOC	A8	I	TXSOC	I	TXSOFA
TBAUD/TXCLAV	D10	O	TXCLAV	I/O	Not used
RXCLK	D13	I	RXCLK	O	RXCKA
RXSOFA/RXSOC	D8	O	RXSOC	O	RXSOFA
RXSOFB/RXCLAV	B11	O	RXCLAV	O	RXSOFB
PIP/POP/TXA0	D6	I	TXA0*	I/O	Not used
TA1/TXA1	E14	I	TXA1*	I/O	Not used
XSB0B/TXA2	P3	I	TXA2*	I/O	Not used
XSB1B/TXA3	N4	I	TXA3*	I/O	Not used
TXA4	M4	I	TXA4*	I/O	Not used
PIP/POP/RXA0	B5	I	RXA0*	I/O	Not used
TA0/RXA1	E12	I	RXA1*	I/O	Not used
RXA2	N5	I	RXA2*	I/O	Not used
RXA3	P5	I	RXA3*	I/O	Not used
RXA4	L4	I	RXA4*	I/O	Not used
TXSOFB/TXEN	A5	I	TXEN	I	TXSOFB
PIP/POP/RXEN	C5	I	RXEN	I	Not used

* Not used for UTOPIA Level 1 applications.

ATM UTOPIA Level 1 and Level 2

Figure 6 and Figure 7 detail the interface for standard ATM UTOPIA Level 1 and Level 2. Dual-channel ATM over UTOPIA Level 2 or single-channel ATM over UTOPIA Level 1 is supported for SHDSL, SDSL 2B1Q, and HDSL2.

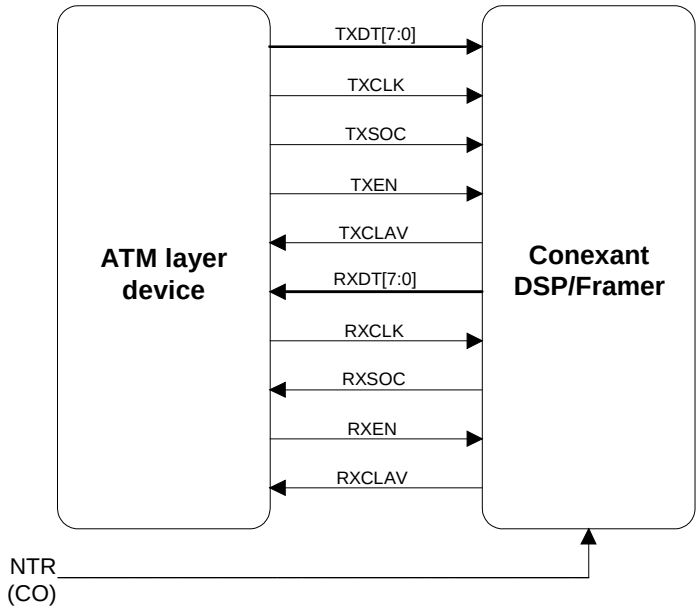
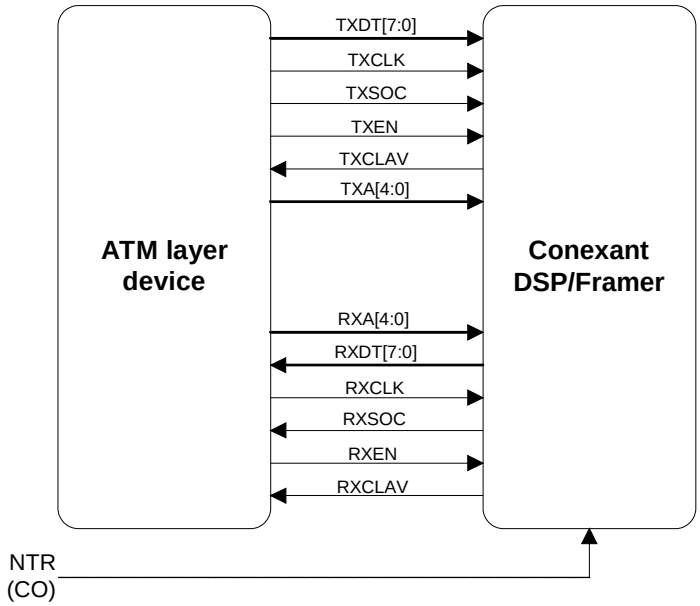


Figure 6: UTOPIA Level 1 Signals



NOTE: RXSOC, RXCLAV, and TXCLAV are tri-state active high signals and need appropriate pull-down terminations.

Figure 7: UTOPIA Level 2 Signals

Transmit, receive, and tri-state timing is shown in Figure 8, Figure 9, and Figure 10. Timing parameters are shown in Table 15.

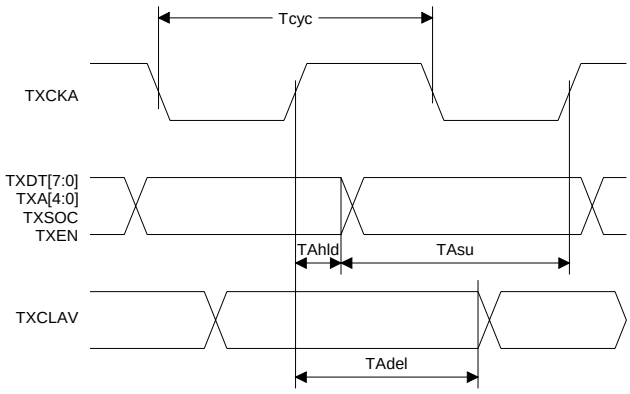


Figure 8: Transmit ATM Timing

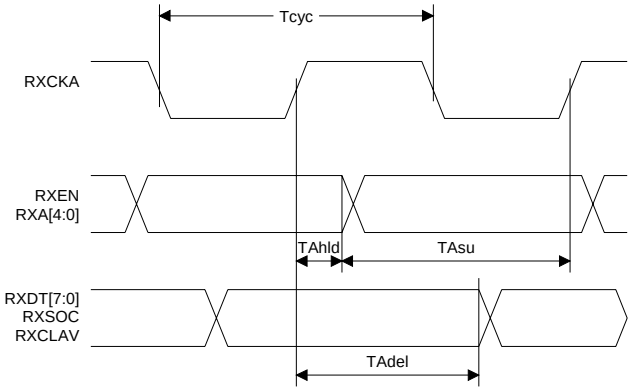


Figure 9: Receive ATM Timing

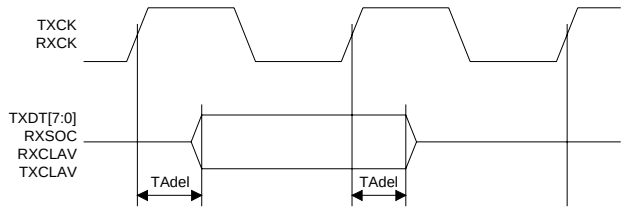


Figure 10: Tri-State ATM Timing

Table 15: ATM Timing Parameters

Specifi-cation	Description	Min	Max
Tcyc	Clock Period	40 ns	
TAsu	Input Setup to Clock Rising Edge	4 ns	
TAhld	Input Hold from Clock Rising Edge	1 ns	
TAdel	Output Delay from Clock Rising Edge		15 ns

Supported Serial Interfaces

The following serial interfaces are supported per application:

SHDSL: Dual or single-channel Slotted E1 and Slotted T1 Interfaces (refer to the SHDSL Design Guide, DO-300041-PS, for a detailed description).

HDSL2: Single-channel Fixed T1 Interface (refer to the HDSL2 Design Guide, DO-009651-PS, for a detailed description).

Table 16: Summary of Transceiver Serial Interface Leads

Name	Type CO/Framer	Type CO/Framer Bypass	Type CP/Framer	Type CP/Framer Bypass	Description
Transmission Interface					
TXD[A,B]	I	I	I	I	Transmit Data for channels A and B
TXCK[A,B]	I	O	I	O	Transmit Bit Clock for channels A and B (see **NOTE**)
RXD[A,B]	O	O	O	O	Receive Data for channels A and B
RXCK[A,B]	O	O	O	O	Receive Bit Clock for channels A and B (see **NOTE**)
TXSOF[A,B]	I	N/C	I	N/C	Transmit start of Frame for channels A and B
RXSOF[A,B]	O	N/C	O	N/C	Receive start of Frame for channels A and B

NOTE:

*Each **Type** field shows the directional flow for the CO/CP with Framer, or CO/CP without the integrated Framer (Bypass mode) from the view of the DSP/Framer.*
Figure 11 and Figure 12 depict the directions of the framed and unframed serial data/clock interfaces.

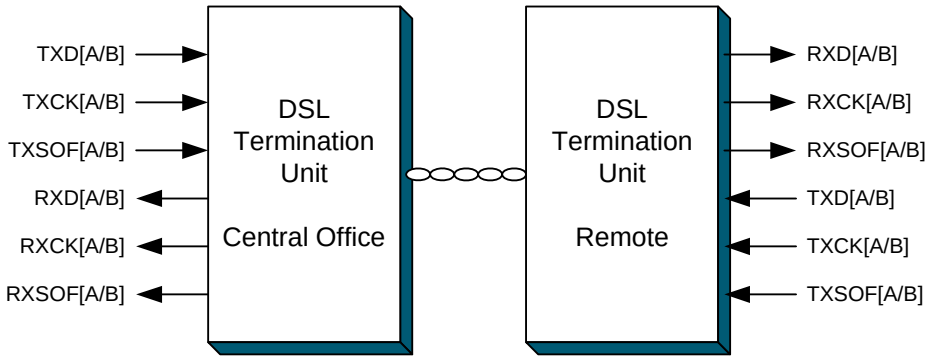


Figure 11: *Framed Serial Data/Clock Interface

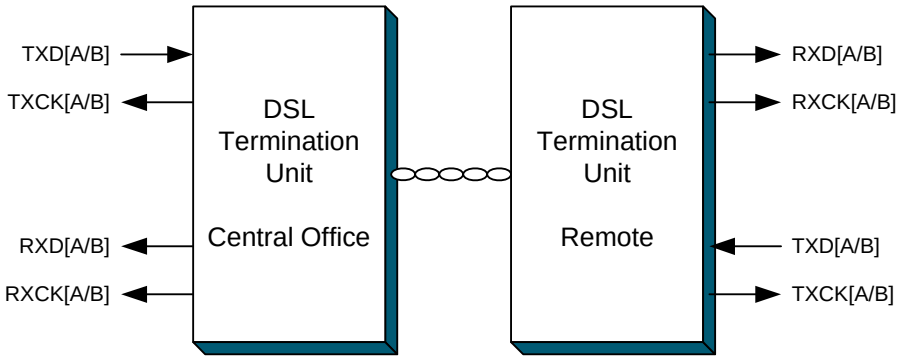
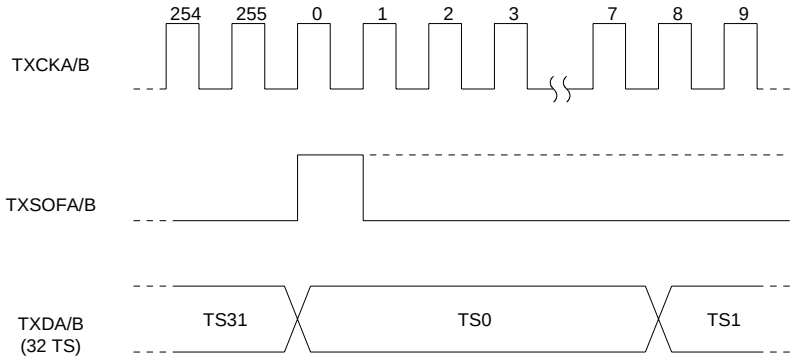


Figure 12: *Unframed (Framer Bypass Mode) Serial Data/Clock Interface.

* Note that TX and RX clocks must have the same frequency at both the CO and CPE.

The relationship between the data and the Start Of Frame signal (SOF) to the clock pulse is illustrated below. Figure 13 and Figure 14 depict E1, which has sync byte in time slot 0. Figure 15 and Figure 16 depict T1, which has an F-bit signifying the start of time slot 0. For unframed mode, the SOF is not applicable.



NOTE: The transmit start of frame pulse (TXSOFA/B) must be low for at least 8 clock cycles.

Figure 13: Transmit Slotted E1 Interface Timing

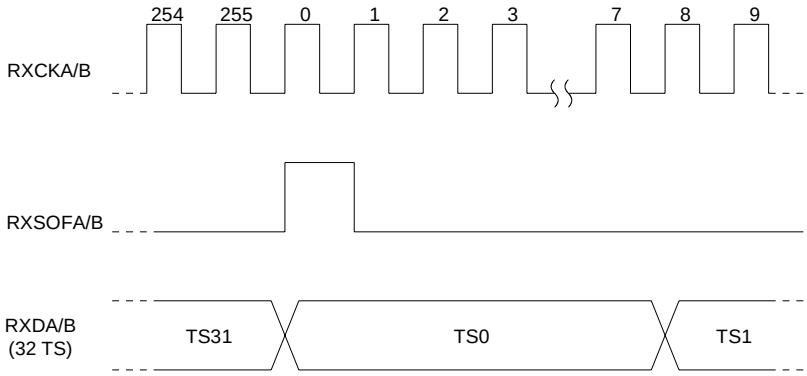
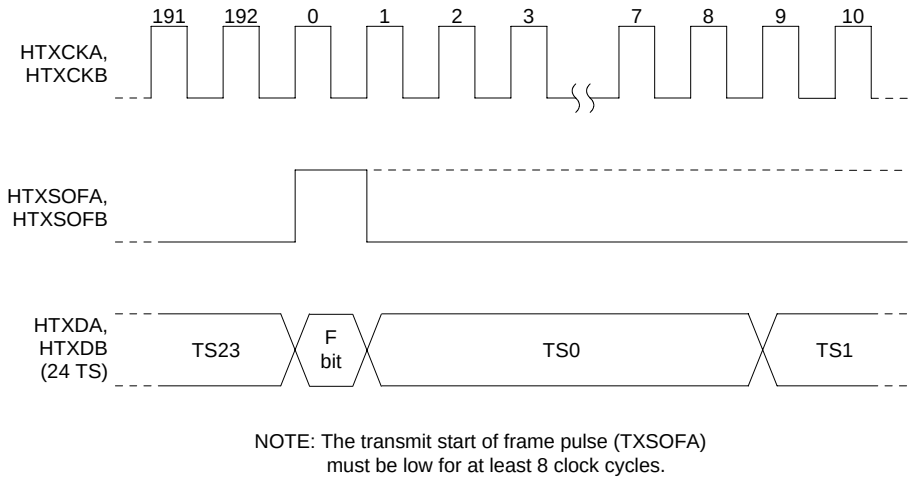


Figure 14: Receive Slotted E1 Interface Timing



NOTE: The transmit start of frame pulse (TXSOFA) must be low for at least 8 clock cycles.

Figure 15: T1 Interface Transmit Timing for HDSL2

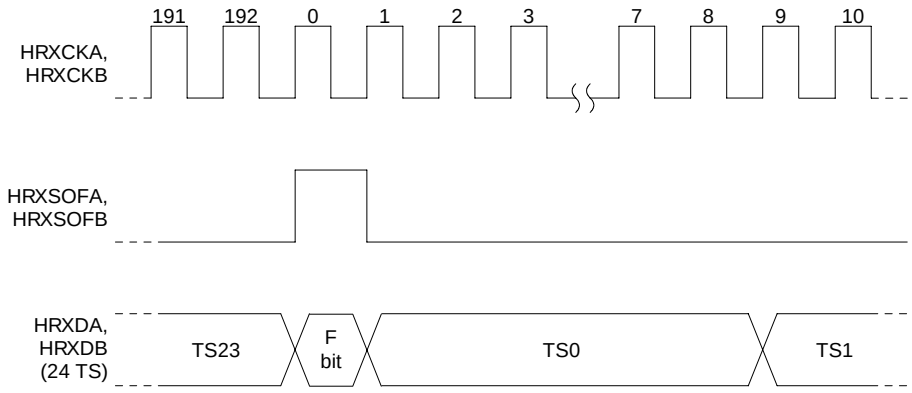


Figure 16: T1 Interface Receive Timing for HDSL2

Figure 17 and Figure 18 show serial transmit and receive timing. This timing applies to all products (SDSL, HDSL2, and SHDSL - ILD2).

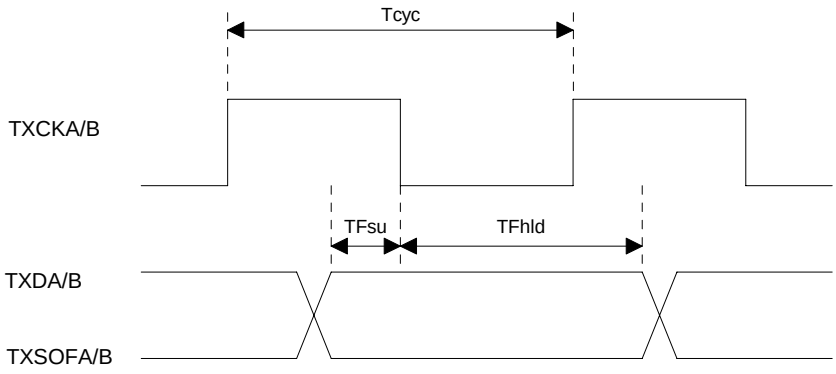


Figure 17: Serial Transmit Timing

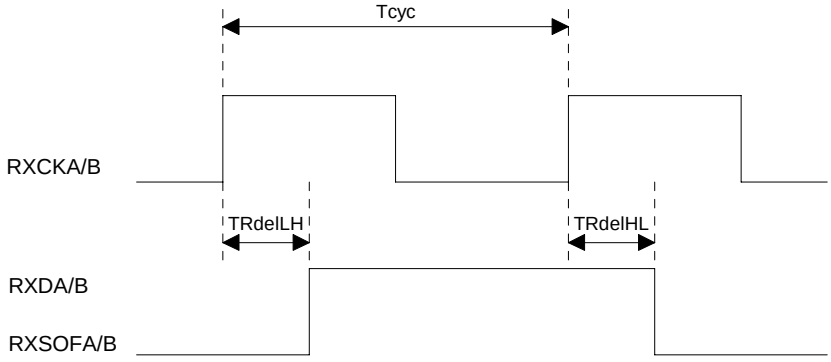


Figure 18: Serial Receive Timing

Table 17: Serial Timing Parameters

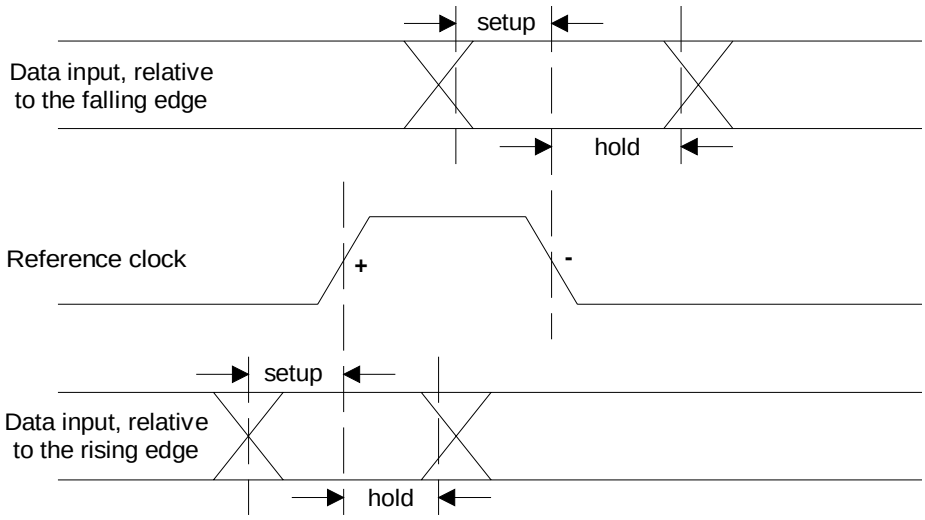
Specification	Description	Min	Max
Tcyc	Clock Period	50 ns	
TFsu	Input Setup to Clock Falling Edge	10 ns	
TFhld	Input Hold from Clock Falling Edge	5 ns	
TRdelLH	Output Delay From Low to High		20 ns
TRdelHL	Output Delay From High to Low		20 ns

Input Timing Parameters

Specifications are defined in terms of setup and hold times of the data inputs relative to a reference clock.

Table 18: Input Timing Parameters

Input Signal	Pin	Edge	Setup (nsec)	Hold (nsec)
TxDA TxDB	TXCKA (D14) TXCKB (D12)	+/-	10	5



This timing applies to ALL data inputs and their respective clocks

Figure 19: Input Timing Diagram

Output Timing Parameters

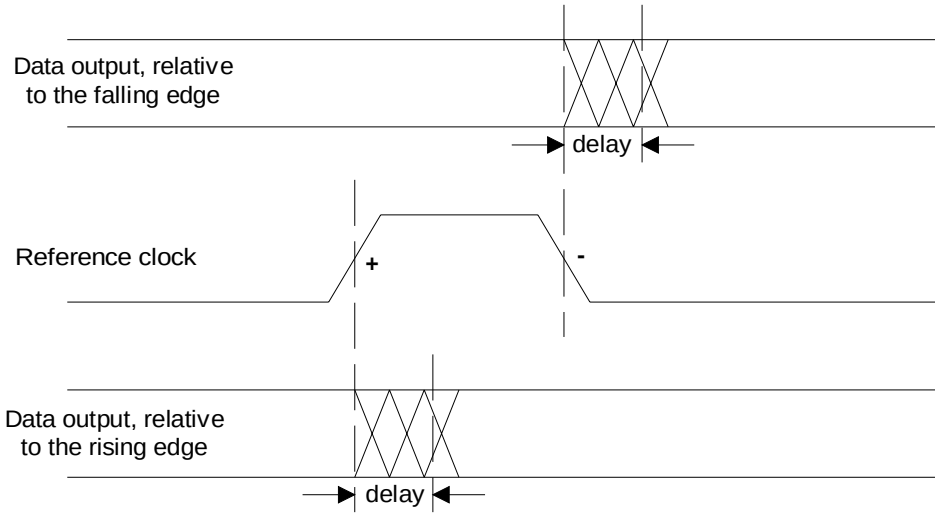
Specifications are defined in terms of propagation delay from a reference clock edge to the data output stable condition.

NOTE:

All loads are 35 pF, unless noted otherwise.
Add 1.5 nsec per 10 pF of additional loading.
Rise and fall times are 5 nsec.

Table 19: Output Timing Parameters

Output	Pin	Edge	Min (nsec)	Max (nsec)
All outputs to high-Z	PWRSTN (N12)	+		50
RxDA RxDB	RXCKA (D13) RXCKB (B14)	+/-		20
ISO/QSO	SOCK (C4)	+		10



This timing applies to ALL data outputs and their respective clocks

Figure 20: Output Timing Diagram

Host Processor Interfaces

Conexant chip sets easily interface with multiplexed (Intel style), generic non-multiplexed, and non-multiplexed Motorola style host processors. The MOD pins on the DSP must be set according to Table 20 for the type of processor interface required. These pins should be set (pulled high or low) using the resistor values shown in the Customer Schematics.

Table 20: MOD Settings

Processor	MOD2	MOD1	MOD0	RDN Function	WRN Function	ALE Use
Multiplexed	1	0	0	RDN	WRN	ALE
Motorola	0	0	1	RD/WRN	DSN	n/a (pulled low)
Other non-multiplexed	0	0	0	RDN	WRN	n/a (pulled low)

NOTE:

A value of 1 refers to pulled high and 0 refers to pulled low.

Table 21: Summary of Transceiver Host Interface Leads

Name	Type CO/Framer	Description
AD[0-7]	I/O	8 Bit Multiplexed Address/Data Bus
CSN	I	DSP Chip Select
ALE	I	Multiplexed Processor Address Latch Enable
WRN	I	Write Strobe
RDN	I	Read Strobe
PWRSTN	I	Power Reset Not
INTA, INTB	O	DSP/Framer Interrupts
MOD[2,1,0]	I	Host Bus Control Modes
A[0-4]	I	Non-multiplexed Address Bus

NOTE:

*Each **Type** field shows the directional flow for the CO/CP with Framer, or CO/CP without the integrated Framer (Bypass mode) from the view of the DSP/Framer.*
Figure 11 and Figure 12 depict the directions of the framed and unframed serial data/clock interfaces.

Multiplexed Bus Mode Timing Requirements and Characteristics

Table 22: Read Cycle Timing Characteristics

Parameter	Symbol	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVDV	35	Capacitive load on HAD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Read strobe active to data valid	tHRDNLDV	25	Capacitive load on HAD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Bus active after read	tHRDNHDX	10	

Table 23: Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Chip select setup time before read strobe	tHCSNLHRDNL	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Chip select hold time after read strobe	tHRDNHHCSNH	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Address setup time before latch strobe low	tHAVHALEL	10	
Address hold time after latch strobe low	tHALELHAX	5	
Address latch strobe width	tHALEHHALEL	10	
Address setup time before read strobe	tHAVHRDNL	10	
Read strobe inactive before next cycle	tHRDNLHHALEH	10	
Inter-access cycle time (not shown)	tHALEHHALEH	200	The minimum time between successive reads

Table 24: Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	tHALELHALEL	200	The minimum time between successive writes
Chip select setup time before write strobe low	tHCSNLHWRNL	10	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Write strobe width	tHWRNLHWRNH	20	
Chip select hold time after write strobe high	tHWRNHHCSNH	0	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Address setup time before latch strobe low	tHAVHALEL	10	
Address hold time after latch strobe low	tHALELHAX	5	
Data setup time before write strobe	tHDVHWRNH	10	
Data hold time after write strobe	tHWRNHHDX	2	
Address latch strobe width	tHALEHHALEL	10	
Address setup time before write strobe	tHAVHWRNL	0	
Write strobe inactive before next cycle	tHWRNHHALEH	10	

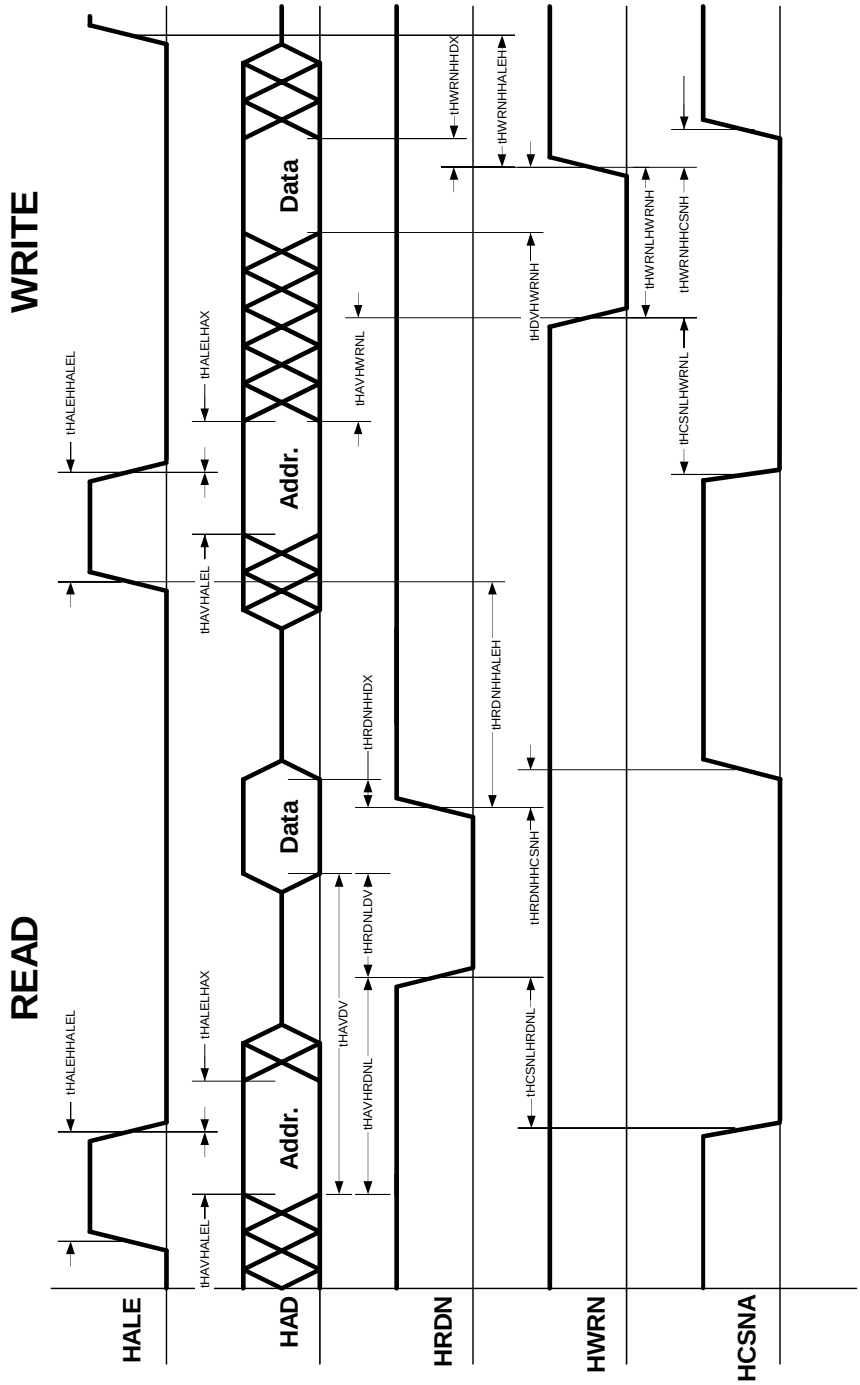


Figure 21: Multiplexed Bus Mode Timing Diagram

Non-multiplexed Bus Mode Timing Requirements and Characteristics

Table 25: Read Cycle Timing Characteristics

Parameter	Symbol	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVHDV	35	Capacitive load on HD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Read strobe active to data valid	tHRDNLHDV	25	Capacitive load on HD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Bus active after read	tHRDNHHDZ	10	

Table 26: Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Chip select active before read	tHCSNLHRDNL	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Chip select hold time after read	tHRDNHHCSNH	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Address setup time before read	tHAVHRDNL	5	
Address hold time after read	tHRDNHHAX	5	
Inter-access cycle time (not shown)	tHRDNLHRDNL	200	The minimum time between successive reads

Table 27: Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	tHWRNLHWRNL	200	The minimum time between successive writes
Chip select setup time before write strobe low	tHCSNLHWRNL	10	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Write strobe width	tHWRNLHWRNH	20	
Chip select hold time after write	tHWRNHHCSNH	0	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Address setup time before write	tHAVHWRNL	10	
Address hold time after write	tHWRNHHAX	5	
Data setup time before write	tHDVHWRNH	10	
Data hold time after write	tHWRNHHDX	2	

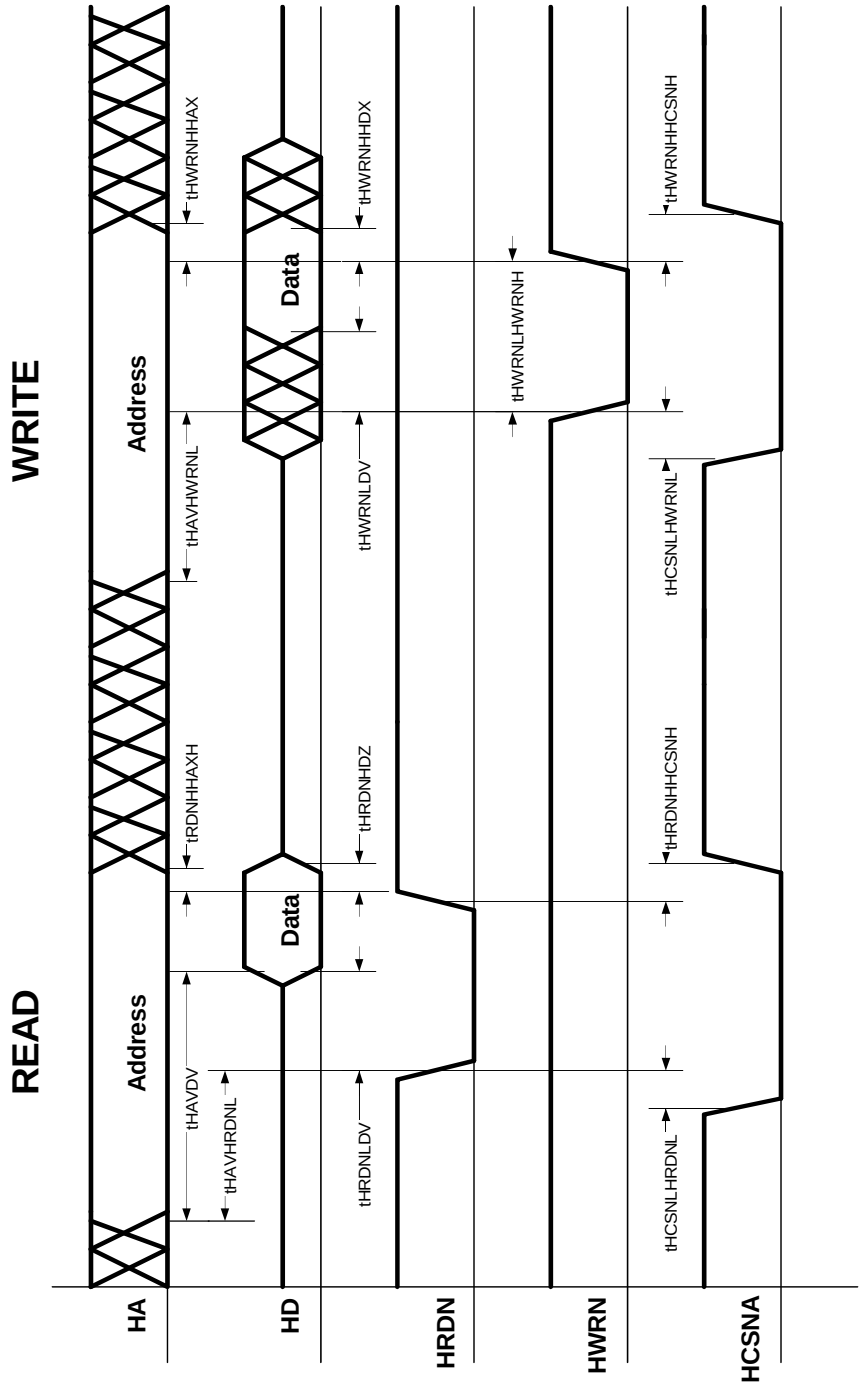


Figure 22: Non-multiplexed Bus Mode Timing Diagram

Motorola Bus Mode Timing Requirements and Characteristics

Table 28: Read Cycle Timing Characteristics

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVDV		20	
Data set (DSN) strobe active to data valid	tDSNLDV		10	
Bus active after data set strobe inactive	tDSNHHDX		6	

Table 29: Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	-	200		The minimum time between successive reads
Address setup time before chip select low	tHAVHCSNL	5		
R/Wn setup before chip select low	tHRWNHHCSNL	5		
R/Wn hold time after chip select inactive	tHCSNHHRWNL	0		
Address hold time after chip select inactive	tDSNHHAX	5		
Chip select setup time before data set strobe	tHCSNLDSNL	5		
Chip select hold time after data set strobe	tDSNHHCSNH	0		

Table 30: Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	-	200		The minimum time between successive writes
Address setup time before chip select low	tHAVHCSNL	5		
R/Wn setup before chip select low	tHRWNHHCSNL	5		
R/Wn hold time after chip select inactive	tHCSNHHRWNH	0		
Data setup time before data set strobe active	tDVDSNL	5		
Data set strobe width for write operation	tDSNLDSNH	5		
Address hold time after chip select inactive	tDSNHHAX	5		
Chip select setup time before data set strobe	tHCSNLDSNL	5		
Chip select hold time after data set strobe	tDSNHHCSNH	0		

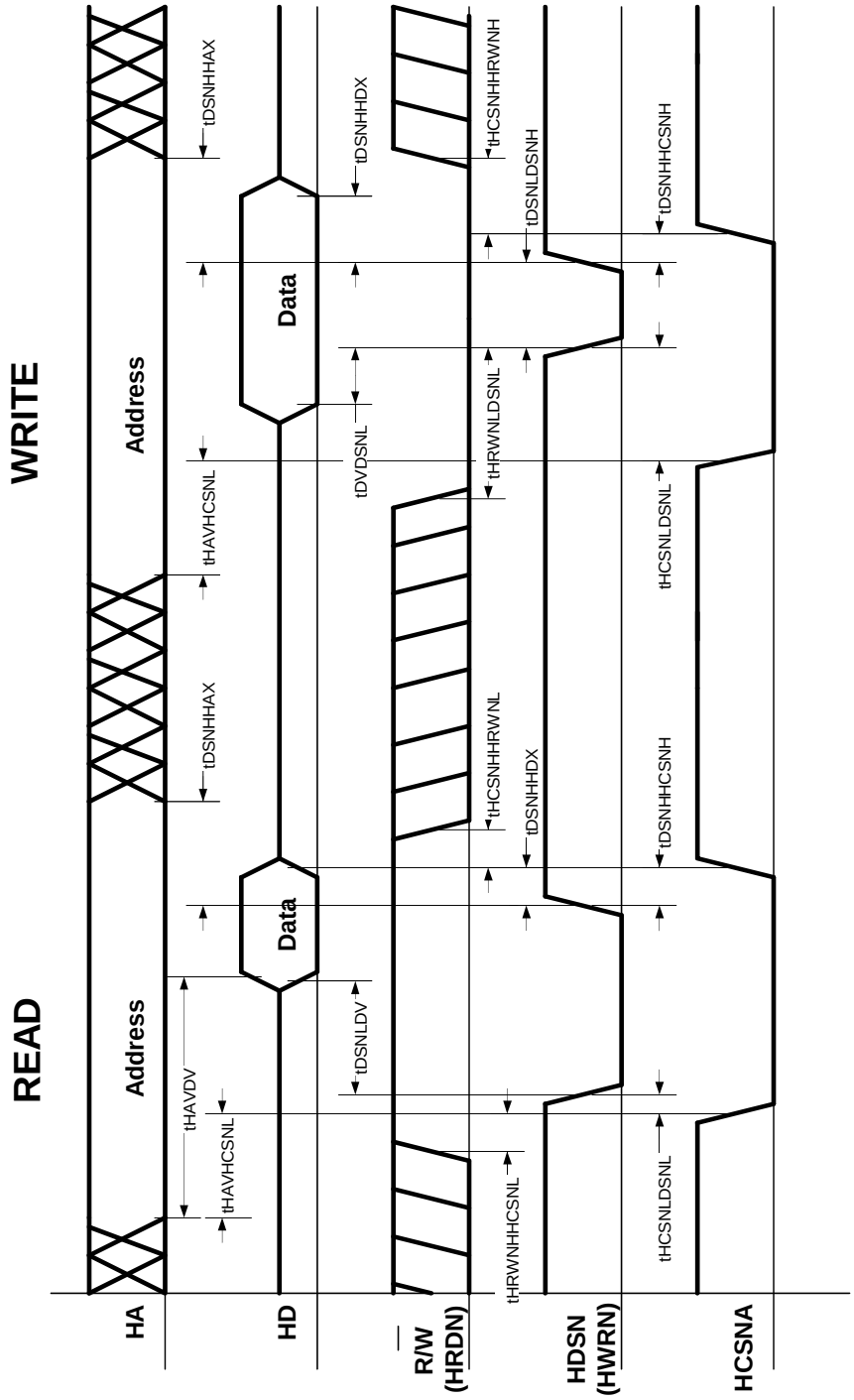


Figure 23: Motorola Bus Mode Timing Diagram

GS3137 ILD2 Specifications

Figure 24: GS3137 28-pin ILD2 Pin Diagram

NOTE:

The EPTSSOP is required to support a transmit power of higher than 15 dbm (HDSL2 and asymmetric PSD options for SHDSL).

Table 31: GS3137 ILD2 Signal Descriptions

Pin	Symbol	Type	Name / Function
1	Q1B	O	Data Output to DSP.
2	Q0B	O	
3	VDDD	P	**Digital Supply.** +3.3V.
4	GNDD	P	Digital Ground.
5	MCLK	I	**Master Clock from DSP.** Input to PLL which generates oversampling clocks.
6	CSD	I	**Control Input from DSP.** Configures the device.
7	DACA	I	Data Input from DSP.
8	DACB	I	
9	Q0A	O	Data Output to DSP.
10	Q1A	O	
11	RBIAS	I	External Bias Resistor Connection.
12	GNDA	P	**Analog Ground**.
13	VDDA	P	**Analog Supply**. +5V.
14	HYBN	I	**Negative Input from Hybrid Network.** See **NOTE**.
15	HYBP	I	**Positive Input from Hybrid Network.** See **NOTE**.
16	RCVN	I	**Negative Input from Line Transformer.** See **NOTE**.
17	RCVP	I	**Positive Input from Line Transformer.** See **NOTE**.
18	GNDA	P	**Analog Ground**.
19	VREFP	I	Positive Reference Voltage.

Table 31: GS3137 ILD2 Signal Descriptions

Pin	Symbol	Type	Name / Function
20	VCM	I	Common-mode Reference Voltage.
21	VREFN	I	Negative Reference Voltage.
22	VDDA	P	**Analog Supply**. +5V.
23	GNDA	P	**Analog Ground**.
24	LDOUTN	O	**Negative Line Driver Output**. See **NOTE**.
25	VDDA	P	**Analog Supply**. +5V.
26	LDOUTP	O	**Positive Line Driver Output**. See **NOTE**.
27	GNDA	P	**Analog Ground**.
28	VDDD	P	**PLL Supply 3.3V.** See **NOTE**.

NOTE:

Refer to your application schematics for all application-specific pin assignments.

Table 32: GS3137 ILD2 Electrical Characteristics

Parameter	Conditions	Min	Nom	Max	Unit
Absolute Maximum Ratings					
Power Supply Voltages	5V supply			7.0	V
	3.3V supply			3.6	V
Recommended Operating Conditions					
Power Supply Voltages	5V supply	4.75	5	5.25	V
	3.3V supply	3.135	3.3	3.465	V
Operating Temperature	–	-40	–	85	℃
Digital Inputs					
Input Logic High V_{IH}	$\lvert I_{IH} \rvert$ <10µA	DV_{DD}-1	–	–	V
Input Logic Low V_{IL}	$\lvert I_{IH} \rvert$ <10µA	- 0.3	–	0.8	V
Digital Outputs					
Output Logic High, V_{OH}	I_{OH}=-20µA	DV_{DD}-0.5	–	–	V
Output Logic Low, V_{OL}	I_{OL}=20µA	–	–	0.4	V

Manufacturing Information

Table 33: Device Manufacturing Characteristics

Parameter	Chip(s)	Conditions
Maximum Temperature Gradient	DSP and AFE	JEDEC Moisture Sensitivity Class 3 • Unsealed parts may be exposed to 30℃ 60% relative humidity for up to one week • If exposed more than one week, parts must be baked at 125℃ for 7 hours
Solder Profile	DSP and AFE	• 6℃/second maximum temperature ramp rate • 10-40 seconds at 220℃-225℃ (do not exceed 225℃) • 120-180 seconds above solder liquidus (approximately 183℃)

Thermal Performance

Table 34: Thermal Resistance

Product	Θ_{jA} at 0 LPM Air Velocity (^{o}C/W)	Θ_{jA} at 200 LPM Air Velocity (^{o}C/W)
160 PBGA DSP	29.0	24.7
28 SSOP AFE	49.8	43.9
28 EPTSSOP AFE	37.9	32.5

NOTE:
^{o}C/W = ^{o}C/Watts
LPM = Linear Feet Per Minute (LPM/196.8 = Meter/Second)
Θ_{JA}= Thermal Resistance - Junction to Ambient

Thermal data is obtained by mounting the chip set to a JEDEC standard board. The thermal performance in a custom board may vary. The following describes JEDEC standards:

In August (1996), the Electronics Industries Association released Standard EIA/JESD51-3 titled, “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.” This Standard provides guidelines for design of the test board used in taking thermal resistance measurements of integrated circuit packages. Prior to release of this Standard, thermal resistance data for similar packages varied greatly across the industry because of the use of different test board designs. In particular, the characteristics of the test board were found to have a dramatic impact on the measured Theta JA (Θ_{JA}). As the industry converts to using this standard test board design, the variation in thermal resistance data caused by the board should be minimized.

Key features of the standard test board design are:

- Board thickness: 0.062”
- Board dimension: 3.0" x 4.5" for packages < 27.0 mm
- Board dimension: 4.0" x 4.5" for packages > 27.0 mm

The JEDEC method for specifying the thermal performance of ICs does not reflect thermal performance at the line card or system level. Equipment OEMs must take thermal management into account in the design of systems featuring high-density line cards.

DSL Chip Set Outline Diagrams

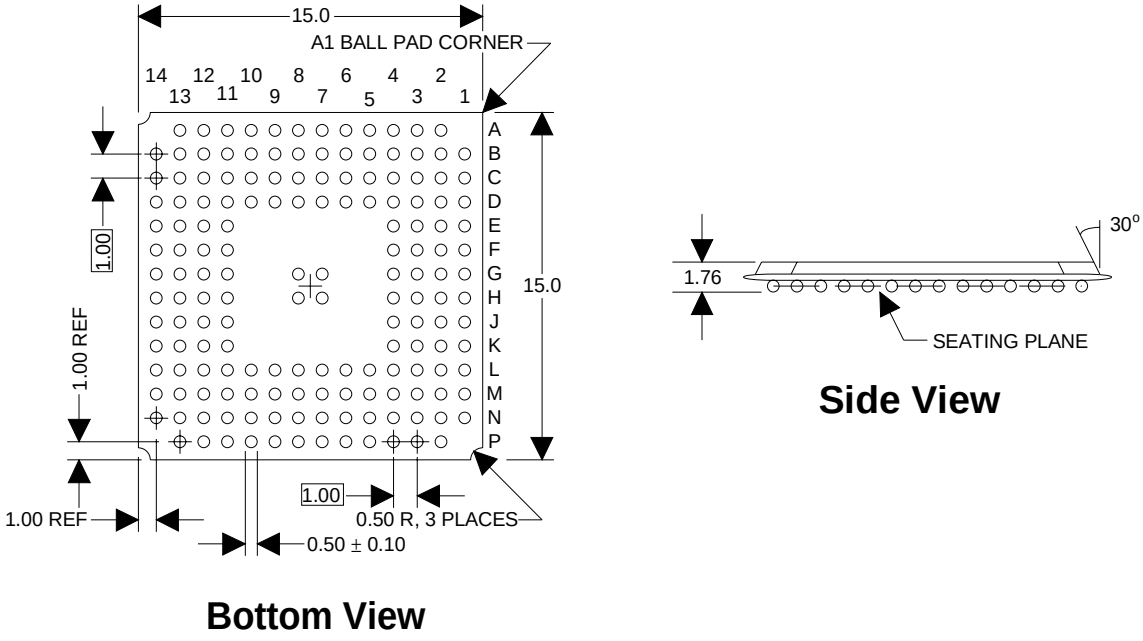


Figure 25: 160 PBGA Dual-Channel DSP/Framer Outline Diagram

The PBGA is a reliable, low-stress and high density packaging alternative.

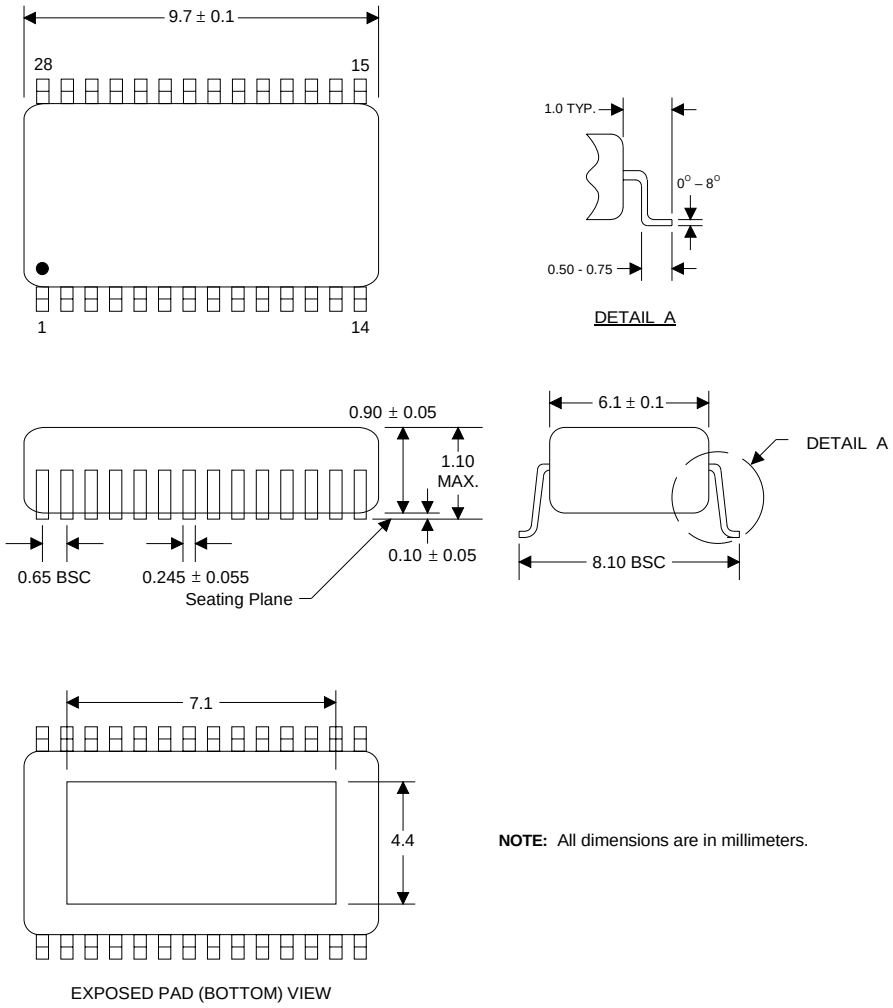


Figure 26: GS3137-08-TA ILD2 in 28 EPTSSOP package

NOTE:

Please make sure your PCB design takes into consideration the exposed PAD at the bottom of this package, which will need to be connected to the analog ground plane. The dimensions for this exposed pad are 7.1 mm x 4.4 mm located at the center of the device, as shown in the Bottom View above. Refer to Application Note DO-009653-AN, "Mounting Guidelines for GS3137-08T in a 28-pin EPTSSOP Package," for detailed mounting guidelines for this package.

Orion SDSL, HDSL2 and SHDSL - ILD2 Chip Set Order Information

Table 35: DSL Chip Set Part Number

Product	Supports	Chip Set	DSP/Framer	ILD2
SHDSL *Only*	Up to 2320 kb/s	G2237-208-041GA C1 G2237-208-041GA C1Z[a]	160 PBGA GS2237-208-001G C1 GS2237-208-001G C1Z[a]	28 EPTSSOP GS3137-08-TA GS3137-08-TAZ[a]

a. Lead (Pb)-free

Table 36: Device Packaging

Device	Part Number	Package	Production Orders	
			Minimum Order Quantity	Quantity Multiples
DSP	GS2237-208-001G C1 GS2237-208-001G C1Z[a]	160 PBGA	504	504
AFE	GS3137-08-TA GS3137-08-TAZ[a]	28 EPTSSOP	500	500

a. Lead (Pb)-free